HARRIS SEMICONDUCTOR

HS-9008RH

T-51-10-08

PRELIMINARY

December 1992

CMOS 8 Bit Flash Analog-to-Digital Converter

Features

- Excellent Noise Rejection - Fully Differential Design
- Superior Linearity (0.5LSB Typical)
- Single Reference Supply
- Low Power (400mW Typical)
- 20MHz Sampling Rate (50ns Conversion Time)
- Total Dose Hardness to 300KRAD

Description

The Harris HS-9008RH is a CMOS 8 Bit Flash Converter designed for space applications were relatively low power, exceptional accuracy and very fast conversion speeds are a necessity.

The HS-9008RH design differs substantially from most other available Flash Converters as it employs fully differential analog input sampling networks and amplifiers, as well as regenerative, offset nulled (error correcting) comparators. These circuit techniques improve noise performance and render the circuit much less sensitive to process and radiation induced device parametric shifts. Outstanding integral and differential linearity error is achieved through the use of a metal film resistor network which exhibits >10 bit linearity without trim. As a result of these innovations, the device operates with a single fixed reference supply as opposed to the multiple, adjustable references used in similar devices.

The HS-9008RH is fabricated in Harris' new AVLSI1RA process, which is dual level metal, twin well, thin EPI, 1.25µM junction isolated CMOS process. The capacitors are metal to metal with a nitride dielectric and have a negligible attenuation factor.

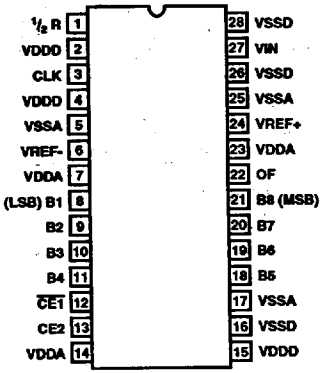
This combination of factors makes the HS-9008RH one of the best 8 Bit Flash Converters available in the Commercial, Military or Rad Hard markets.

Truth Table

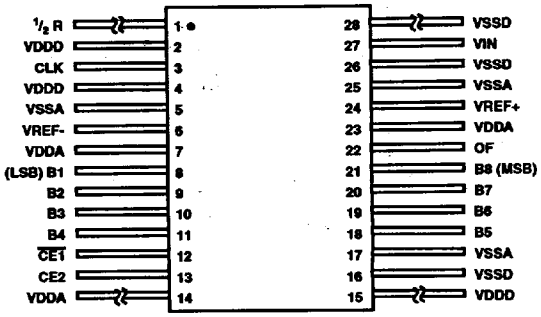
$\overline{CE1}$	CE2	B1 - B8	OF
0	1	Valid	Valid
1	1	Tri-State	Valid
X	0	Tri-State	Tri-State

Pinouts

28 PIN CERAMIC DIP CASE OUTLINE D1, CONFIGURATION 3
TOP VIEW



28 PIN FLATPACK CASE OUTLINE F11A, CONFIGURATION 2
TOP VIEW



5 DATA CONVERTERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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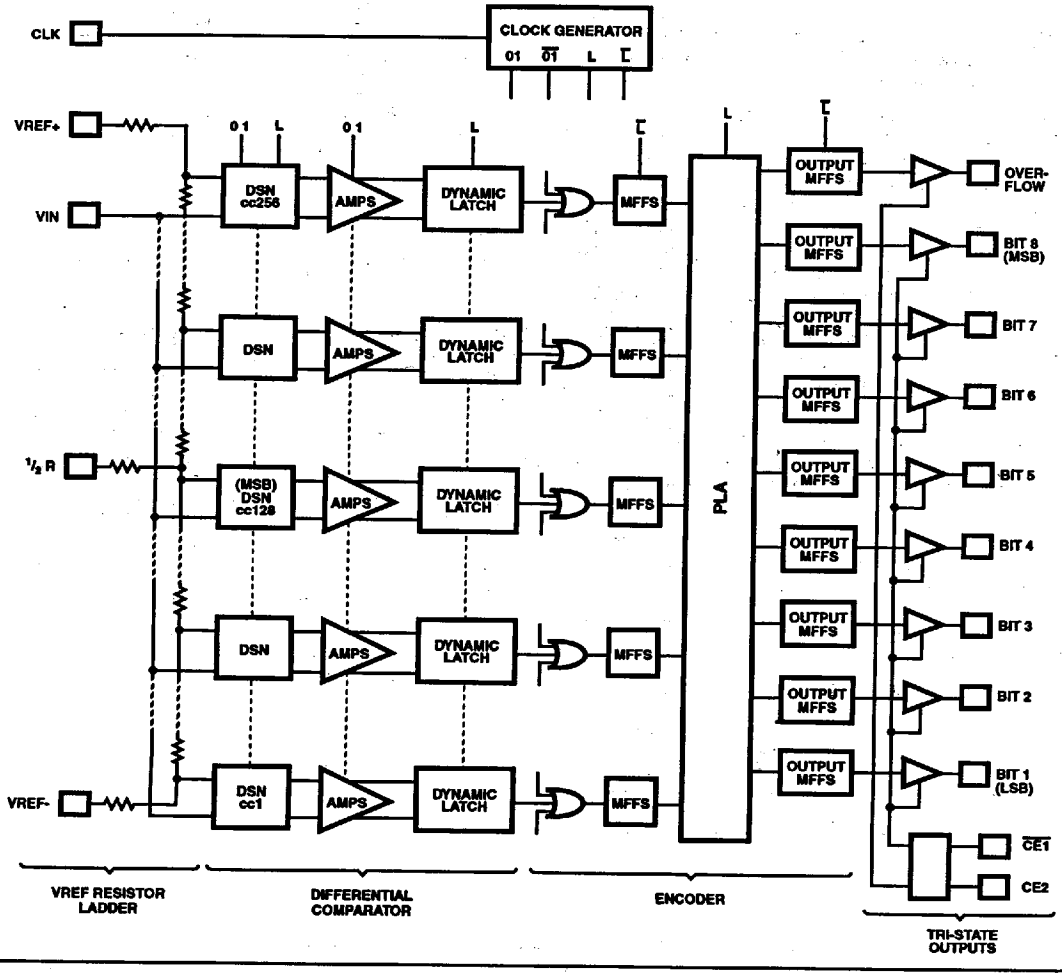
Pin Description

PACKAGE PIN 28 DIP/FP	NAME	DESCRIPTION
8	B1	(LSB) Output Data Bits
9	B2	Output Data Bits
10	B3	Output Data Bits
11	B4	Output Data Bits
18	B5	Output Data Bits
19	B6	Output Data Bits
20	B7	Output Data Bits
21	B8	(MSB) Output Data Bits
22	OF	Overflow
16, 26, 28	VSSD	Digital Ground

PACKAGE PIN 28 DIP/FP	NAME	DESCRIPTION
2, 4, 15	VDDD	Digital Supply
13	CE2	Tri-State Output Enable
12	$\overline{CE1}$	Tri-State Output Enable
6	VREF-	Negative Reference Input
27	VIN	Analog Signal In
5, 17, 25	VSSA	Analog Ground
3	CLK	Clock Input
1	1/2 R	Reference Midpoint
24	VREF+	Positive Reference Input
7, 14, 23	VDDA	Analog Supply

Functional Diagram



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Specifications HS-9008RH

Absolute Maximum Ratings

DC Supply Voltage Range, VDDD = VDDA
(Referenced to VSSD = VSSA = GND) ..... -0.3V to +7.0V
Input Voltage Range: $\overline{CE1}$, CE2, CLK, VREF-,
VREF+, VIN, $^1/_2$ R ..... VSS -0.3V to VDD +0.3V
Output Voltage Range: B1 - B8, OF
(Outputs Off) ..... VSS -0.3V to VDD.+0.3V
DC Input Current $\overline{CE1}$, CE2, CLK, VIN, B1 - B8, OF 10mA
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +265°C

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
28 Flatpack Package	TBD	TBD
28 Ceramic DIP Package	TBD	TBD
24 Flatpack Package	TBD	TBD

Package Power Dissipation
For T_A = -55°C to +125°C ..... TBD

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range (VDDD = VDDA) ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Digital Input Low Voltage ..... 0V to +0.2VDDD
Input High Voltage ..... 0.8VDDD to VDDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

All Typical Values Represent +25°C, Nominal Conditions and have been characterized but are not tested.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Resolution		VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	1, 2, 3	-55°C to +125°C	8	-	-	Bits
Integral Linearity Error	ILE	VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	1, 2, 3	-55°C to +125°C	-	±0.5	±1.0	LSB
Differential Linearity Error	DLE	VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	1, 2, 3	-55°C to +125°C	-	±0.25	±0.5	LSB
Offset Error	VOS	VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), VIN = VREF- + 0.5LSB	1, 2, 3	-55°C to +125°C	-	-	±1.25	LSB
Gain Error	GE	VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), VIN = VREF+ - 1.5LSB	1, 2, 3	-55°C to +125°C	-	-	±2.25	LSB
Ladder Impedance	Ref	VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	1, 2, 3	-55°C to +125°C	300	500	600	Ω
Full Scale Range (VIN and (VREF+) - (VREF-))		VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	1, 2, 3	-55°C to +125°C	-	4	5	V
Supply Current (IDDD + IDDA + IREF) Dynamic	IDDD	VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), CLK = 25MHz (Note 1)	1, 2, 3	-55°C to +125°C	-	60	135	mA
Static	IDDS	VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), CLK = High	1, 2, 3	-55°C to +125°C	-	40	80	mA

NOTE:
1. *For typical value, CLK = 1MHz.*

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TABLE 2A. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

All Typical Values Represent +25°C, Nominal Conditions and have been characterized but are not tested.

PARAMETERS	SYMBOL	CONDITIONS		GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Conversion Speed		VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), CLK = 50% Duty Cycle, Square Wave		9, 10, 11	-55°C to +125°C	20	-	-	MSPS
Full Power Bandwidth		VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), VIN = Full Scale Sine Wave (Note 1)		9, 10, 11	-55°C to +125°C	-	10	-	MHz
Differential Gain Error		VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), (Note 2)		9, 10, 11	-55°C to +125°C	-	-	2.5	%
Differential Phase Error		VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), (Note 2)		9, 10, 11	-55°C to +125°C	-	-	2.5	Deg.
Total Harmonic Distortion	THD	VDDD = VDDA = 5V, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	CLK = 1MHz	9, 10, 11	-55°C to +125°C	-	-	-48	dB
			CLK = 10MHz	9, 10, 11	-55°C to +125°C	-	-	-48	dB
			CLK = 20MHz	9, 10, 11	-55°C to +125°C	-	-	-48	dB
Signal-to-Noise Ratio (Plus Distortion)	SNRD	VDDD = VDDA = 5V, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	CLK = 1MHz	9, 10, 11	-55°C to +125°C	47	-	-	dB
			CLK = 10MHz	9, 10, 11	-55°C to +125°C	47	-	-	dB
			CLK = 20MHz	9, 10, 11	-55°C to +125°C	42	-	-	dB

NOTE:

1. The -3dB bandwidth for frequency response purposes is greater than 30MHz.
2. VIN = 3.58MHz burst, CLK = 14MHz, 6 DC levels (2.0, 2.2, 2.4, 2.6, 2.8, 3.0V).

TABLE 2B. AC ELECTRICAL SWITCHING CHARACTERISTICS

All Typical Values Represent +25°C, Nominal Conditions and have been characterized but are not tested.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Track Time (Auto Balance Time)	TTRACK	VDDD = VDDA = 5V, CLK = 25MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), CLK = High	9, 10, 11	-55°C to +125°C	20	-	-	ns
Hold Time	THOLD	VDDD = VDDA = 5V, CLK = 25MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), CLK = Low	9, 10, 11	-55°C to +125°C	20	-	-	ns
Data Output Delay	TOD	VDDD = VDDA = 5V, CLK = 25MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	9, 10, 11	-55°C to +125°C	-	-	35	ns
Output Enable Time	TEN	VDDD = VDDA = 5V, CLK = 25MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	9, 10, 11	-55°C to +125°C	-	-	25	ns
Output Disable Time	TDIS	VDDD = VDDA = 5V, CLK = 25MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	9, 10, 11	-55°C to +125°C	-	-	25	ns

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TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

All Typical Values Represent +25°C, Nominal Conditions and have been characterized but are not tested.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Digital Input Capacitance	CI	f = 1MHz, VDDD = VDDA = OPEN, VSSD = VSSA = 0V, T_A = +25°C	1, 2	+25°C	-	-	15	pF
			1, 3	+25°C	-	-	15	pF
Output Capacitance	CO	f = 1MHz, VDDD = VDDA = OPEN, VSSD = VSSA = 0V, T_A = +25°C	1, 2	+25°C	-	-	10	pF
			1, 3	+25°C	-	-	10	pF
Analog Input Capacitance (Static)	CIN	CLK = High, VDDD = VDDA = 5V, VSSD = VSSA = 0V, VREF = 4.000V (Adj.),	1	-55°C to +125°C	-	70	-	pF
Analog Input Capacitance (Dynamic)	DYNCIN	CLK = 3MHz, VDDD = VDDA = 5V, VSSD = VSSA = 0V, VREF = 4.000V (Adj.),	1	-55°C to +125°C	-	30	-	pF
Aperture Delay		VDDD = VDDA = 5V, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	1	-55°C to +125°C	-	TBD	-	ns
Aperture Jitter		VDDD = VDDA = 5V, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	1	-55°C to +125°C	-	TBD	-	ps
Analog DC Input Current	IREF	VIN = 4.0V, VDDD = VDDA = 5V, VSSD = VSSA = 0V, VREF = 4.000V (Adj.),	1	-55°C to +125°C	-	2	-	mA
Power Supply Rejection	PSR	VDDD = VDDA = 5.5V, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	1	-55°C to +125°C	-	<1.0	-	LSB/V

NOTES:

1. The parameters listed in Table 3 are controlled via design or process and are not tested. These parameters are characterized upon initial design release.
2. 28 Pin DIP package only.
3. 28 Pin Flatpack package only.

TABLE 4. POST 300KRAD ELECTRICAL PERFORMANCE CHARACTERISTICS

Post 300KRAD Electrical Performance is per Tables 1, 2, and 3

TABLE 5. BURN-IN DELTA PARAMETERS (T_A = +25°C)

TBD

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	Q SUBGROUPS
Initial Test		100%/5004	1, 7, 9
PDA		100%/5004	1, 7, Δ
Final Test		100%/5004	1, 7, 9
Group A		Samples/5005	1, 2, 3, 7, 8, 9, 10, 11
Group B	B5	Samples/5005	1, 2, 3, 7, 8, 9, 10, 11
	Others	Samples/5005	1, 7
Group D		Samples/5005	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9

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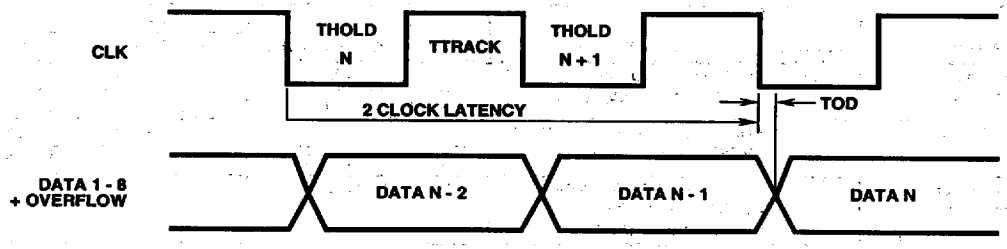
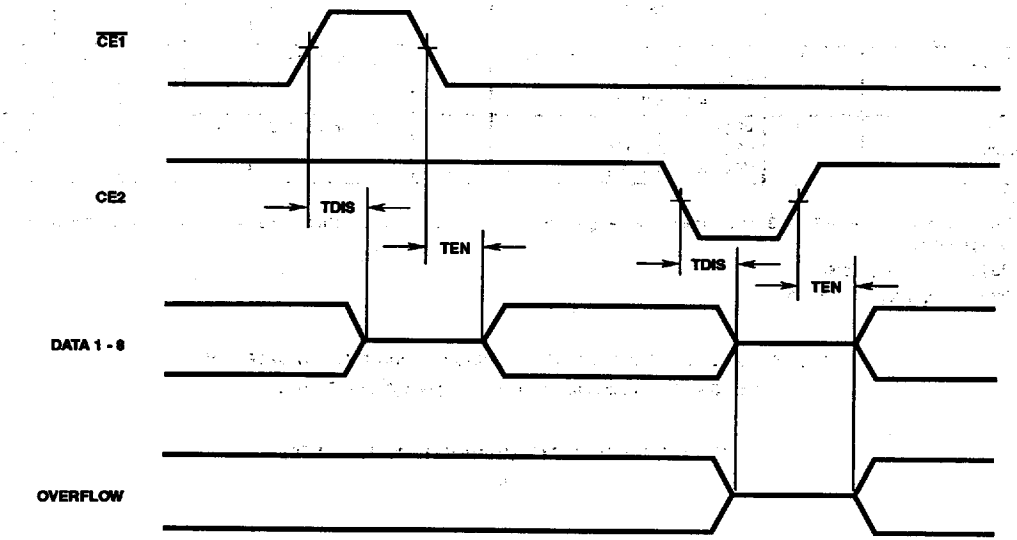
Timing Diagrams

INPUT TIMING



OUTPUT ENABLE TIMING



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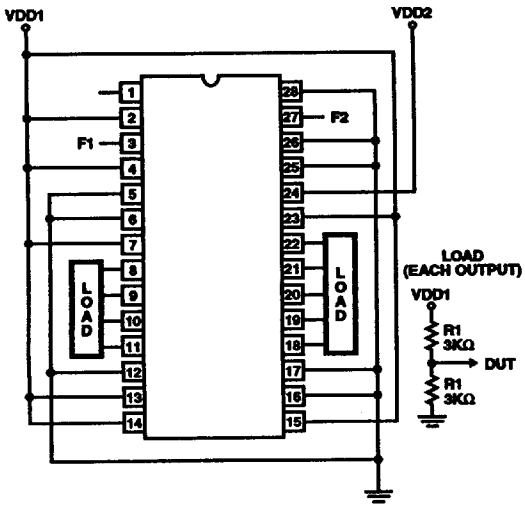
Burn-In Diagram

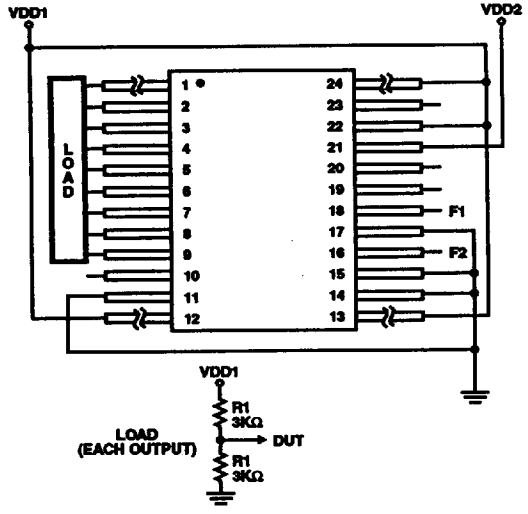
HS-9008RH 28 PIN DIP/FLATPACK



DYNAMIC

NOTES:
VDD1 = 5.5V Min
VDD2 = 4V Min
Input Signals: F1 = 1MHz (50% Duty Cycle); F2 = F1/4
VIH = 5V, +0.5V, -0; VIL = 0V, +0.5V, -0

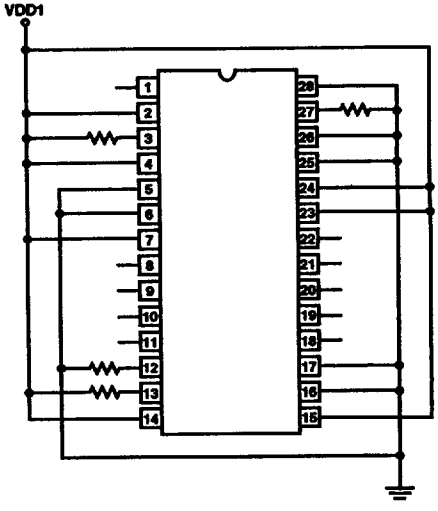
HS-9008RH 24 PIN FLATPACK



DYNAMIC

NOTES:
VDD1 = 5.5V Min
VDD2 = 4V Min
Input Signals: F1 = 1MHz (50% Duty Cycle); F2 = F1/4
VIH = 5V, +0.5V, -0; VIL = 0V, +0.5V, -0

Irradiation Circuit



NOTES:
All Total Dose Testing is performed using the HS1-9008RH package (28 DIP)
VDD1 = 5.5V Min
Resistors = 10KΩ ± 10%
Total Dose = 300KRADS

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