# Am81C471/478

## CMOS Color Palette

Advanced
Micro
Devices

## DISTINCTIVE CHARACTERISTICS

- Plug-In replacements for Bt471 and Bt478
- VGA hardware and software compatible
- Available in 35, 50, 66, 80 MHz versions
- Available in 44-pin PLCC package
- 256 x 18(24) Color Palette RAM
- 15 x 18(24) Overlay RAM

- Triple 6-bit (8-bit) DACs
- Sync on all three outputs
- RS-343A/RS-170 compatible RGB outputs
- External current or voltage reference
- Standard MPU interface
- Single +5 V power supply

## GENERAL DESCRIPTION

The Am81C471/478 CMOS Color Palette has been designed specifically for the VGA market. Applications include high-resolution color graphics, CAD/CAM/CAE, and desktop publishing. The Am81C471 and Am81C478 operate at speeds sufficient to support monitor sizes of 1024 X 768 pixels.

The Am81C471/478 has a 256 x 18(24) look-up table and 15 X 18(24) overlay regsiters and as such can simultaneously display 271 colors out of an available set of 65K (16.8 million) colors. The Am81C471 has triple 6-bit video DACs; the Am81C478 may be used in either 6-bit or 8-bit mode.

The Am81C471/478 also include input buffers and programmable bit-plane Read Masks. They are available in versions with pixel rates as high as 80 MHz. Proprietary

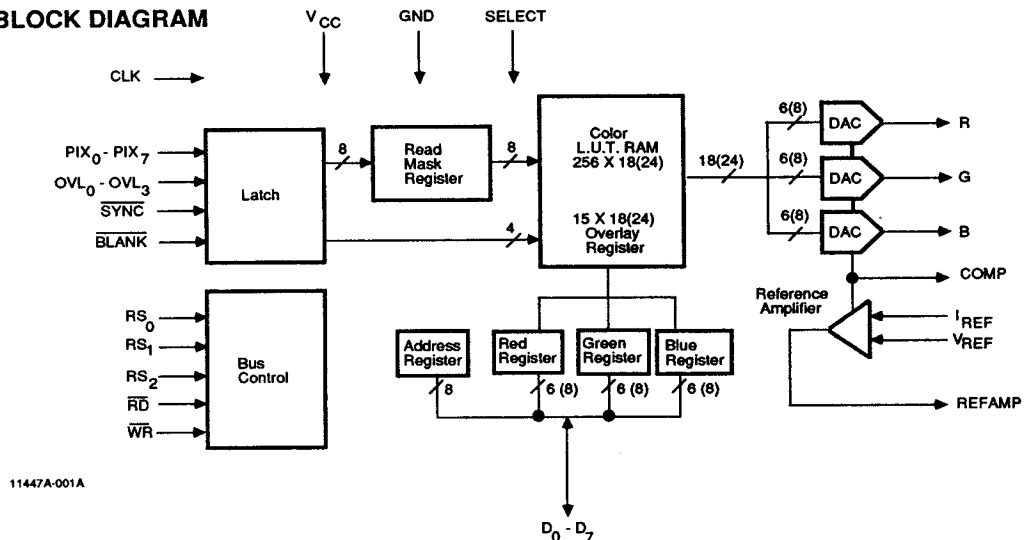DAC decoding techniques minimize glitch energy and skew.

Both the Am81C471 and Am81C478 include programmable pedestals (0 or 7.5 IRE) and can be used with an external voltage or current reference. EGA emulation, overlaying cursors, text, grids, etc. can be implemented using the 15 overlay registers.

The Am81C471/478 generate RS-343A compatible outputs into doubly-terminated 75 Ω loads and RS-170 compatible output into a singly-terminated 75 Ω load, without external buffers.

The Am81C471 and Am81C478 are fabricated using AMD's state-of-the-art 1.2μ CMOS process. The devices are available in a 44-lead PLCC package.
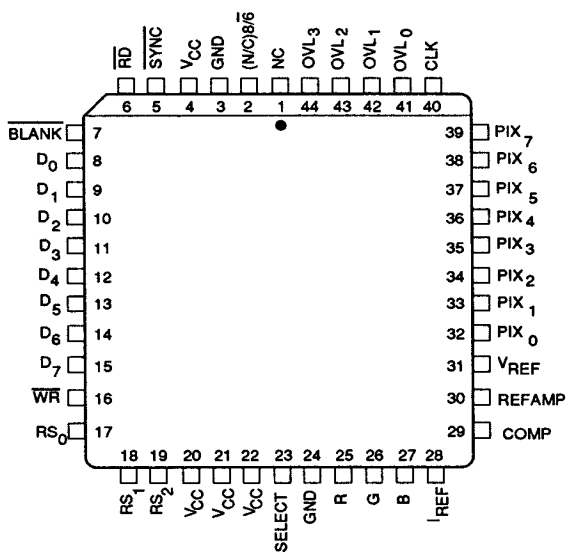
## BLOCK DIAGRAM



11447A-001A

Am81C471/478

3-137

## CONNECTION DIAGRAM

**PLCC**

**(Top View)**

Top pins (6 to 40): $\overline{RD}$, $\overline{SYNC}$, $V_{CC}$, GND, (N/C)8/6, NC, $OVL_3$, $OVL_2$, $OVL_1$, $OVL_0$, CLK

Pin numbers top: 6, 5, 4, 3, 2, 1, 44, 43, 42, 41, 40

Left side pins:
- $\overline{BLANK}$ — 7
- $D_0$ — 8
- $D_1$ — 9
- $D_2$ — 10
- $D_3$ — 11
- $D_4$ — 12
- $D_5$ — 13
- $D_6$ — 14
- $D_7$ — 15
- $\overline{WR}$ — 16
- $RS_0$ — 17

Right side pins:
- 39 — $PIX_7$
- 38 — $PIX_6$
- 37 — $PIX_5$
- 36 — $PIX_4$
- 35 — $PIX_3$
- 34 — $PIX_2$
- 33 — $PIX_1$
- 32 — $PIX_0$
- 31 — $V_{REF}$
- 30 — REFAMP
- 29 — COMP

Bottom pin numbers: 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28

Bottom pins: $RS_1$, $RS_2$, $V_{CC}$, $V_{CC}$, $V_{CC}$, SELECT, GND, R, G, B, $I_{REF}$

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Note: Pin 1 is marked for orientation.

## LOGIC DIAGRAM

Inputs:
- CLK
- $\overline{BLANK}$
- $\overline{SYNC}$
- 8 — $PIX_0$ - $PIX_7$
- 4 — $OVL_0$ - $OVL_3$
- $V_{REF}$
- $I_{REF}$
- COMP
- 8 — $D_0$ - $D_7$
- $\overline{RD}$
- $\overline{WR}$
- $RS_0$ - $RS_2$
- 8 / $\overline{6}$
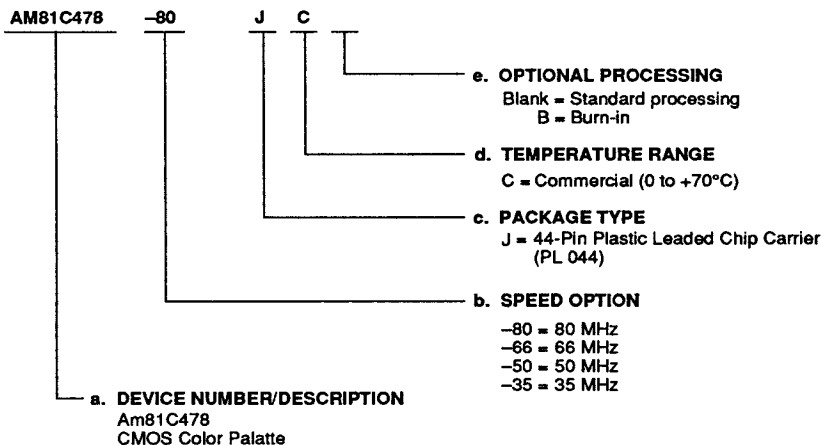- SELECT

Outputs:
- R
- G
- B
- REFAMP
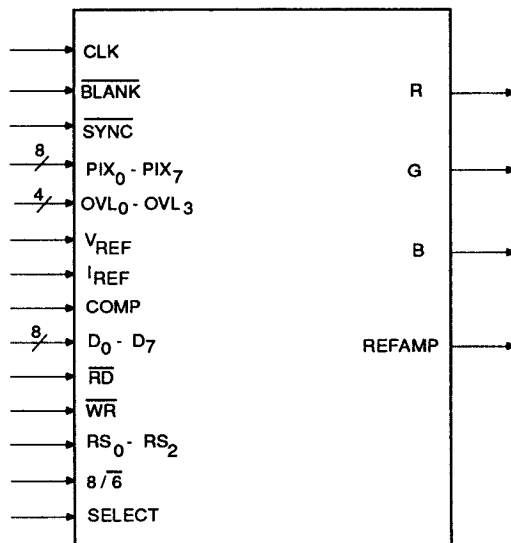
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# ORDERING INFORMATION

## Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
   a. **Device Number**
   b. **Speed Option** (if applicable)
   c. **Package Type**
   d. **Temperature Range**
   e. **Optional Processing**

```
AM81C478    –80      J   C
```

**e. OPTIONAL PROCESSING**
   Blank = Standard processing
   B = Burn-in

**d. TEMPERATURE RANGE**
   C = Commercial (0 to +70°C)

**c. PACKAGE TYPE**
   J = 44-Pin Plastic Leaded Chip Carrier
   (PL 044)

**b. SPEED OPTION**
   –80 = 80 MHz
   –66 = 66 MHz
   –50 = 50 MHz
   –35 = 35 MHz

**a. DEVICE NUMBER/DESCRIPTION**
   Am81C478
   CMOS Color Palatte

| Valid Combinations | |
|---|---|
| AM81C471-80 | |
| AM81C471-66 | |
| AM81C471-50 | |
| AM81C471-35 | JC, JCB |
| AM81C478-80 | |
| AM81C478-66 | |
| AM81C478-50 | |
| AM81C478-35 | |

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

   * Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

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# PIN DESCRIPTION

## Timing Section

### CLK
### Clock source pin (TTL compatible Input)
This input operates at the pixel clock rate of the system. It is to be driven by a dedicated TTL buffer. The rising edge of CLK latches the $\overline{SYNC}$, $\overline{BLANK}$, $PIX_0$–$PIX_7$, and $OVL_0$–$OVL_3$ inputs.

### $\overline{BLANK}$
### Blank (TTL compatible Input)
The $\overline{BLANK}$ input, when active, overrides the color pixel and overlay data to force the R,G, and B video outputs to their blank levels. This blank level is required during the monitor's vertical and horizontal retrace times. It is latched on the rising edge of CLK.

### $\overline{SYNC}$
### Sync (TTL compatible Input)
The $\overline{SYNC}$ input, when active, switches off a current source on the R, G, and B video outputs. It is latched on the rising edge of CLK. Because $\overline{SYNC}$ does not override any other input or control pin, it should be asserted only during blanking intervals.

## Bit Map Interface Section

### $PIX_0$–$PIX_7$
### Color Pixel Data addresses
###    (TTL compatible inputs)
These 8 inputs select which of the 256 entries in the Color Palette look-up table is to be used to provide pixel color information. They are latched into the input buffer on the rising edge of CLK. $PIX_0$ is the least significant bit. Unused inputs should be grounded.

### $OVL_0$–$OVL_3$
### Overlay Data address (TTL compatible Inputs)
These 4 inputs select which of the 15 overlay registers is to be used to provide color information. They are latched into the input buffer on the rising edge of CLK. The $PIX_0$–$PIX_7$ inputs are ignored when the overlay palette is accessed. $OVL_0$ is the least significant bit. Unused inputs should be grounded.

## MPU Interface Section

### $D_0$–$D_7$
### Data and address bus (TTL compatible bi-directional)
These 8 pins are used to load and read back the Color look-up table and the internal control registers. $D_0$ is the least significant bit.

### $\overline{RD}$
### Read Control Input (TTL compatible Input)
$\overline{RD}$ must be a logical zero to read data from the Color look-up table or any of the registers. During Read operations, $RS_0$–$RS_2$ are latched on the falling edge of $\overline{RD}$.

### $\overline{WR}$
### Write Control Input (TTL compatible Input)
$\overline{WR}$ must be a logical zero to write data to the Color look-up table or any of the registers. During Write operations, $RS_0$–$RS_2$ are latched on the falling edge of $\overline{WR}$.

### $RS_0$–$RS_2$
### Register Select Inputs (TTL compatible Inputs)
$RS_0$–$RS_2$ allow the MPU to address any location in the Color look-up tables or any of the internal control registers. These inputs determine the type of read or write operation being performed.

### $8/\overline{6}$
### 8-bit/6-bit Select Input (TTL compatible Input).
This pin is not used on the Am81C471 and should not be connected. For the Am81C478, this pin determines whether the MPU is reading or writing 8-bits (logical one) or 6-bits (logical zero) of information during each cycle. In 8-bit operation, $D_7$ is the most significant bit. In 6-bit operation $D_5$ is the most significant bit; $D_6$ and $D_7$ are ignored during write cycles and are logical zero during read cycles.

## Analog Output Section

### R
### Red video output (Analog output)
Analog output of the red DAC. This output is capable of driving an RS-343A compatible doubly-terminated 75 Ω cable and an RS-170 compatible singly terminated 75 Ω cable.

### G
### Green video output (Analog output)
Analog output of the green DAC. This output is capable of driving an RS-343A compatible doubly-terminated 75 Ω cable and an RS-170 compatible singly terminated 75 Ω cable.

### B
### Blue video output (Analog output)
Analog output of the blue DAC. This output is capable of driving an RS-343A compatible doubly-terminated 75 Ω cable and an RS-170 compatible singly terminated 75 Ω cable.

### $V_{REF}$
### Voltage reference (Analog input).
An external voltage reference circuit such as the one shown in Figure A1 must supply this input with a 1.235 volt (typical) reference.

### $I_{REF}$
### Current reference (Analog input).
### Voltage Mode:
When an external voltage reference is used the $R_{SET}$ resistor connecting this pin and GND controls the magnitude of the full scale video signal according to the following relationship:

$$R_{SET} \text{ (ohms)} = K \cdot 1,000 \cdot V_{REF} \text{ (V)} / I_{out} \text{ (mA)}$$

The table shown below defines K along with $R_{SET}$ values for doubly-terminated 75 Ω loads.

| Mode | Pedestal | K | $R_{SET}$ (Ω) |
|---|---|---|---|
| 6-bit | 7.5 IRE | 3.025 | 147 |
| 8-bit | 7.5 IRE | 3.200 | 148 |
| 6-bit | 0 IRE | 3.000 | 139 |
| 8-bit | 0 IRE | 3.175 | 140 |

### Current Mode:
When an external current reference is used, the relationship between $I_{REF}$ and the full scale output current on each video output is given by:

$$I_{REF} \text{ (mA)} = I_{out} \text{ (mA)} / K$$

### REFAMP
### Reference Amplifier Output (Analog output)
When an external voltage reference is used, this pin should be connected to COMP. When an external current reference is used this pin should be left floating.

### COMP
### Compensation capacitor connection (Analog input)
A 0.1 μF ceramic capacitor is connected between this pin and $V_{CC}$. This pin should be connected to REFAMP when an external voltage reference is used. When an external current reference is used this pin should be connected to $I_{REF}$.

## Power Supply Section

### $V_{CC}$
Analog +5 volt supply

### SELECT
### Select control input (TTL-compatible input)
This pin selects either a 0 IRE (SELECT = GND) or 7.5 IRE (SELECT = $V_{CC}$) blanking pedestal.

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## FUNCTIONAL DESCRIPTION

The Am81C471/478 CMOS Color Palette integrates all major functions required in the backend of a video system and supports pixels rates sufficient to drive most low-to-medium resolution monitors (including 1024 X 768).

A programmable look-up table maps the pixel data from a frame buffer into physical color and three Digital-to-Analog-Converters (DACs) convert the digital outputs of the look-up table into RS-343A compatible RGB analog outputs.

## Microprocessor Interface

The Am81C471/478 is designed to support a standard microprocessor bus interface with direct access to 256 look-up table (LUT) RAM locations, 15 overlay registers, and two control registers. The microprocessor interface is asynchronous with respect to pixel clock. However, data transfers between the LUT RAM or overlay registers and the Red Register, Green Register, and Blue Register as shown in the block diagram are synchronized to pixel clock. Such read and write operations take one and two pixel clock cycles, respectively.

The nature of the microprocessor operation is determined by examining the $RS_0$–$RS_2$ inputs. The $RS_0$–$RS_2$ select among the address register, the 256 LUT RAM locations, 15 overlay registers, or the Read Mask register, as shown in Table 1.

### Table 1. $RS_0$–$RS_2$ Decoding

| $RS_2$ | $RS_1$ | $RS_0$ | Function |
|---|---|---|---|
| 0 | 0 | 0 | Write Mode RAM Look-Up-Table Address Register |
| 0 | 1 | 1 | Read Mode RAM Look-Up-Table Address Register |
| 0 | 0 | 1 | Color Palette RAM Look-Up-Table |
| 0 | 1 | 0 | Pixel Read Mask Register |
| 1 | 0 | 0 | Write Mode Overlay Address Register |
| 1 | 1 | 1 | Read Mode Overlay Address Register |
| 1 | 0 | 1 | Overlay Registers |
| 1 | 1 | 0 | Reserved |

A typical color data write cycle is initiated by setting the 8-bit Address Register with the desired address of the LUT RAM (Overlay Registers) with the proper setting of $RS_0$–$RS_2$. Next, the microprocessor performs three write cycles to the color palette: one for Red, one for Green, and one for Blue data with the $RS_0$–$RS_2$ selecting either the LUT RAM or $RS_0$ of the the Overlay Registers. At the end of the blue cycle the data is concatenated into a 24-bit word (18 bits for the Am81C471 or for the Am81C478 with the 8/$\overline{6}$ input set LOW) and subsequently written to the LUT RAM location (Overlay Register) pointed to by the Address Register. The Address Register is then auto-incremented to point to the next LUT RAM location in the LUT RAM (to the next Overlay Register). This process may be repeated again as required by the microprocessor. See Table 2.

A typical color data read cycle is initiated by setting the 8-bit Address Register with the desired address of the LUT RAM (Overlay Registers) with the proper setting of $RS_0$–$RS_2$. Next, the microprocessor performs three read cycles to the color palette: one for Red, one for Green, and one for Blue data with the $RS_0$–$RS_2$ selecting either the LUT RAM or one of the Overlay Registers. At the end of the blue cycle the Address Register is auto-incremented to point to the next LUT RAM location in the LUT RAM (to the next Overlay Register). This process may be repeated again as required by the microprocessor. See Table 2.

For the Am81C471 (and for the Am81C478 with the 8/$\overline{6}$ pin set LOW), the 6-bit color data occupies the six least significant positions of the data bus. Bits $D_6$ and $D_7$ are ignored during write cycles and are set to 0 during read cycles. Bit $D_0$ is the least significant bit (LSB).

The Am81C471/478 uses one 8-bit Address Register to address both the LUT RAM and the Overlay Registers as shown in Table 3. During access to the Overlay Registers the upper four bits of the Address Registers are ignored. The Address Register resets to 0 after a blue read/write cycle to the LUT RAM address 255. A user-transparent modulo-3 counter (ARb, ARa) keeps track of the read, green, and blue cycles and auto-increments at the end of each read/write access to the LUT RAM or Overlay Registers. This counter is reset to zero after a write access to the Address Register and is unchanged following a read access to the Address Register.

The Am81C471/478 uses the 8-bit Pixel Read Mask Register to modify the address of the LUT RAM as provided by $PIX_0$–$PIX_7$. The eight bits of this register are ANDed with $PIX_0$–$PIX_7$ and the result used as the address to the LUTRAM. This masking mechanism provides a quick way to alter the appearance of one or more colors on the display unit with just one microprocessor access.

## Display Memory Interface

The color inputs, $PIX_0$–$PIX_7$ and $OVL_0$–$OVL_3$ are latched on the rising edge of CLK and are used as address to the 256 locations of the LUT RAM and the 15 Overlay Registers, respectively.

The total pipeline delay from the digital inputs $PIX_0$–$PIX_7$, $OVL_0$–$OVL_3$, $\overline{SYNC}$, and $\overline{BLANK}$ to the analog R, G, and B outputs is four clock cycles.

## Video Generation

During each clock cycle, a 24-bit word (18-bits for the Am81C471 or for the Am81C478 with the 8/$\overline{6}$ input set LOW) from either the LUT RAM or the Overlay Registers is presented to the three DACs. The three DACs convert the digital color memory output into RGB RS-343A analog format.

The $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs are latched on the rising edge of CLK. These two inputs are responsible for adding weighted currents to RGB analog outputs as shown in Figures 1 and 2.

Tables 4 and 5 show how the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs change analog output levels.

The $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs are routed to the three DACs after a delay equal to four clock periods, identical to the delay incurred by the video stream.

To specify which blanking pedestal is to be applied, the SELECT input is used; if SELECT is set to logical zero, the blanking pedestal is 0.0 IRE and if SELECT is set to logical one, the blanking pedestal is 7.5 IRE.

The three analog outputs of the Am81C471/478 are each capable of driving a doubly terminated 75 Ω coaxial cable.

### Table 2. Read/Write Access to the Am81C471/478

| $\overline{\text{RD}}$ | $\overline{\text{WR}}$ | RS$_2$ | RS$_1$ | RS$_0$ | ARb | ARa | FUNCTION | |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | X | X | Write Address Register; (LUT Write) | AR(7:0) ← D(7:0); ARb, ARa ← 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | Write Red Color; | RREG(7:0) ← D(7:0); INC. ARb, ARa |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | Write Green Color; | GREG(7:0) ← D(7:0); INC. ARb, ARa |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | Write Blue Color; | BREG(7:0) ← D(7:0); ARb, ARa ← 0; |
| | | | | | | | Write Color Look-Up-Table: R(7:0) ← RREG; G(7:0) ← GREG; B(7:0) ← BREG; INC AR(7:0) | |
| 1 | 0 | 1 | 0 | 0 | X | X | Write Address Register; (Overlay Write) | AR(7:0) ← D(7:0); ARb, ARa ← 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | Write Red Color; | RREG(7:0) ← D(7:0); INC. ARb, ARa |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | Write Green Color; | GREG(7:0) ← D(7:0); INC. ARb, ARa |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | Write Blue Color; | BREG(7:0) ← D(7:0); ARb, ARa ← 0; |
| | | | | | | | Write Overlay Register; ; R(7:0) ← RREG; G(7:0) ← GREG; B(7:0) ← BREG; INC AR(7:0) | |
| 1 | 0 | 0 | 1 | 1 | X | X | Write Address Register; (LUT Read) | AR(7:0) ← D(7:0); ARb, ARa ← 0; RREG ← R(7:0); GREG ← G (7:0); BREG ← B(7:0) |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | Read LUT Red; | D (7:0) ← RREG(7:0); INC. ARb, ARa |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | Read LUT Green; | D(7:0) ← GREG(7:0); INC. ARb, ARa |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | Read LUT Blue; | D(7:0) ← BREG(7:0); ARb, ARa ← 0; INC AR(7:0) |
| 1 | 0 | 1 | 1 | 1 | X | X | Write Address Register; (Overlay Read) | AR(7:0) ← D(7:0); ARb, ARa ← 0; RREG ← R(7:0); GREG ← G (7:0); BREG ← B(7:0) |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | Read Overlay Red; | D(7:0) ← RREG(7:0); INC. ARb, ARa |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | Read Overlay Green ; | D(7:0) ← GREG(7:0); INC. ARb, ARa |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | Read Overlay Blue ; | D(7:0) ← BREG(7:0); ARb, ARa ← 0; INC AR(7:0) |

Note: Refer to timing diagrams for edge information on $\overline{\text{RD}}$ and $\overline{\text{WR}}$.

### Table 3. Address Register Operation

| AR(7:0) | RS$_2$ | RS$_1$ | RS$_0$ | Function |
|---|---|---|---|---|
| $00-$FF | 0 | 0 | 1 | Color Look-Up-Table location $00-$FF |
| XXXX-0000 | 1 | 0 | 1 | Reserved |
| XXXX-0001 | 1 | 0 | 1 | Overlay Register 1 |
| XXXX-0010 | 1 | 0 | 1 | Overlay Register 2 |
| XXXX-0011 | 1 | 0 | 1 | Overlay Register 3 |
| : | : | : | : | : |
| XXXX-1111 | 1 | 0 | 1 | Overlay Register 15 |

| V | mA |
|---|---|
| 1.000 | 26.67 |
| 0.340 | 9.05 |
| 0.286 | 7.62 |
| 0.000 | 0.00 |
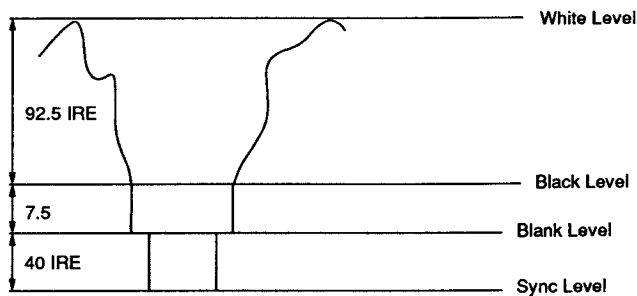


Note: 75 Ω doubly-terminated load, SELECT = $V_{CC}$. External voltage or current reference adjusted for 26.67 mA full scale output. RS-343A levels and tolerances assumed on all levels.

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**Figure 1. Composite Video Output Signals (SELECT = $V_{CC}$)**

**Table 4. Video Output Truth Table (SELECT = $V_{cc}$)**

| Description | $\overline{SYNC}$ | $\overline{BLANK}$ | $I_{out}$ (mA) | DAC Input Data |
|---|---|---|---|---|
| WHITE | 1 | 1 | 26.67 | $FF |
| DATA | 1 | 1 | data + 9.05 | data |
| DATA–SYNC | 0 | 1 | data + 1.44 | data |
| BLACK | 1 | 1 | 9.05 | $00 |
| BLACK-SYNC | 0 | 1 | 1.44 | $00 |
| BLANK | 1 | 0 | 7.62 | $xx |
| SYNC | 0 | 0 | 0 | $xx |

Note: Typical will full scale G = 26.67 mA. SELECT = $V_{cc}$. External voltage or current reference adjusted for 26.67 mA full scale output.

**Table 5. Video Output Truth Table (SELECT = GND)**

| Description | $\overline{SYNC}$ | $\overline{BLANK}$ | $I_{out}$ (mA) | DAC Input Data |
|---|---|---|---|---|
| WHITE | 1 | 1 | 26.67 | $FF |
| DATA | 1 | 1 | data + 8.05 | data |
| DATA–SYNC | 0 | 1 | data | data |
| BLACK | 1 | 1 | 8.05 | $00 |
| BLACK-SYNC | 0 | 1 | 0 | $00 |
| BLANK | 1 | 0 | 8.05 | $xx |
| SYNC | 0 | 0 | 0 | $xx |

Note: Typical will full scale G = 26.67 mA. SELECT = GND. External voltage or current reference adjusted for 26.67 mA full scale output.

| V | mA |
|---|---|
| 1.000 | 26.67 |
| 0.302 | 8.05 |
| 0.000 | 0.00 |
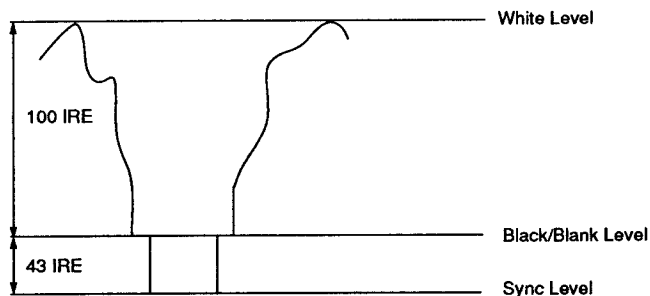


Note: 75 Ω doubly-terminated load, SELECT = GND. External voltage or current reference adjusted for 26.67 mA full scale output.

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**Figure 2. Composite Video Output Signals (SELECT = GND)**

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ........................................ –65 to +150°C
Ambient Temperature
   Under Bias ................................................. –55 to +125°C
   Junction Temperature ............................................ +175°C
Supply Voltage to Ground Potential
   Continuous ......................................................... –0.5 to 7.0 V
DC Voltage Applied to ............ GND–0.5 V to $V_{CC}$ Max+0.5 V
   Outputs for HIGH
   Output State
DC Input Voltage GND ............................. –0.3 to $V_{CC}$ +0.3 V

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
   Ambient Temperature ($T_A$) ................................ 0 to +70°C
   Supply Voltage ($V_{CC}$)
   for 80 MHz devices .................................. +4.75 to +5.25 V
   for 35, 50, 66 MHz devices ...................... +4.50 to +5.50 V
Reference Voltage ....................................... +1.14 to +1.26 V
   (Voltage Reference Configuration)
$I_{REF}$ Current ...................................................... –3 to –10 mA
   (Current Reference Configuration)
Output Load ................................................................ 37.5 Ω

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS (Over operating range)

| Parm. Num | Parm. Symbol | Parameter Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Digital Inputs** | | | | | | | |
| | $V_{IH}$ | Input High Voltage | | 2.0 | | $V_{CC}$+0.5 | V |
| | $V_{IL}$ | Input Low Voltage | | GND–0.5 | | 0.8 | V |
| | $I_{IH}$ | Input High Current | $V_{in}$=2.4 V | | | 1 | µA |
| | $I_{IL}$ | Input Low Current | $V_{in}$–0.4 V | | | –1 | µA |
| | $C_{IN}$ | Input Capacitance | f=1 MHz, $V_{in}$= 2.4 V | | | 7 | pF |
| **Digital Outputs** | | | | | | | |
| | $V_{OH}$ | Output High Voltage | $I_{OH}$ = –400 µA | 2.4 | | | V |
| | $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 3.2 mA | | | .4 | V |
| | $I_{OZ}$ | 3-State Current | | | | 50 | µA |
| | $C_{out}$ | Output Capacitance | | | | 7 | pF |
| **Analog Outputs** | | | | | | | |
| | | Resolution (each DAC) | | 6 (8) | 6 (8) | 6 (8) | Bits |
| | | Accuracy (each DAC) | | | | | |
| | $LIN_i$ | Integral Linearity Error | | | | ±1/4(1) | LSB |
| | $LIN_d$ | Differential Linearity Error | | | | ±1/4(1) | LSB |
| | | Gray Scale Error | | | | ±5 | %Gray |
| | | Monotonicity | | | Guaranteed | | |
| | | Coding | Binary | | | | Binary |
| | | Output Current | | | | | |
| | |   White Level Relative to Blank | | 17.69 | 19.05 | 20.4 | mA |
| | |   White Level Relative to Black | | 16.74 | 17.62 | 18.5 | mA |
| | |   Black Level Relative to Blank | SELECT = $V_{CC}$ | 0.95 | 1.44 | 1.9 | mA |
| | | | SELECT = GND | 0 | 5 | 50 | µA |
| | | Blank Level | | 6.29 | 7.62 | 8.96 | mA |
| | | Sync Level | | 0 | 5 | 50 | µA |
| | | LSB Size | | | | | |
| | |   Am81C478 (8/6̄=Logical one) | | | 69.1 | | µA |
| | |   Am81C471 | | | 279.68 | | µA |
| | | DAC-to-DAC Matching | | | 2 | 5 | % |
| | $R_{out}$ | Output Impedance | | | 10 | | KΩ |
| | $C_{out}$ | Output Capacitance | f=1 MHz, $I_{out}$=0 mA | | | 30 | pF |
| | $I_{VREF}$ | Voltage Reference Input Current | | | 100 | | µA |
| | PSSR | Power Supply Rejection Ratio | COMP=0.1 pF, f=1 KHz | | | 0.5 | %/%$V_{CC}$ |

**3**

## SWITCHING CHARACTERISTICS (Over operating range)

| Parm. Num. | Parm. Symbol | Parameter Description | 80 MHz Min | Typ | Max | 66 MHz Min | Typ | Max | 50 MHz Min | Typ | Max | 35 MHz Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Clock Rate | | | 80 | | | 66 | | | 50 | | | 35 | MHz |
| 1 | $t_S$ | $RS_0$–$RS_2$ Setup Time | 10 | | | 10 | | | 10 | | | 15 | | | ns |
| 2 | $t_H$ | $RS_0$–$RS_2$ Hold Time | 10 | | | 10 | | | 10 | | | 15 | | | ns |
| 3 | $t_P$ | $\overline{RD}$ Asserted to Data Bus Driven | 5 | | | 5 | | | 5 | | | 5 | | | ns |
| 4 | $t_P$ | $\overline{RD}$ Asserted to Data Valid | | | 40 | | | 40 | | | 40 | | | 40 | ns |
| 5 | $t_P$ | $\overline{RD}$ Negated to Data Bus 3-stated | | | 20 | | | 20 | | | 20 | | | 20 | ns |
| 6 | $t_S$ | Write Data Setup Time | 10 | | | 10 | | | 10 | | | 15 | | | ns |
| 7 | $t_H$ | Write Data Hold Time | 10 | | | 10 | | | 10 | | | 15 | | | ns |
| 8 | $t_W$ | $\overline{RD}$, $\overline{WR}$ Pulse Width Low | 50 | | | 50 | | | 50 | | | 50 | | | ns |
| 9 | $t_W$ | $\overline{RD}$, $\overline{WR}$ Pulse Width High | 4 X $t_{cyc}$ | | | 4 X $t_{cyc}$ | | | X $t_{cyc}$ | | | 4 X $t_{cyc}$ | | | ns |
| 10 | $t_S$ | Pixel and Overlay Setup Time | 3 | | | 3 | | | 3 | | | 4 | | | ns |
| 11 | $t_H$ | Pixel and Overlay Hold Time | 3 | | | | | | 3 | | | 4 | | | ns |
| 12 | $t_{CYC}$ | Clock Cycle Time | 12.5 | | | 15.2 | | | 20 | | | 28 | | | ns |
| 13 | $t_W$ | Clock Pulse Width High Time | 4 | | | 5 | | | 6 | | | 7 | | | ns |
| 14 | $t_W$ | Clock Pulse Width Low Time | 4 | | | 5 | | | 6 | | | 9 | | | ns |
| 15 | $t_P$ | Analog Output Delay | | | 30 | | | 30 | | | 30 | | | 30 | ns |
| 16 | $t_R$, $t_F$ | Analog Output Rise/Fall Time (Note 1) | | | 3 | | | 3 | | | 3 | | | 3 | ns |
| 17 | $t_S$ | Analog Output Settling Time (Note 1) | | | 13 | | | 16 | | | 20 | | | 28 | ns |
| | | Clock and Data Feedthrough | –30 | | | –30 | | | –30 | | | –30 | | | dB |
| | | Glitch Impulse (Note 2) | 75 | | | 75 | | | 75 | | | 75 | | | pV–sec |
| | | DAC to DAC Crosstalk | –23 | | | –23 | | | –23 | | | –23 | | | dB |
| | | Analog Output Skew | | | 2 | | | 2 | | | 2 | | | 2 | ns |
| | | Pipeline Delay | 4 | | | 4 | | | 4 | | | 4 | | | clocks |
| $I_{CC}$ | | $V_{CC}$ Supply Current (Note 3) | 160 | 200 | | 160 | 200 | | 160 | 200 | | 160 | 200 | | mA |

**Notes:**
1. Clock and data feedthrough are not included
2. Included clock and data feedthrough, –3 dB bandwidth = 2 x clock frequency
3. Measured at maximum $f_{CLK}$;
   $I_{CC}$(Max.): $V_{CC}$ = 5.25 V, $T_A$ = 0°C
   $I_{CC}$(Typ.): $V_{CC}$ = 5.0 V, $T_A$ + 25°C

**Test Conditions:**
TTL Input Level: 0 to 3 V with $t_R$, $t_F$ (10–90%) ≤ 3 ns
$R_{set}$ = 148 Ω (Am81C478); $R_{set}$ = 147 Ω (Am81C471)
$V_{ref}$ = 1.235 V, Select = $V_{CC}$, 8/6 = Logical '1'
Analog Output Load ≤ 10 pF, $D_0$–$D_7$ Output Load ≤ 50 pF
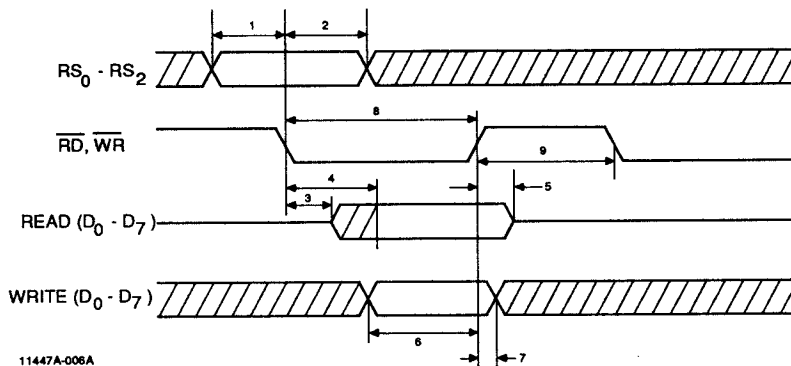
**MPU  Read / Write Timing**

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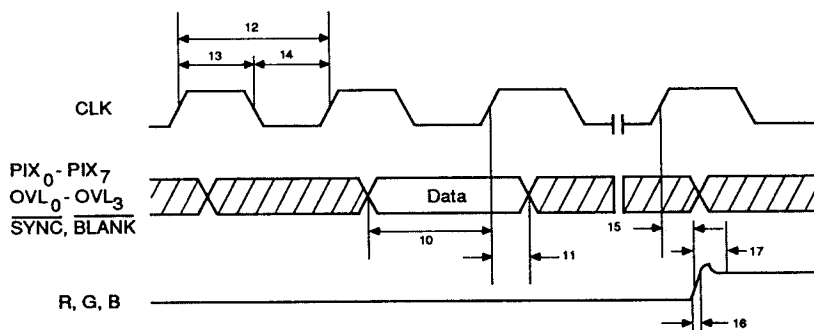


Note 1: Output delay measured from the 50% point of the rising edge of CLK to the 50 % point of the full scale transition

Note 2: Settling time measured from the 50% point of the full scale transition to the output remaining within ± LSB (Am81C478) or ± 1/4 LSB (Am81C471)

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition

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**Video Input / Output Timing**
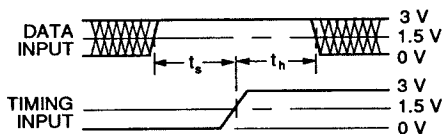


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Notes:  1.  Diagram shown for HIGH data only.  Output transition may be opposite sense.
2.  Cross-hatched areas are don't care condition.

**Switching Test Waveform**

# APPENDIX A: APPLICATION NOTE FOR THE AM81C471/478

The design of a system using the Am81C471/478 should be guided by considerations similar to those used for designing precision high-speed mixed analog and digital systems. The following rules and examples are given for orientation purposes. Users may choose to design circuits, which may differ considerably from the examples given here.

The Am81C471/478 can be configured in either current or voltage reference modes. The voltage reference scheme, as shown in Figure A1, is preferred over the current source scheme because of the following features: superior power supply rejection, temperature compensation, lower power, fewer components and overall simplicity of design. The current reference mode, as shown in Figure A2, requires more components to provide adequate temperature compensation, and power supply rejection.

Power pins should be decoupled from the power lines in the rest of the system. The Am81C471/478 should have its own power plane; this plane should provide power to all its power pins and voltage/current reference circuits. This plane should be connected to the main power plane by a wire running through ferrite beads as shown in Figures A1 and A2.

If further noise reduction is required on the analog outputs then a separate analog power plane and digital power plane should be used and connected to pins (21,22) and (4,20) respectively. These two power planes should be connected to the main power plane by wires running through ferrite beads. The analog plane should not be crossed by any digital signal. Only one ground plane should be used, directly connected to the rest of the system. Tantalum capacitors, in parallel with a 0.1 µF ceramic capacitor, should be placed between each side of the ferrite beads and the ground plane. If too much ripple exists on the lines, the use of a dedicated linear regulator is recommended.

The COMP pin should be decoupled from the power pins and the rest of the system. A 0.1 µF ceramic capacitor should be connected in parallel between this pin and the analog power pins (21,22).

Digital lines accessible by the MPU interface should be kept far from pixel data lines. Pixel clock lines should be kept far from all other digital inputs. Analog outputs should be kept far from any other input. No digital line should run under the analog plane.

Connection to the monitor should be done through a doubly-terminated 75 $\Omega$ coaxial cable. To minimize reflections, terminating resistors on the color palette side should be placed as close as possible to the R, G, and B outputs.

The signals produced by the Am81C471/478 are all positive currents, which when passing through the terminating resistors produce positive voltages. Since most monitors are AC-coupled, DC restoration with the proper DC level is done inside the monitor. If a negative-going sync (–0.286V) is required, DC level shifting can be done outside the palette, prior to entering the transmission cable. The circuit that produces this level shifting is shown in Figure A3. This circuit shows two resistors, $R_1$ and $R_2$, as the termination at the transmitting side. $R_1$ is connected between R (G, or B) outputs and ground, while $R_2$, is connected between R (G, or B) outputs and a voltage source more negative than –0.572V. $R_1$ and $R_2$ are such that in parallel they equal 75 $\Omega$, while their ratio is such that the voltage drop caused by the negative voltage source across $R_1$ is 0.572 V. The relationship is described by the following formulae:

$$R_1 \parallel R_2 = 75\,\Omega\;;\;R_1 = V \cdot 75/(V+0.572)\;;\;R_2 = V \cdot 75/(-0.572)$$

Figure A4 shows a VGA system in which a VGA graphics controller is paired with Am81C471/478 in a typical PC board design.

The Am81C471 has 6-bit µP interface which is compatible with existing VGA software. To accomodate 8-bit software the Am81C478 can be used. By driving the $8/\overline{6}$ input pin from the µP interface the software can automatically change the DAC resolution (bits per channel) according to its own requirements.
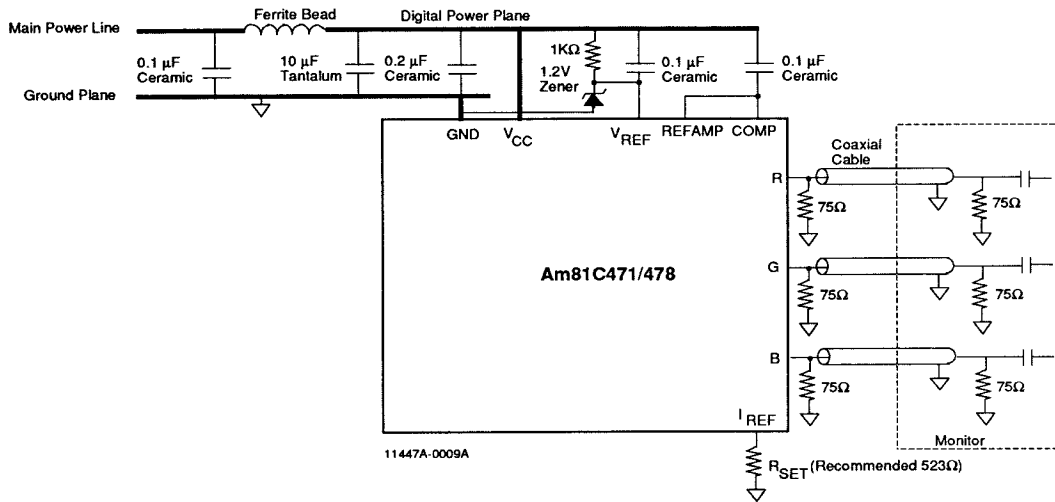
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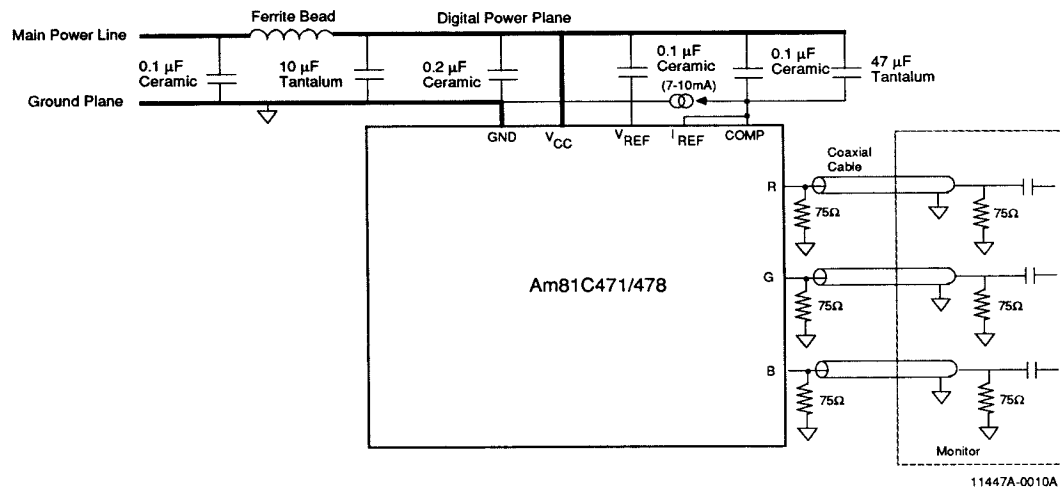**Figure A1. Am81C471/478 Voltage Reference Connection Diagram (AC Coupling of the Monitor)**



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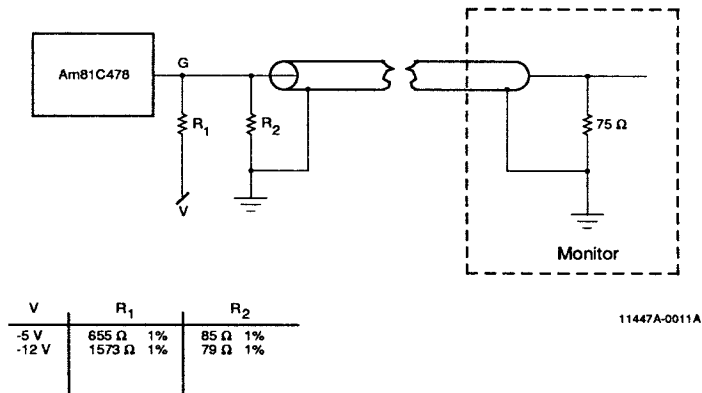**Figure A2. Am81C471/478 Current Reference connection Diagram (AC Coupling of the Monitor)**

| V | $R_1$ | | $R_2$ | |
|---|---|---|---|---|
| -5 V | 655 Ω | 1% | 85 Ω | 1% |
| -12 V | 1573 Ω | 1% | 79 Ω | 1% |

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**Figure A3. DC-Level Shifting Using Two Resistors in Parallel**
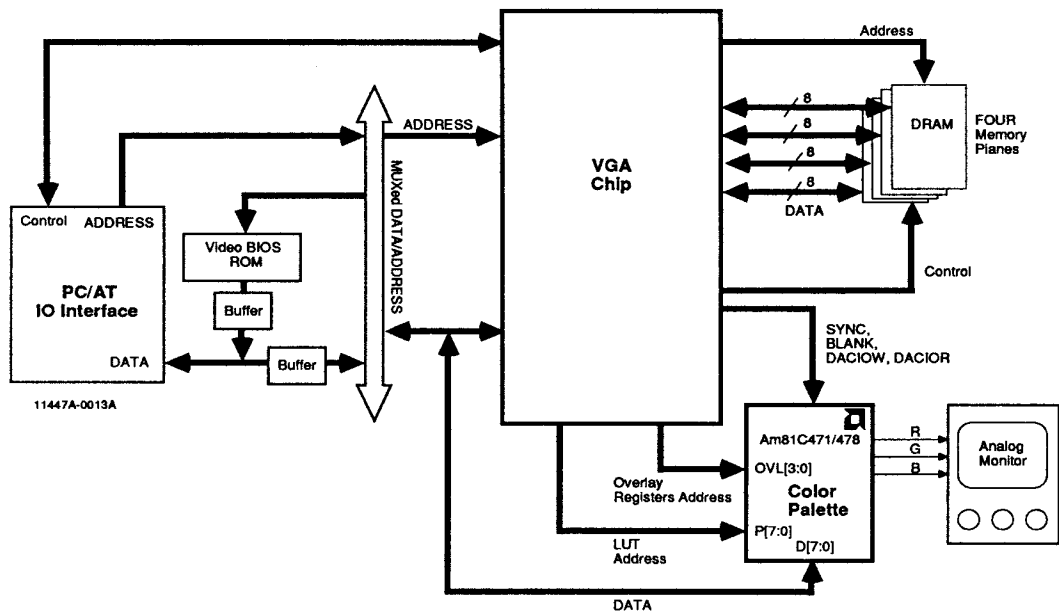


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**Figure A4. Application Example: VGA system using a VGA chip and an Am81C471/478**