Signetics

54164, 54LS164
Shift Registers

8-Bit Serial-In Parallel-Out Shift Registers

Product Specification

Military Logic Products

FEATURES

- **Gated serial data inputs**
- **Typical shift frequency of 36MHz**
- **Asynchronous Master Reset**
- **Fully buffered clock and data inputs**

DESCRIPTION

The 54164 and 54LS164 are 8-bit edge-triggered shift registers with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (D_{sa} or D_{sb}); either input can be used as an Active-High enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied High.

Data shifts one place to the right on each Low-to-High transition of the Clock (CP) input, and enters into Q_0 the logical AND of the two Data inputs ($D_{sa} \cdot D_{sb}$) that existed one setup time before the rising clock edge. A Low-level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

ORDERING INFORMATION

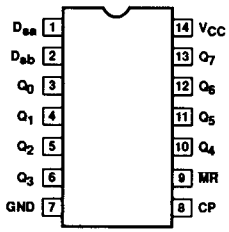
DESCRIPTION	ORDER CODE
Ceramic DIP	54LS164/BCA, 54164/BCA
Ceramic Flat Pack	54LS164/BDA
Ceramic LLCC	54LS164/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54	54LS
All	Inputs	1UL	1LSUL
All	Outputs	5UL	10LSUL

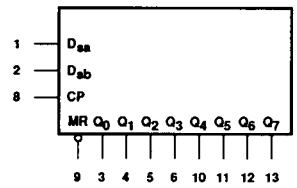
NOTE: Where a 54 Unit Load (UL) is understood to be 40µA I_{IH} and -1.6mA I_{IL}, and a 54LS Unit Load (LSUL) is 20µA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

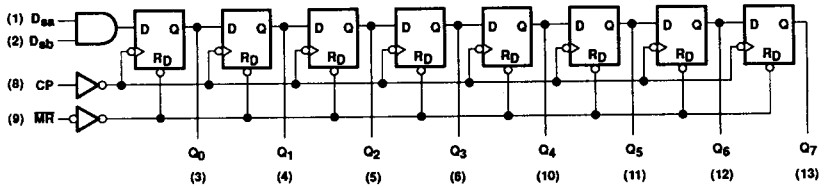
LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

For LLCC pin assignments, see JEDEC Standard No. 2

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS		
	MR	CP	D_{sa}	D_{sb}	Q_0	Q_1 —	Q_7
Reset	L	X	X	X	L	L —	L
Shift	H	↑	l	l	L	q_0 —	q_6
	H	↑	l	h	L	q_0 —	q_6
	H	↑	h	l	L	q_0 —	q_6
	H	↑	h	h	H	q_0 —	q_6

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High Clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High Clock transition
q = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the Low-to-High Clock transition
X = Don't care
↑ = Low-to-High Clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54164	54LS164	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +5.5	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

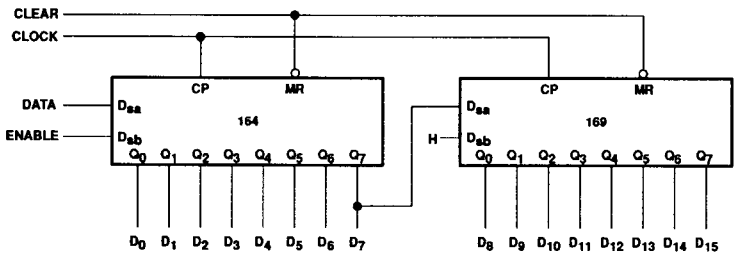
RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54164			54LS164			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			+0.8			+0.7	V
I_{IK}	Input clamp current			-12			-18	mA
I_{OH}	High-level output current			-400			-400	µA
I_{OL}	Low-level output current			8			4	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		54164			54LS164			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.2	0.4		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5			-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V			1.0				mA
			V_I = 7.0V						0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max	V_I = 2.4V			40				µA
			V_I = 2.7V						20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V				-1.6			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-10		-27.5	-20		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			37	54		16	27	mA

APPLICATION DIAGRAM



The '164 can be cascaded to form synchronous shift registers of longer length. Here, two devices are combined to form a 16-bit shift register.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	54164		54LS164		UNIT
			C_L = 15pF		C_L = 15pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum shift frequency	Waveform 1	25		25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		27 32		27 32	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 2		36		36	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54164		54LS164		UNIT
			Min	Max	Min	Max	
t_W	Clock pulse width	Waveform 1	20		20		ns
t_W	$\overline{MR}$ pulse width	Waveform 2	20		20		ns
t_S	Setup time data to clock	Waveform 3	15		15		ns
t_H	Hold time data to clock	Waveform 3	5.0		5.0		ns
t_{REC}	$\overline{MR}$ clock recovery time	Waveform 2	30		30		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54164		54LS164		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum shift frequency	Waveform 1	22		22		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		34 41		31 36	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 2		46		40	ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	54164		54LS164		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum shift frequency	Waveform 1	18		20		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		31 48		40 47	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 2		55		52	ns

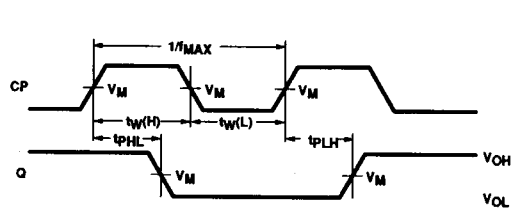
AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	54164		54LS164		UNIT
			Min	Max	Min	Max	
t_W	Clock pulse width	Waveform 1	30		20		ns
t_W	$\overline{MR}$ pulse width	Waveform 2	50		25		ns
t_S	Setup time data to clock	Waveform 3	15		20		ns
t_H	Hold time data to clock	Waveform 3	10		10		ns
t_{REC}	$\overline{MR}$ clock recovery time	Waveform 2	30		30		ns

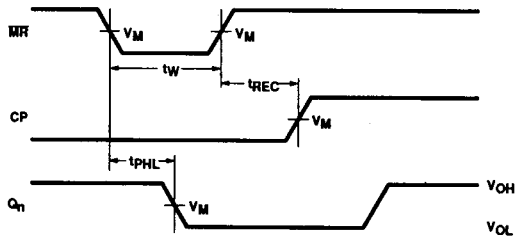
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with the Serial inputs grounded, the Clock input at 2.4V, and a momentary ground, then ≥4.0V applied to Master Reset, and all outputs open.
5. These parameters are guaranteed, but not tested.

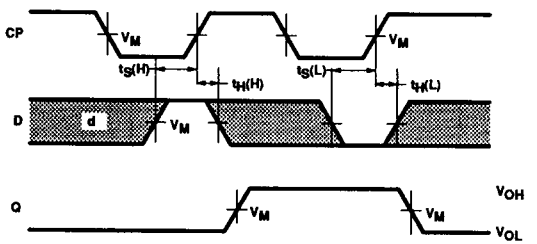
AC WAVEFORMS



Waveform 1. Clock to Output Delays and Clock Pulse Width



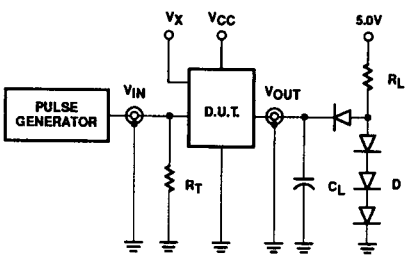
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



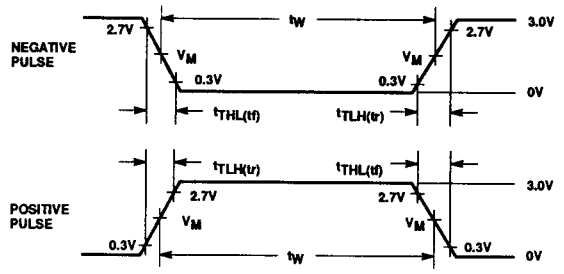
Waveform 3. Data Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V for 54; V_M = 1.3V for 54LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54XXX	400Ω	1.5V	1MHz	500ns	≤7ns	≤7ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per Function Table.