

5 Gbit/s ATM Switch Fabric Element

FEATURES

SWITCHING ALGORITHM

- Supports blocking resolution in the switch fabric.
- Guarantees a lower bound on switch performance using a patented randomization algorithm called Evil Twin Switching™.
- Determines routes using specified bits in the header (self-routing switch fabric) for unicast traffic.
- Determines output groupings using a lookup table for multicast traffic.
- Allows output ports to be combined in groups of 1, 2, 4, 8, 16, or 32 for unicast traffic.
- Allows output ports to be combined in groups of 1, 2, or 4 for multicast traffic.

MULTICAST SUPPORT

- Supports optimal tree-based multicast replication in the switch fabric.

- Supports 128 internal multicast groups, expandable to 256 K with external SRAM.
- Provides 64 internal cell buffers for multicast cells.

DIAGNOSTIC/ROBUSTNESS FEATURES

- Checks the header parity.
- Counts tagged cells.
- Checks for connectivity and stuck-at faults on all switch fabric interconnects.

I/O FEATURES

- Provides 32 switch fabric interfaces with integrated phase aligner clock recovery circuitry.
- Provides a Start-Of-Cell (SOC) output per four switch element interfaces.
- Provides an external 16-bit Synchronous SRAM (SSRAM) interface for multicast group expansion.

- Provides a demultiplexed address/data CPU interface.
- Provides an IEEE 1149.1 (JTAG) boundary scan test bus.

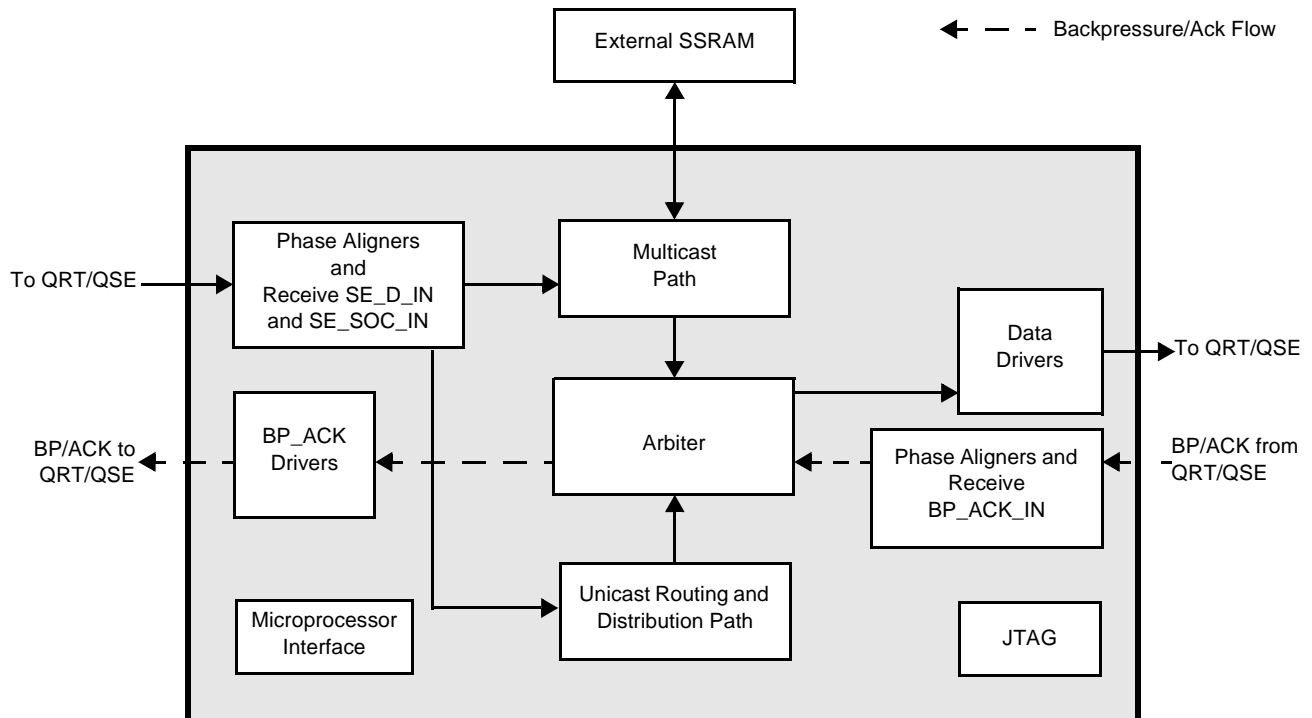
PHYSICAL CHARACTERISTICS

- 3.3 V supply voltage.
- 5 V tolerant inputs.
- 596-pin Enhanced Plastic Ball Grid Array (EPBGA) package.
- Operates from a single 66 MHz clock.

APPLICATIONS

- A 5 Gbit/s Switch
- A 10 Gbit/s Switch
- A 5 Gbit/s-to-20 Gbit/s Scalable Switch Architecture
- A 2.4 Gbit/s-to-80 Gbit/s Scalable Switch Architecture
- A 5 Gbit/s-to-320 Gbit/s Scalable Switch Architecture

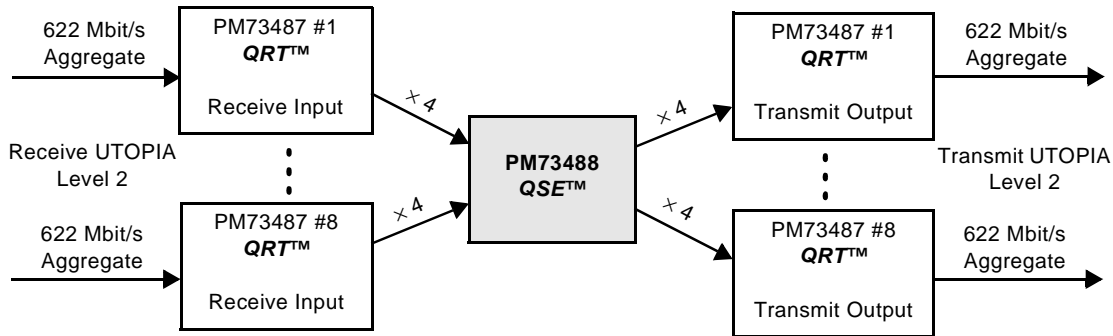
BLOCK DIAGRAM



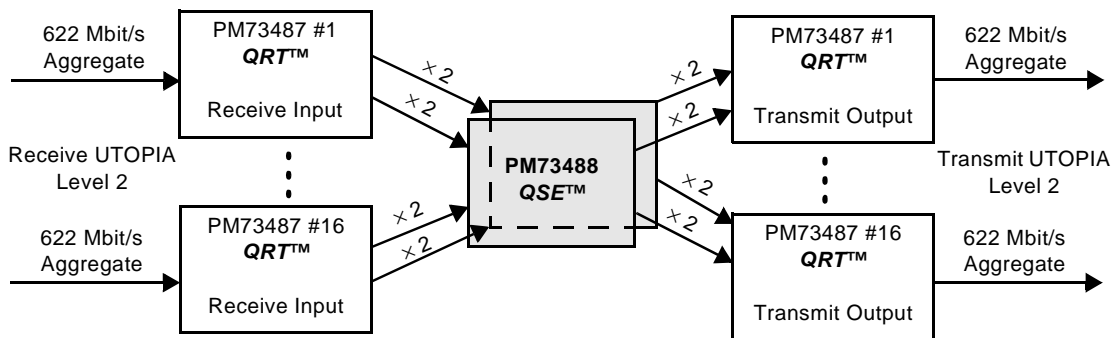
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TYPICAL APPLICATIONS

5 Gbit/s ATM SWITCH USING 8 QRTs AND 1 QSE



10 Gbit/s ATM SWITCH USING 16 QRTs AND 2 QSEs



64 x 64 SWITCH APPLICATION (10 Gbit/s)

