I C T INC

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T-46-19-07

PEEL™ 22CV10Z "Zero Power" CMOS Programmable Electrically Erasable Logic Device

Features

- **Advanced CMOS EEPROM Technology**
- **High Performance and Ultra-Low Power**
  - — t_{PD} = 25ns, fmax=33.3MHz
  - — I_{CC} = 5mA at 1MHz
  - — I_{CC} = 200µA at "Zero-Power" standby
- **EE Reprogrammability**
  - — Low-risk reprogrammable inventory
  - — Superior programming and functional yield
  - — Erases and programs in seconds
- **Development and Programming Support**
  - — Third-party software and programmers
  - — ICT PEEL Development System and software.
- **Architectural Flexibility**
  - — 132 product term x 44 input AND array
  - — Up to 22 inputs and 10 outputs
  - — Variable product term distribution (8 to 16 per output) for greater logic flexibility
  - — Independently programmable 12-configuration I/O macrocells
  - — Synchronous preset, asynchronous clear
  - — Independently programmable output enables
- **Application Versatility**
  - — Ideal for power-sensitive systems
  - — Replaces random SSI/MSI logic
  - — Superset compatible with the bipolar AmPAL22V10 and CMOS PALC22V10

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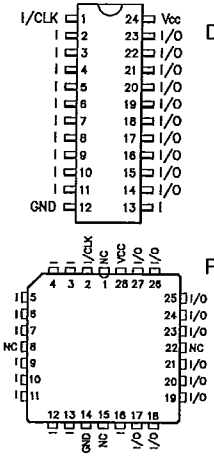
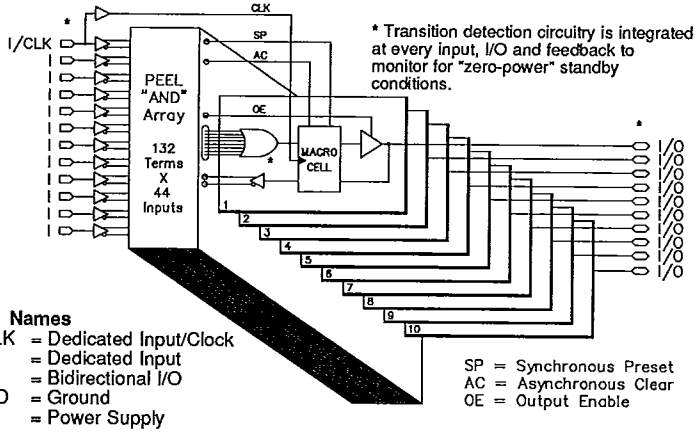
General Description

The CMOS PEEL22CV10Z is a Programmable Electrically Erasable Logic Device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to early-generation programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL22CV10Z rivals speed parameters of comparable bipolar PLDs while providing a dramatic reduction in active power consumption. A user-programmable "zero-power" standby mode further reduces power consumption, making the PEEL22CV10Z ideal for power sensitive applications such as hand held meters, portable communication equipment and laptop computer/peripherals. EE reprogrammability allows cost effective plastic packaging, low-risk inventories, reduced development and retrofit costs, and enhanced testability to ensure 100% field programmability and function. The PEEL 22CV10Z's flexible architecture provides function compatibility with the bipolar AmPAL22V10 and CMOS PALC22V10, plus eight additional macrocell configurations (a total of twelve) for increased design flexibility. The PEEL22CV10Z can be used to replace random SSI/MSI logic circuitry or 24-pin bipolar PAL devices, or implement user-customized sequential and combinatorial functions such as counters, shift registers, state machines, address decoders, multiplexers, etc. Development and programming support for the PEEL22CV10Z is provided by ICT and third-party manufacturers.

Pin Configuration (Figure1)



Block Diagram (Figure 2)



* Transition detection circuitry is integrated at every input, I/O and feedback to monitor for "zero-power" standby conditions.

Pin Names

I/CLK	= Dedicated Input/Clock
I	= Dedicated Input
I/O	= Bidirectional I/O
GND	= Ground
Vcc	= Power Supply

SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable

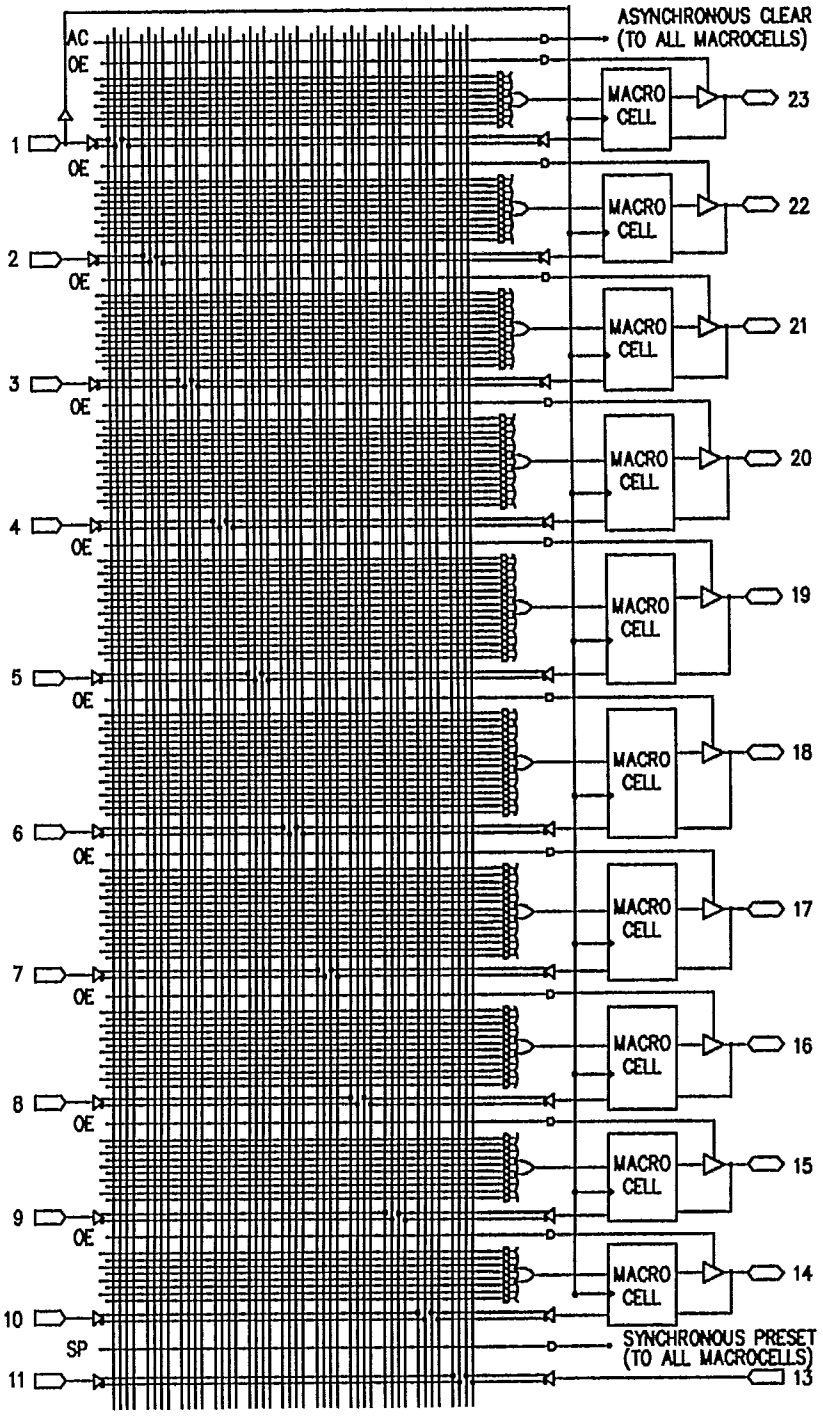


Figure 3. PEEL22CV10Z Logic Array Diagram

Function Description

The PEEL22CV10Z implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL22CV10Z architecture is illustrated in the block diagram of figure 2. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure, the PEEL22CV10Z can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 12 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable AND array of the PEEL22CV10Z (shown in figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

- 24 input lines carry the true and complement of the signals applied to the 12 input pins
- 20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

132 product terms:

- 120 product terms (arranged in 2 groups of 8, 10, 12,14, and 16) used to form logical sums
- 10 output enable terms (one for each I/O)
- 1 global synchronous preset term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the true and compliment of an input signal will always be FALSE, and thus will not effect the OR function that it drives. When all the connections on a product term are opened, a don't care state exists and that term will always be TRUE. When programming the PEEL22CV10Z, the device programmer first performs a bulk erase to instantly remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array.

Variable Product Term Distribution

The PEEL22CV10Z provides 120 product terms to drive the ten OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14, and 16 to form logical sums (see figure 3). This distribution allows optimum use of device resources.

Programmable I/O Macrocell

The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL22CV10Z to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the four EEPROM bits (A,B,C,D) controlling these multiplexers. These bits determine: output polarity; output type (registered or non-registered); and input/feedback path (bi-directional I/O, combinatorial feedback, or register feedback). Table 1 shows the bit settings for each of the twelve macrocell configurations.

Equivalent circuits for the twelve macrocell configurations are illustrated in figure 5. In addition to emulating the four PAL-type output structures (configurations 3, 4, 9, and 10) the macrocell provides eight additional configurations.

Output Type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

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Output Polarity

Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state. Under the control of the output enable term, the I/O pin can function as a dedicated input, output, or a bi-directional I/O.

Input/Feedback Select

The PEEL22CV10Z macrocell also provides control over the feedback path. The input/feedback signal associated with each I/O macrocell may be obtained from three different locations: from the I/O pin (bi-directional I/O); directly from the Q output of the flip-flop (registered feedback); or directly from the OR gate (combinatorial feedback).

Bi-directional I/O

The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with bi-directional I/O.)

Combinatorial Feedback

The signal-select multiplexer gives the macrocell the ability to feedback the output directly from the OR gate, regardless of whether the output function is registered or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7, and 8 in figure 5.)

Registered Feedback

Feedback also can be taken from the register, regardless of whether the output function is registered or combinatorial. When implementing configurations 11 and 12, the register can be used for internal latching of data while leaving the external output free for combinatorial functions.

"Zero-Power" Mode

The CMOS PEEL22CV10Z features a user-selectable "Zero-Power" standby mode for ultra-low power consumption. When the "Zero-Power" mode is selected, transition-detection circuitry monitors the inputs, I/O (including CLK) and feedback. If the inputs do not change for a period of time equal to approximately [t_{PD} X 2], the outputs are latched in their current state and the device automatically powers-down. When the next transition is detected at the inputs, the device will "wake up" for active operation until the inputs stop switching long enough to trigger the next power-down. When powering up, an additional delay is added to the first output transition. (See A.C. electrical characteristics, note 12, for details.)

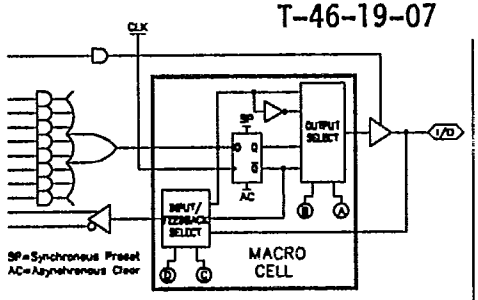

Figure 4. 22CV10Z Macro Cell Block Diagram

The "Zero-power" mode is best used for combinatorial applications since sequential functions will be powered-up with every edge of the clock. Significant power savings can still be realized, however, when running the clock at a modest rate. Figure 6 shows the typical Icc vs Input transition frequency for the 22CV10Z when the zero-power mode is programmed.

The Z-bit may be set either in the design file or when programming (depending on the programmer used). For APEEL logic assembler design files, the zero-power mode is selected using the ZERO_POWER declaration. With other logic compilers, a set fuse (to "0") command for cell location 5848 can be used.

Design Security

The PEEL22CV10Z provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

Signature Word

The signature word feature allows a 24-bit code to be programmed into the PEEL22CV10Z. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

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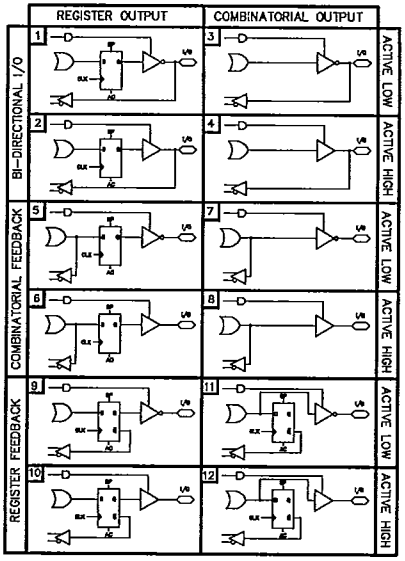

Figure 5. Equivalent Circuits for the Twelve Configurations of the PEEL22CV10Z I/0 Macrocell.

Configuration #	A	B	C	D	Input/Feedback Select	Output Select	
1	0	0	1	0	Bi-Directional I/O	Register	Active Low
2	1	0	1	0	"	"	Active High
3	0	1	0	0	"	Combinatorial	Active Low
4	1	1	0	0	"	"	Active High
5	0	0	1	1	Combinatorial Feedback	Register	Active Low
6	1	0	1	1	"	"	Active High
7	0	1	1	1	"	Combinatorial	Active Low
8	1	1	1	1	"	"	Active High
9	0	0	0	0	Register Feedback	Register	Active Low
10	1	0	0	0	"	"	Active High
11	0	1	1	0	"	Combinatorial	Active Low
12	1	1	1	0	"	"	Active High

Table 1. PEEL22CV10Z Macrocell Configuration Bits

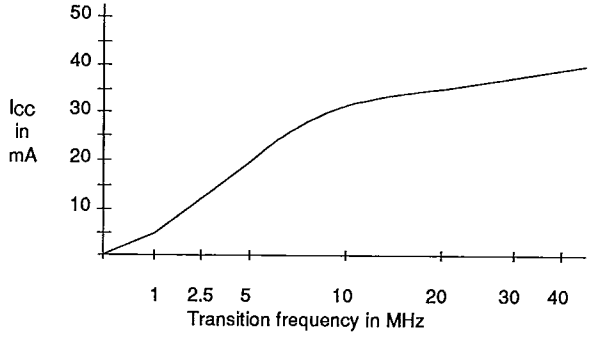

Figure 6. Typical Icc vs Input or Clock transition frequency for 22CV10Z (zero-power mode)

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [3]	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	Ambient Temperature	Commercial [2]	0	70	°C
T_R	Clock Rise Time	See note 4		250	nS
T_F	Clock Fall Time	See note 4		250	nS
T_{RVCC}	VCC Rise Time	See note 4		250	mS

D.C. Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = −4.0mA	2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 8mA		0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		− 0.3	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	Output Short Circuit Current	V_{CC}=5V, V_O = 0.5V [10], T_A = 25°C	− 30	− 90	mA
I_{CC}	V_{CC} Current (Applicable when "Zero-Power" not in use)†	V_{IN} = 0V or 3V [5,11] f = 25MHz All outputs disabled		67	mA
I_{CCSZ}	V_{CC} Current, "Zero-power" standby	V_{IN} = V_{CC} or		200	µA
C_{IN} [8]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT} [8]	Output Capacitance			12	pF

† See figure 6 for typical ICC over frequency using "Zero-Power" mode.

A.C. Electrical Characteristics

Over the Operating Range [9,13]

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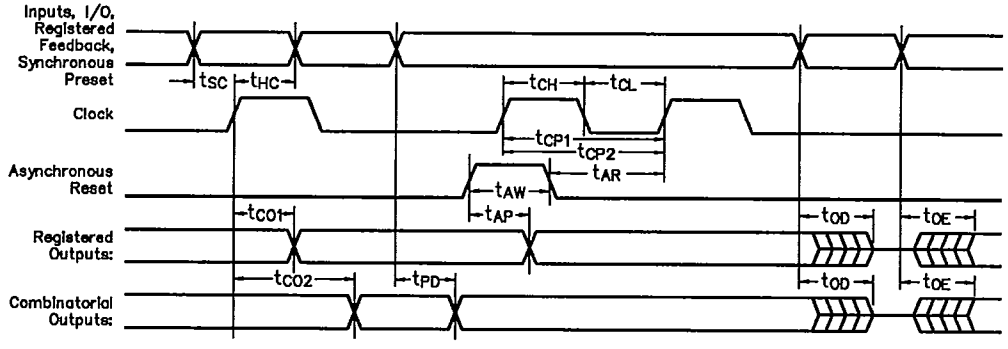
Symbol	Parameter	22CV10Z-25		22CV10Z-35		Unit
		Min	Max	Min	Max	
t_{PD}	Input[6] or feedback to non-registered output [12]		25		35	ns
t_{OE}	Input [6] to output enable [7, 12]		25		30	ns
t_{OD}	Input [6] to output disable [7, 12]		25		30	ns
t_{CO1}	Clock to output		15		20	ns
t_{CO2}	Clock to combinatorial output delay via internal registered feedback		35		45	ns
t_{SC}	Input [6] or feedback setup to clock [12]	15		30		ns
t_{HC}	Input [6] hold after clock	0		0		ns
t_{CL},t_{CH}	Clock width - clock low time, clock high time [4]	13		15		ns
t_{CP1}	Minimum clock period (register feedback to registered output via internal path)	27		45		ns
f_{max1}	Maximum clock frequency ($1/t_{CP1}$)	37		22.2		MHz
t_{CP2}	Minimum clock period ($t_{SC} + t_{CO1}$) [12]	30		50		ns
f_{max2}	Maximum clock frequency ($1/t_{CP2}$)	33.3		20		MHz
t_{AW}	Asynchronous Reset pulse width [12]	25		25		ns
t_{AP}	Input [6] to Asynchronous Reset [12]		25		35	ns
t_{AR}	Asynchronous Reset recovery time		25		35	ns
t_{RESET}	Power-on reset time for registers in clear state [4]		5		5	µs

Switching Waveforms



1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20nS.
2. Contact ICT for other operating ranges (Industrial, Mil-temp)
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
5. I/O pins open (no load).
6. "Input" refers to an Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OL} + 0.1V$. $V_{REF} = V_L$ see test loads at the end of this section.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified) and specified test loads (figure 6)
10. One output at a time for a duration of less than 1 second.
11. I_{CC} for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
12. When leaving the zero-power standby state the first signal transition must add an additional delay of 10ns for these parameters.
13. PEEL test loads are specified at the end of this section.