3.3V SDRAM Modules HYS64V32220GD(L)

256MB PC100/PC133 144 pin SO-DIMM SDRAM Modules

Datasheet

- 144 Pin Eight Byte Small Outline Dual-In-Line Synchronous DRAM Modules for notebook applications
- Two bank 32M x 64 (256 MByte) non-parity module organisation
- Performance:

		-7.5	-8	
		PC133 3-3-3	PC100 2-2-2	Units
f_{CK}	Clock frequency (max.)	133	100	MHz
t_{AC}	Clock access time	5.4	6	ns

- Single +3.3V(± 0.3V) power supply
- Programmable $\overline{CAS}$ Latency, Burst Length and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs are LVTTL compatible
- Serial Presence Detect with E^2PROM
- Eight 256Mbit SDRAM components in TSOP54 packages with 16M x 16 organisation in two memory banks
- 8192 refresh cycles every 64 ms
- Standard and Low-Power “L” versions
- Gold contact pad, JEDEC MO-190 outline dimensions
- This module family is fully compliant with the latest INTEL SO-DIMM layout and electrical specifications
- The -7.5 (PC133-333) module version is fully backward compatible to PC100-222 operation
- ***Importante Notice***:
  This SO-DIMM module is based on 256Mbit SDRAM technology and can be used in applications only, where 256Mbit addressing is supported.

This INFINEON modules are industry standard 144 pin 8-byte Synchronous DRAM (SDRAM) Small Outline Dual In-line Memory Modules (SO-DIMM) which are organised as x64 high speed memory arrays designed for use in non-parity applications. These SO-DIMMs use 256Mbit SDRAMs in TSOPII packages. Decoupling capacitors are mounted on the board.

The DIMMs use serial presence detects implemented via a serial E^2PROM using the two pin I^2C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All INFINEON 144-pin SO-DIMMs provide a high performance, flexible 8-byte interface in a 67,6 mm long footprint.

Product Spectrum:

		Speed	SDRAMs used	RowAddr.	Bank Select	Column Addr.	Refresh Period
32M x 64	HYS64V32220GD-7.5-C2	PC133-333	8 16Mx16	13	BA0, BA1	9	8k 7,8 µs
	HYS64V32220GD-8-C2	PC100-222					
	HYS64V32220GDL-7.5-C2	PC133-333					
	HYS64V32220GDL-8-C2	PC100-222					

Note: All partnumbers end with a place code, designating the die revision. Example: HYS64V32220GD-8-C2, indicating Rev.C2 dies are used for SDRAM components.

Card Dimensions:

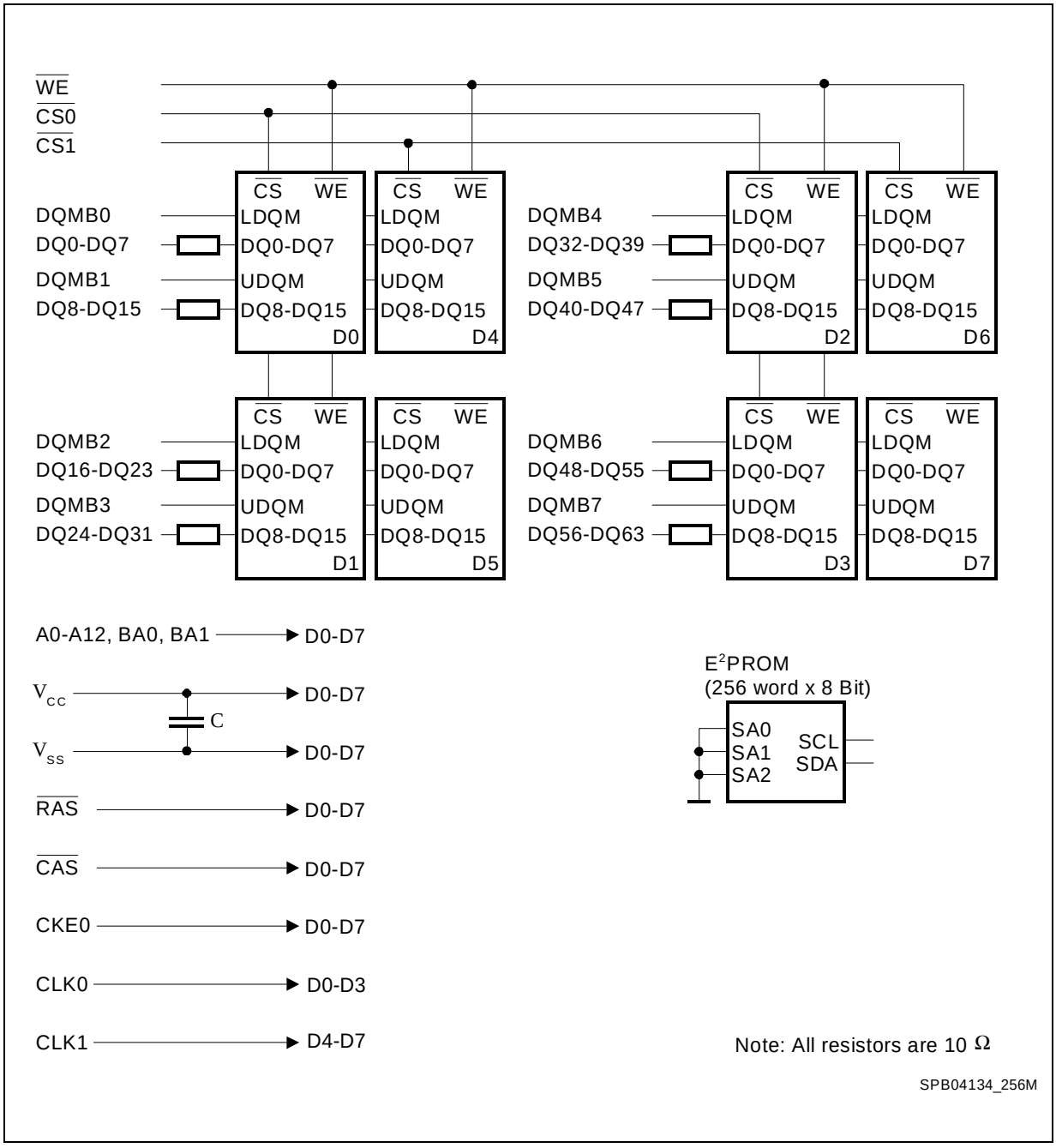
Organisation	PCB-Board	L x H x T [mm]
32M x 64	INTEL Rev. 1.0/1.2	67.60 x 31.75 x 3.80

Pin Names

A0-A11	Address Inputs	DQMB0 -DQMB7	Data Mask
BA0,BA1	Bank Selects	$\overline{CS0}$, $\overline{CS1}$	Chip Select
DQ0 - DQ63	Data Input/Output	Vcc	Power (+3.3 Volt)
$\overline{RAS}$	Row Address Strobe	Vss	Ground
$\overline{CAS}$	Column Address Strobe	SCL	Clock for Presence Detect
$\overline{WE}$	Read / Write Input	SDA	Serial Data Out for Presence Detect
$\overline{CKE0}$, $\overline{CKE1}$	Clock Enable	N.C.	No Connection
CLK0, CLK1	Clock Input		

Pin Configuration

PIN #	Front Side	PIN #	Back Side		PIN #	Front Side	PIN #	Back Side
1	VSS	2	VSS		73	NC	74	CLK1
3	DQ0	4	DQ32		75	Vss	76	Vss
5	DQ1	6	DQ33		77	NC	78	NC
7	DQ2	8	DQ34		79	NC	80	NC
9	DQ3	10	DQ35		81	Vcc	82	Vcc
11	VCC	12	Vcc		83	DQ16	84	DQ48
13	DQ4	14	DQ36		85	DQ17	86	DQ49
15	DQ5	16	DQ37		87	DQ18	88	DQ50
17	DQ6	18	DQ38		89	DQ19	90	DQ51
19	DQ7	20	DQ39		91	Vss	92	Vss
21	Vss	22	Vss		93	DQ20	94	DQ52
23	DQMB0	24	DQMB4		95	DQ21	96	DQ53
25	DQMB1	26	DQMB5		97	DQ22	98	DQ54
27	Vcc	28	Vcc		99	DQ23	100	DQ55
29	A0	30	A3		101	Vcc	102	Vcc
31	A1	32	A4		103	A6	104	A7
33	A2	34	A5		105	A8	106	BA0
35	Vss	36	Vss		107	Vss	108	Vss
37	DQ8	38	DQ40		109	A9	110	BA1
39	DQ9	40	DQ41		111	A10	112	A11
41	DQ10	42	DQ42		113	Vcc	114	Vcc
43	DQ11	44	DQ43		115	DQMB2	116	DQMB6
45	Vcc	46	Vcc		117	DQMB3	118	DQMB7
47	DQ12	48	DQ44		119	Vss	120	Vss
49	DQ13	50	DQ45		121	DQ24	122	DQ56
51	DQ14	52	DQ46		123	DQ25	124	DQ57
53	DQ15	54	DQ47		125	DQ26	126	DQ58
55	Vss	56	Vss		127	DQ27	128	DQ59
57	NC	58	NC		129	Vcc	130	Vcc
59	NC	60	NC		131	DQ28	132	DQ60
61	CLK0	62	CKE0		133	DQ29	134	DQ61
63	Vcc	64	Vcc		135	DQ30	136	DQ62
65	$\overline{RAS}$	66	$\overline{CAS}$		137	DQ31	138	DQ63
67	$\overline{WE}$	68	$\overline{CKE1}$		139	Vss	140	Vss
69	$\overline{CS0}$	70	A12		141	SDA	142	SCL
71	$\overline{CS1}$	72	N.C		143	Vcc	144	Vcc



Block Diagram for two bank 32M x 64 SDRAM DIMM - Module

DC Characteristics

T_A = 0 to 70 ×C; V_{SS} = 0 V; V_{DD},V_{DDQ} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input high voltage	V_{IH}	2.0	Vcc+0.3	V
Input low voltage	V_{IL}	– 0.5	0.8	V
Output high voltage (I_{OUT} = – 4.0 mA)	V_{OH}	2.4	–	V
Output low voltage (I_{OUT} = 4.0 mA)	V_{OL}	–	0.4	V
Input leakage current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	– 20	20	mA
Output leakage current (DQ is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	– 20	20	mA

Capacitance

T_A = 0 to 70 ×C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values	Unit
		32M x 64 max.	
Input capacitance (A0 to A11, BA0, BA1)	C_{I1}	52	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE0)	C_{I2}	46	pF
Input Capacitance (CLK0, CLK1)	C_{I3}	35	pF
Input capacitance (CS0)	C_{I4}	30	pF
Input capacitance (DQMB0-DQMB7)	C_{I5}	15	pF
Input / Output capacitance (DQ0-DQ63)	C_{IO}	18	pF
Input Capacitance (SCL,SA0-2)	C_{sc}	8	pF
Input/Output Capacitance	C_{sd}	10	pF

Operating Currents per memory bank (T_A = 0 to 70°C, Vdd = 3.3V ± 0.3V

(Recommended Operating Conditions unless otherwise noted)

Parameter & Test Condition		Symb.	-7.5	-8		Note
OPERATING CURRENT trc=trcmin., All banks operated in random access, all banks operated in ping-pong manner		ICC1	920	680	mA	1, 2
PRECHARGE STANDBY CURRENT in Power Down Mode $\overline{CS}$ =VIH (min.), CKE<=Vil(max)	tck = min.	ICC2P	8		mA	1
PRECHARGE STANDBY CURRENT in Non-Power Down Mode $\overline{CS}$ = VIH (min.), CKE>=Vih(min)	tck = min.	ICC2N	160	120	mA	1
NO OPERATING CURRENT tck = min., $\overline{CS}$ = VIH(min), active state (max. 4 banks)	CKE>=VIH(min.)	ICC3N	200	180	mA	1
	CKE<=VIL(max.)	ICC3P	40		mA	1
BURST OPERATING CURRENT tck = min., Read command cycling		ICC4	600	400	mA	1,2
AUTO REFRESH CURRENT tck = min., Auto Refresh command cycling		ICC5	960	880	mA	1
SELF REFRESH CURRENT Self Refresh Mode, CKE=0.2V, tck = infinity.	"non-L"-versions	ICC6	12		mA	1
	L-versions		7.2			

Notes:

1. These parameters depend on the cycle rate. These values are measured at 133 MHz for -7.5 and at 100 MHz for -8 modules. Input signals are changed once during tck.
2. These parameters are measured with continuous data stream during read access and all DQ toggling. CL=3 and BL=4 is assumed and the VDDQ current is excluded.

AC Characteristics 1)2)

T_A = 0 to 70 ×C; V_{SS} = 0 V; V_{CC} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values				Unit	
		-7.5 PC133 333		-8 PC100 222			
		min.	max.	min.	max.		
Clock and Access Time							
Clock Cycle Time							
$\overline{\text{CAS}}$ Latency = 3	t_{CK}	7.5	–	10	–	ns	
$\overline{\text{CAS}}$ Latency = 2		12	–		–	ns	
Clock Frequency							
$\overline{\text{CAS}}$ Latency = 3	t_{CK}	–	133	–	100	MHz	
$\overline{\text{CAS}}$ Latency = 2		–	100	–	100	MHz	
Access Time from Clock							
$\overline{\text{CAS}}$ Latency = 3	t_{AC}	–	5.4	–	6	ns	2, 3
$\overline{\text{CAS}}$ Latency = 2		–	6	–	6	ns	
Clock High Pulse Width	t_{CH}	2.5	–	3	–	ns	
Clock Low Pulse Width	t_{CL}	2.5	–	3	–	ns	
Transition time	t_T	0.5	7.5	0.5	10	ns	
Setup and Hold Parameter							
Input Setup Time	t_{IS}	1.5	–	2	–	ns	4
Input Hold Time	t_{IH}	0.8	–	1	–	ns	4
Power Down Mode Entry Time	t_{SB}	1	–	1	–	CLK	4
Power Down Mode Exit Setup Time	t_{PDE}	1	–	1	–	CLK	4
Mode Register Set-up time	t_{RSC}	2	–	2	–	CLK	
Common Parameters							
Row to Column Delay Time	t_{RCD}	20		20	–	ns	5
Row Precharge Time	t_{RP}	20		20	–	ns	5
Row Active Time	t_{RAS}	45	100k	45	100k	ns	5
Row Cycle Time	t_{RC}	67.5		70	–	ns	5
Activate(a) to Activate(b) Command period	t_{RRD}	15		16	–	ns	5
$\overline{\text{CAS}}$(a) to $\overline{\text{CAS}}$(b) Command period	t_{CCD}	1		1		CLK	

Parameter	Symbol	Limit Values				Unit	
		-7.5 PC133 333		-8 PC100 222			
		min.	max.	min.	max.		
Refresh Cycle							
Refresh Period (8192 cycles)	t_{REF}	–	64	–	64	ms	
Self Refresh Exit Time	t_{SREX}	1	–	1	–	CLK	6
Read Cycle							
Data Out Hold Time	t_{OH}	3	–	3	–	ns	2, 7
Data Out to Low Impedance Time	t_{LZ}	0	–	0	–	ns	
Data Out to High Impedance Time	t_{HZ}	3	7	3	8	ns	
DQM Data Out Disable Latency	t_{DQZ}	–	2	–	2	CLK	
Write Cycle							
Data Input to Precharge (write recovery)	t_{WR}		–	2	–	CLK	
DQM Write Mask Latency	t_{DQW}		–	0	–	CLK	

Notes:

1. An initial pause of 100 µs is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
2. AC timing tests have V_{il} = 0.4 V and V_{ih} = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{ih} and V_{il}. All AC measurements assume t_T=1ns with the AC output load circuit shownSpecified tac and toh parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1V / ns edge rate between 0.8V and 2.0 V.
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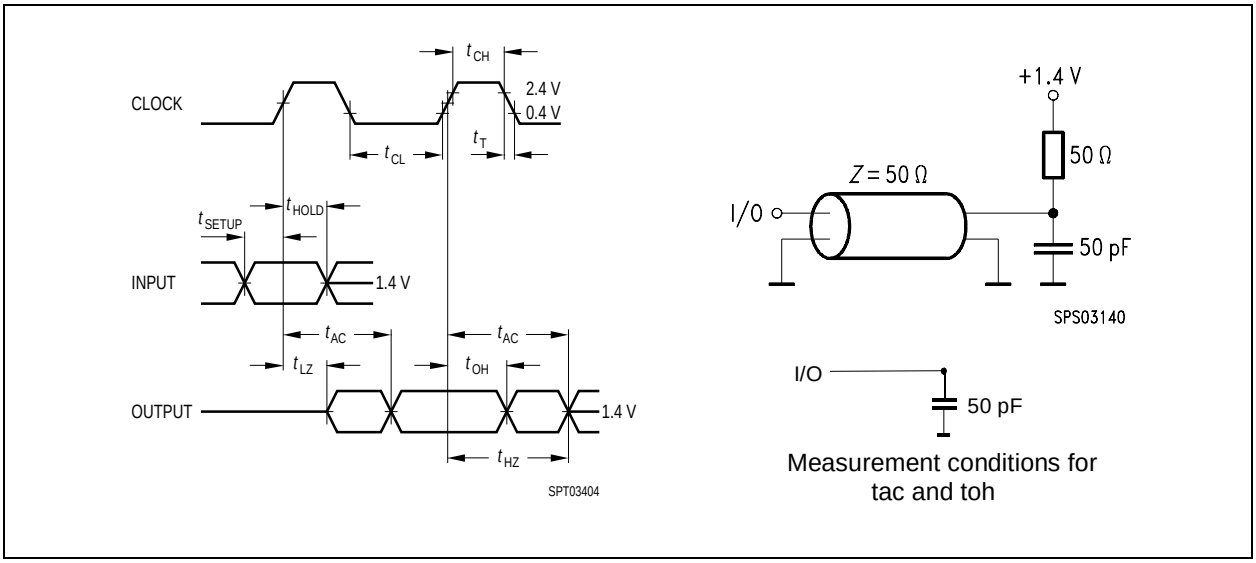


3. If clock rising time is longer than 1ns, a time (t_T -0.5) ns has to be added to this parameter.
4. If t_T is longer than 1ns, a time (t_T -1) ns has to be added to this parameter.
5. Any time that the refresh Period has been exceeded, a minimum of two Auto (CRB) Refresh commands must be given to “wake-up“ the device.
6. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to tRC is satisfied once the Self Refresh Exit command is registered.
7. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.

Serial Presence Detects:

A serial presence detect storage device - E^2PROM - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E^2PROM device during module production using a serial presence detect protocol (I^2C synchronous 2-wire bus)

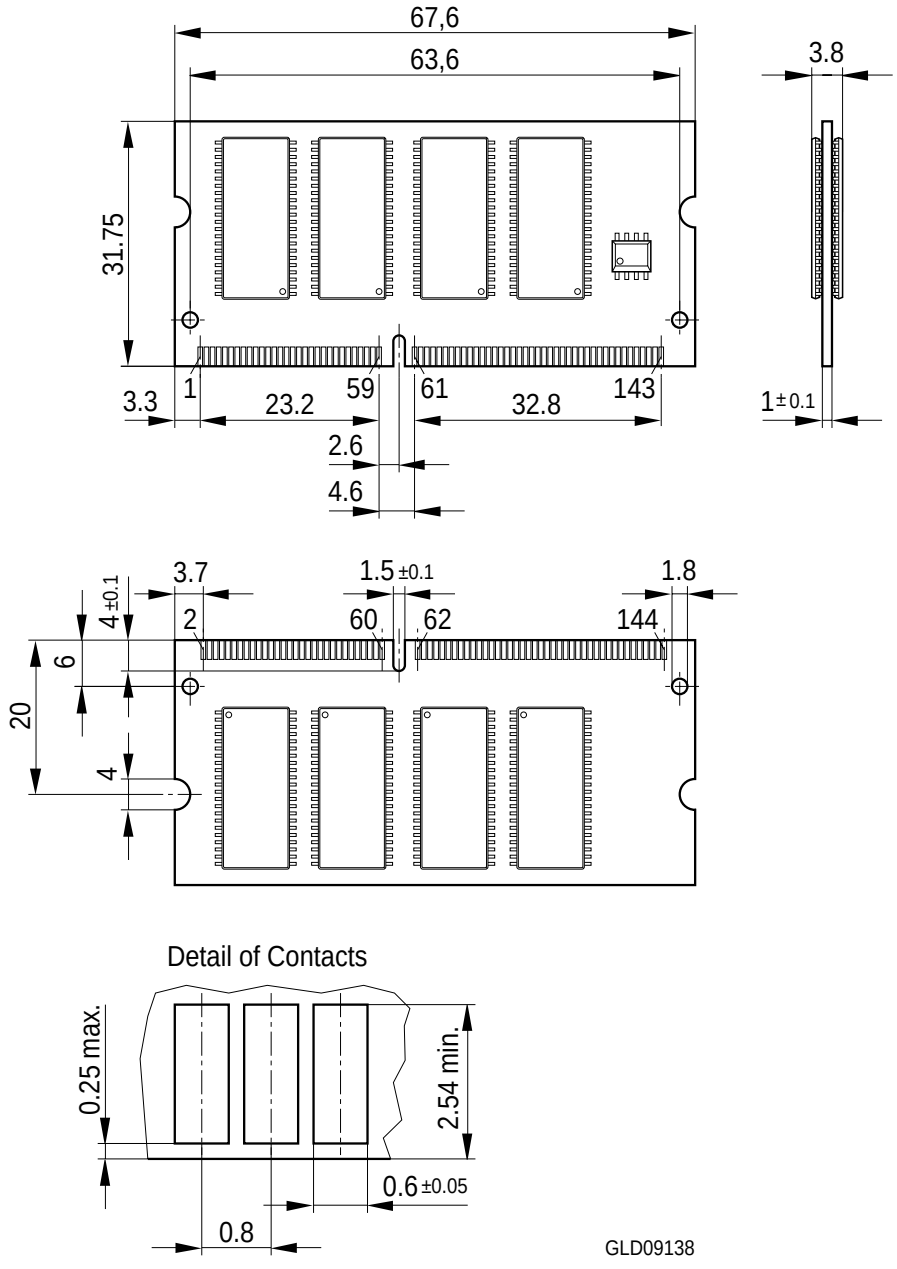
SPD-Table:

Byte#	Description	SPD Entry Value	Hex	
			32Mx64 -7.5	32Mx64 -8
0	Number of SPD bytes	128	80	
1	Total bytes in Serial PD	256	08	
2	Memory Type	SDRAM	04	
3	Number of Row Addresses (without BS)	13	0D	
4	Number of Column Addresses	9	09	
5	Number of DIMM Banks	2	02	
6	Module Data Width	64	40	
7	Module Data Width (cont'd)	0	00	
8	Module Interface Levels	LVTTL	01	
9	SDRAM Cycle Time at CL=3	7.5 / 10.0 ns	75	A0
10	SDRAM Access time from Clock at CL=3	5.4 / 6.0 ns	54	60
11	Dimm Config (Error Det/Corr.)	none	00	
12	Refresh Rate/Type	Self-Refresh, 7.8 µs	82	
13	SDRAM width, Primary	x16	10	
14	Error Checking SDRAM data width	n/a	00	
15	Minimum clock delay for back-to-back random column address	t_{ccd} = 1 CLK	01	
16	Burst Length supported	1, 2, 4 & 8	0F	
17	Number of SDRAM banks	2	04	
18	Supported CAS Latencies	2, & 3	06	
19	CS Latencies	CS latency = 0	01	
20	WE Latencies	Write latency = 0	01	
21	SDRAM DIMM module attributes	non buffered/non reg.	00	
22	SDRAM Device Attributes :General	Vcc tol +/- 10%	0E	
23	SDRAM Cycle Time at CL = 2	10 ns	A0	
24	SDRAM Access Time from Clock at CL=2	6.0 ns	60	
25	SDRAM Cycle Time at CL = 1	not supported	FF	
26	SDRAM Access Time from Clock at CL=1	not supported	FF	
27	Minimum Row Precharge Time	20 ns	14	

SPD-Table (cont'd):

Byte#	Description	SPD Entry Value	Hex	
			32Mx64 -7.5	32Mx64 -8
28	Minimum Row Active to Row Active delay	15 / 16 ns	0F	10
29	Minimum RAS to CAS delay	20 ns	14	
30	Minimum Ras pulse width	45 / 60 ns	2D	32
31	Module Bank Density (per bank)	128MB	20	
32	SDRAM input setup time	1.5 / 2 ns	15	20
33	SDRAM input hold time	0.8 / 1 ns	08	10
34	SDRAM data input setup time	1.5 / 2 ns	15	20
35	SDRAM data input hold time	0.8 / 1 ns	08	10
36-61	Superset information		FF	
62	SPD Revision	Revision 1.2	12	
63	Checksum for bytes 0 - 62		1E	81
64-125	Manufactures's information (optional)		FF	
126	Frequency Specification		64	
127	Details		C7	
128+	Unused storage locations		FF	

256 MByte SO-DIMM Module package (JEDEC MO-190)
(144 pin, dual read-out, single in-line memory module)



note: all tolerances are in accordance with the JEDEC standard

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