SIEMENS

3.3V 4M × 64-Bit EDO-DRAM Module
3.3V 4M × 72-Bit EDO-DRAM Module

168pin unbuffered DIMM Module with serial presence detect

HYM64V4005GU-50/-60/-70
HYM64V4045GU-50/-60/-70
HYM72V4005GU-50/-60/-70
HYM72V4045GU-50/-60/-70

Preliminary Information

- 168 Pin JEDEC Standard, Unbuffered 8 Byte Dual In-Line Memory Module
- 1 bank 4M × 64, 4M × 72 in 2k and 4k refresh organisations
- Optimized for byte-write non-parity or ECC applications
- Extended Data Out (EDO)
- Performance:

		-50	-60	-70
t_{RAC}	RAS Access Time	50 ns	60 ns	70 ns
t_{CAC}	CAS Access Time	13 ns	15 ns	20 ns
t_{AA}	Access Time from Address	25 ns	30 ns	35 ns
t_{RC}	Cycle Time	84 ns	104 ns	124 ns
t_{HPC}	EDO Mode Cycle Time	20 ns	25 ns	30 ns

- Single + 3.3 V ± 0.3 V Power Supply
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only-refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs and clocks are fully LV-TTL compatible
- Serial presence detects (optional)
- Utilizes 4M × 4 -DRAMs in TSOPII packages
- 2048 refresh cycles / 32 ms with 11 / 11 addressing (Row / Column) for HYM 64/72V4005GU
- 4096 refresh cycles / 64 ms with 12 / 10 addressing (Row / Column) for HYM 64/72V4045GU
- Gold contact pads
- Card Size: 133.35 mm × 25.40 mm × 4.00 mm
- This DRAM product module family is intended to be fully pin and architecture compatible with the 168pin unbuffered SDRAM DIMM module family

The HYM 64(72)V4005/45GU-50/-60/-70 are industry standard 168-pin 8-byte Dual In-Line Memory Modules (DIMMs) which are organized as 4M × 64 and 4M × 72 high speed memory arrays designed with EDO DRAMs for non-parity and ECC applications. 2k refresh with 11 / 11 addressing and 4k refresh modules with 12 / 10 addressing are available. The DIMMs use sixteen 4M × 4 EDO DRAMs for the 4M × 64 organisation and eighteen 4M × 4 DRAMs for the 4M × 72 organisation, both in TSOPII packages. Decoupling capacitors are mounted on the PC board.

The DIMMs use optional serial presence detects implemented via a serial E^2PROM using the two pin I^2C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes of serial PD data are available to the customer.

All 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133.35 mm long space-saving footprint.

Ordering Information

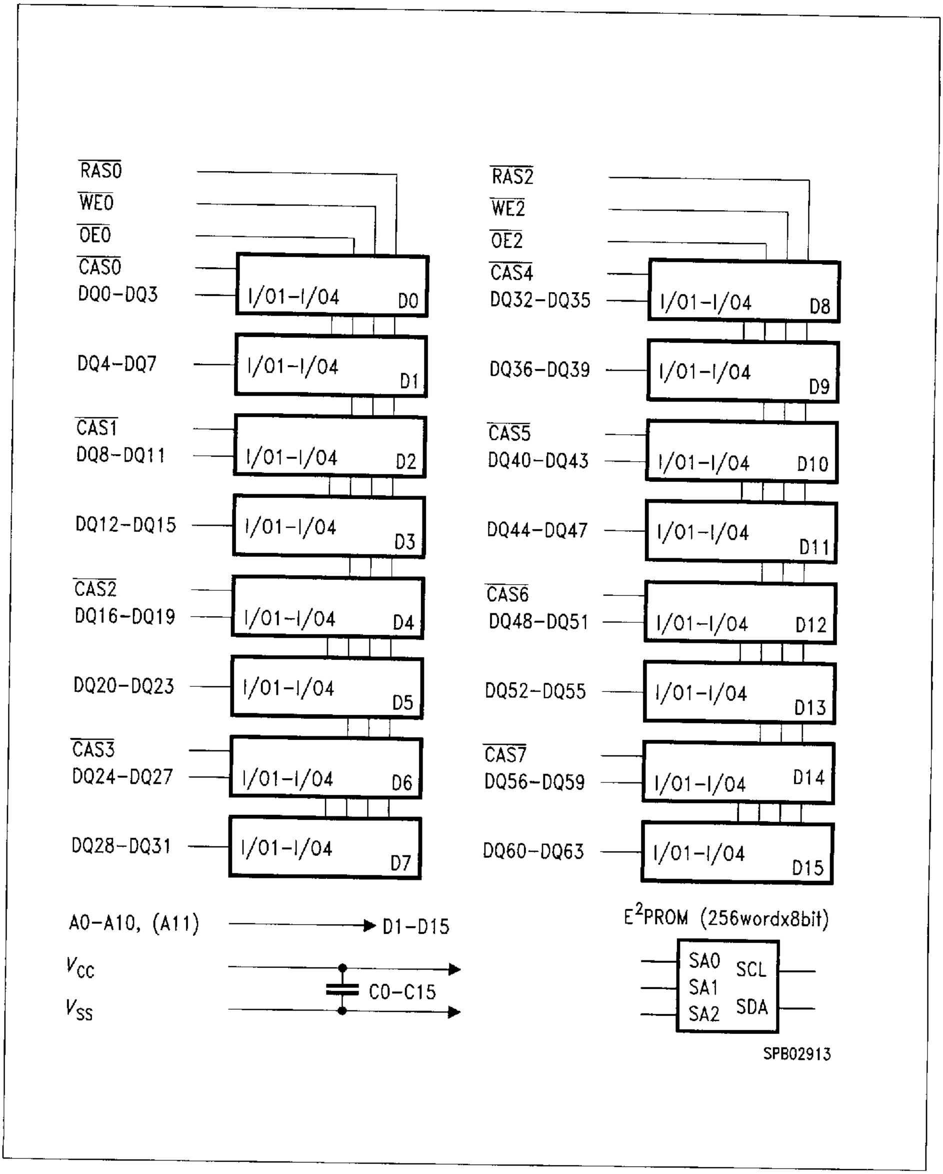
Type	Ordering Code	Package	Descriptions
2k-Refresh:			
HYM 64V4005GU-50	on request	L-DIM-168-12	4M x 64 DRAM module (access time 50 ns)
HYM 64V4005GU-60	on request	L-DIM-168-12	4M x 64 DRAM module (access time 60 ns)
HYM 64V4005GU-70	on request	L-DIM-168-12	4M x 64 DRAM module (access time 70 ns)
HYM 72V4005GU-50	on request	L-DIM-168-12	4M x 72 DRAM module (access time 50 ns)
HYM 72V4005GU-60	on request	L-DIM-168-12	4M x 72 DRAM module (access time 60 ns)
HYM 72V4005GU-70	on request	L-DIM-168-12	4M x 72 DRAM module (access time 70 ns)
4k-Refresh:			
HYM 64V4045GU-50	on request	L-DIM-168-12	4M x 64 DRAM module (access time 50 ns)
HYM 64V4045GU-60	on request	L-DIM-168-12	4M x 64 DRAM module (access time 60 ns)
HYM 64V4045GU-70	on request	L-DIM-168-12	4M x 64 DRAM module (access time 70 ns)
HYM 72V4045GU-50	on request	L-DIM-168-12	4M x 72 DRAM module (access time 50 ns)
HYM 72V4045GU-50	on request	L-DIM-168-12	4M x 72 DRAM module (access time 60 ns)
HYM 72V4045GU-70	on request	L-DIM-168-12	4M x 72 DRAM module (access time 70 ns)

Pin Names

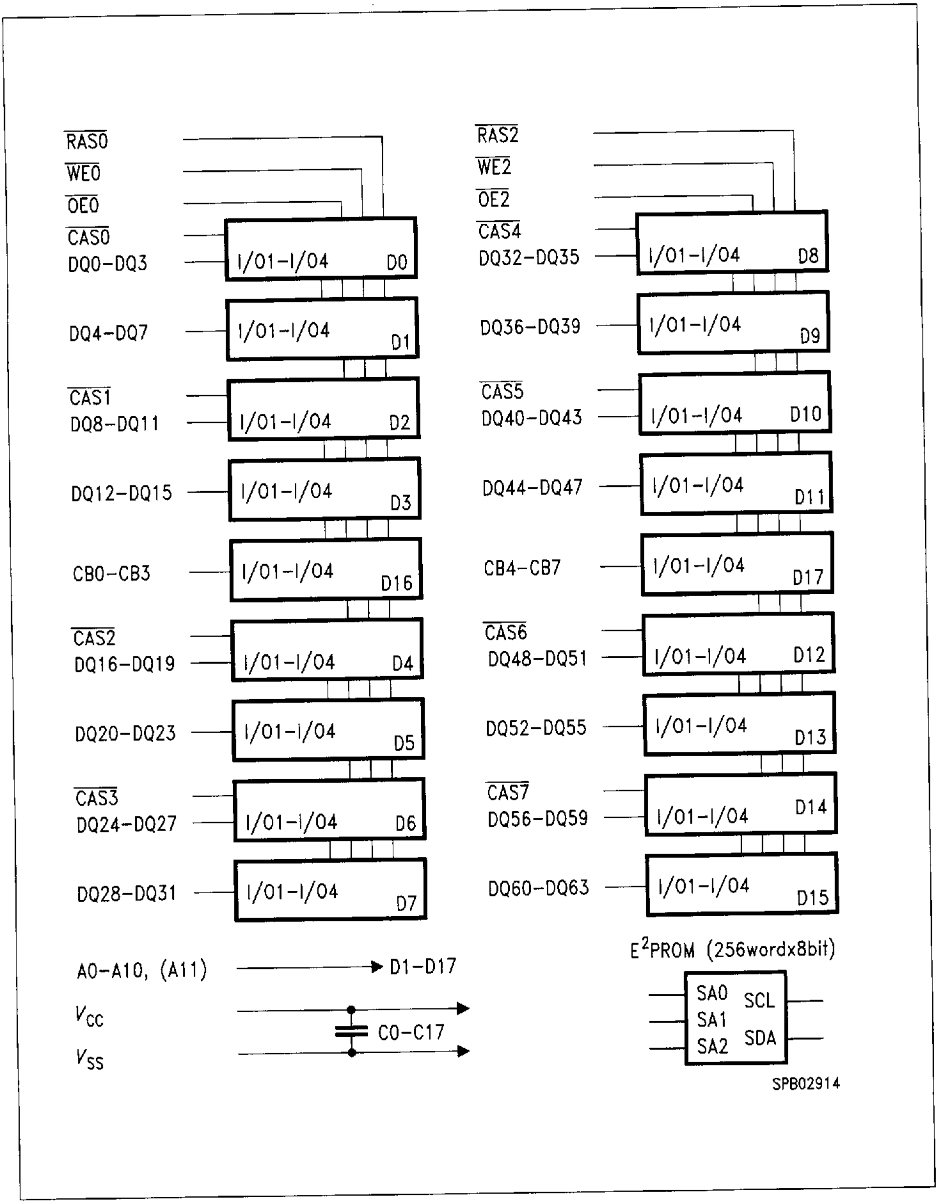
A0-A10	Row Address Input for HYB64/72V4005
A0-A10	Column Address Input for HYB64/72V4005
A0-A11	Row Address Input for HYB64/72V4045
A0-A9	Column Address Input for HYB64/72V4045
DQ0 - DQ63	Data Input/Output
CB0-CB7	Check Bit Data Input/Output (x72 only)
RAS0, RAS2	Row Address Strobe
CAS0 - CAS7	Column Address Strobe
WE0, WE2	Read / Write Input
OE0, OE2	Output Enable
Vcc	Power (+ 3.3 Volt)
Vss	Ground
SCL	Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0-SA2	Serial Presence Detect Addresses
N.C.	No Connection
DU	Don't use

Pin Configuration

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	OE2	86	DQ32	128	DU
3	DQ1	45	RAS2	87	DQ33	129	NC
4	DQ2	46	CAS2	88	DQ34	130	CAS6
5	DQ3	47	CAS3	89	DQ35	131	CAS7
6	VCC	48	WE2	90	VCC	132	DU
7	DQ4	49	VCC	91	DQ36	133	VCC
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB3	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VCC	101	DQ45	143	VCC
18	VCC	60	DQ20	102	VCC	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	DU	104	DQ47	146	DU
21	CB0	63	NC	105	CB4	147	NC
22	CB1	64	VSS	106	CB5	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VCC	68	VSS	110	VCC	152	VSS
27	WE0	69	DQ24	111	DU	153	DQ56
28	CAS0	70	DQ25	112	CAS4	154	DQ57
29	CAS1	71	DQ26	113	CAS5	155	DQ58
30	RAS0	72	DQ27	114	NC	156	DQ59
31	OE0	73	VCC	115	DU	157	VCC
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	A11	164	NC
39	NC	81	NC	123	NC	165	SA0
40	VCC	82	SDA	124	VCC	166	SA1
41	VCC	83	SCL	125	DU	167	SA2
42	DU	84	VCC	126	DU	168	VCC



4M x 64 DIMM Module Block Diagram



4M x 72 DIMM Module Block Diagram

Truth Table

FUNCTION		RAS	CAS	WRITE	OE	ROW ADDR	COL ADDR	DQ0-DQ63
Standby		H	X	X	X	X	X	High Impedance
Read		L	L	H	L	ROW	COL	Data Out
Early-Write		L	L	L	X	ROW	COL	Data In
Late-Write		L	L	H - L	H	ROW	COL	Data In
Read-Modify-Write (RMW)		L	L	H - L	L - H	ROW	COL	Data Out, Data In
EDO Page Mode Read	1st Cycle	L	H - L	H	L	ROW	COL	Data Out
	2nd Cycle	L	H - L	H	L	n/a	COL	Data Out
EDO Page Mode Write	1st Cycle	L	H - L	L	X	ROW	COL	Data In
	2nd Cycle	L	H - L	L	X	n/a	COL	Data In
EDO Page Mode RMW	1st Cycle	L	H - L	H - L	L - H	ROW	COL	Data Out, Data In
	2st Cycle	L	H - L	H - L	L - H	n/a	COL	Data Out, Data In
$\overline{RAS}$ only refresh		L	H	X	X	ROW	n/a	High Impedance
$\overline{CAS}$-before-$\overline{RAS}$ refresh		H - L	L	H	X	X	n/a	High Impedance
Hidden Refresh	READ	L-H-L	L	H	L	ROW	COL	Data Out
	WRITE	L-H-L	L	L	X	ROW	COL	Data In
Self Refresh		H - L	L	H	X	X	X	High Impedance

Serial Presence Detects:

A serial presence detect storage device -- EEPROM 24C02 -- is assembled on to the module. Information about the modul confuguration, speed, etc. is written into the EEPROM device during module production using a serial presence detect protocol (I^2C synchronous 2-wire bus).

Byte#	Description	SPD Entry Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex
0	Number of SPD bytes	128	1	0	0	0	0	0	0	0	80
1	Total bytes in Serial PD	256	0	0	0	0	1	0	0	0	08
2	Memory Type	EDO	0	0	0	0	0	0	1	0	02
3	Number of Row Addresses	11	0	0	0	0	1	0	1	1	0B
		12	0	0	0	0	1	1	0	0	0C
4	Number of Column Addresses	11	0	0	0	0	1	0	1	1	0B
		10	0	0	0	0	1	0	1	0	0A
5	Number of DIMM Banks	1	0	0	0	0	0	0	0	1	01
6	Module Data Width	x64	0	1	0	0	0	0	0	0	40
		x72	0	1	0	0	1	0	0	0	48
7	Module Data Width (cont'd)	0	0	0	0	0	0	0	0	0	00
8	Module Interface Levels	LVTTL	0	0	0	0	0	0	0	1	01
9	RAS access time	50 ns	0	0	1	1	0	0	1	0	32
		60 ns	0	0	1	1	1	1	0	0	3C
		70 ns	0	1	0	0	0	1	1	0	46
10	CAS access time	13 ns	0	0	0	0	1	1	0	1	0D
		15 ns	0	0	0	0	1	1	1	1	0F
		20 ns	0	0	0	1	0	1	0	0	14
11	Dimm Config (Error Det/Corr.)	none	0	0	0	0	0	0	0	0	00
		ECC	0	0	0	0	0	0	1	0	02
12	Refresh Rate/Type	normal 15.6µs	0	0	0	0	0	0	0	0	00

Absolute Maximum Ratings

Operating temperature range .... 0 to + 70 °C
Storage temperature range........ – 55 to + 125 °C
Input/output voltage .... – 0.5 to min. (V_{CC} + 0.5, 4.6) V
Power supply voltage........ – 0.5 to 4.6 V
Power dissipation........ 9.94 W
Data out current (short circuit) .... 50 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = 3.3 V ± 0.3 V

Parameter	Symbol	x 64/x 72		Unit	Notes
		min.	max.		
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
Output high voltage (LVTTL) Output „H“ level voltage (I_{OUT} = – 2 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (LVTTL) Output „L“ level voltage (I_{OUT} = + 2 mA)	V_{OL}	–	0.4	V	1)
Output high voltage (LVCMOS) Output „H“ level voltage (I_{OUT} =– 100µA)	V_{OH}	V_{CC} – 0.2	–	V	1)
Output low voltage (LVCMOS) Output „L“ level voltage (I_{OUT} =+100 µA)	V_{OL}	–	0.4	V	1)
Input leakage current (0 V < V_{IN} < V_{CC}, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	– 10	+10	µA	1)

DC Characteristics for HYM64/72V4005

T_A = 0 to 70 °C; V_{CC} = 3.3 V ± 0.3 V

Parameter	Symbol	x 64		x 72		Unit	Notes
		min.	max.	min.	max.		
Average V_{CC} supply current:	I_{CC1}						
-50 version		–	1920	–	2160	mA	2) 3) 4)
-60 version		–	1760	–	1980	mA	
-70 version		–	1600	–	1800	mA	
($\overline{RAS}$,$\overline{CAS}$,address cycling, $t_{RC} = t_{RC}$ min.)							
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = $V_{IH,}$ one address change)	I_{CC2}	–	32	–	36	mA	–
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles:	I_{CC3}						2) 4)
-50 version		–	1920	–	2160	mA	
-60 version		–	1760	–	1980	mA	
-70 version		–	1600	–	1800	mA	
($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, $t_{RC} = t_{RC}$ min.)							
Average V_{CC} supply current during hyper page mode (EDO):	I_{CC4}						
-50 version		–	1120	–	1260	mA	2) 3) 4)
-60 version		–	880	–	990	mA	
-70 version		–	720	–	810	mA	
($\overline{RAS}$ = $V_{IL,}$ $\overline{CAS}$, address cycling $t_{PC} = t_{PC}$ min.)							
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V, one address change)	I_{CC5}	–	16	–	18	mA	–
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode:	I_{CC6}						
-50 version		–	1920	–	2160	mA	2) 4)
-60 version		–	1760	–	1980	mA	
-70 version		–	1600	–	1800	mA	
($\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min.)							

DC Characteristics for HYM64/72V4045

T_A = 0 to 70 °C; V_{CC} = 3.3 V ± 0.3 V

Parameter	Symbol	x 64		x 72		Unit	Notes
		min.	max.	min.	max.		
Average V_{CC} supply current:	I_{CC1}						
-50 version		–	1600	–	1800	mA	2) 3)
-60 version		–	1440	–	1620	mA	4)
-70 version		–	1280	–	1440	mA	
($\overline{RAS}$,$\overline{CAS}$,address cycling, $t_{RC} = t_{RC}$ min.)							
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = $V_{IH,}$ one address change)	I_{CC2}	–	32	–	36	mA	–
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles:	I_{CC3}						2) 4)
-50 version		–	1600	–	1800	mA	
-60 version		–	1440	–	1620	mA	
-70 version		–	1280	–	1440	mA	
($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, $t_{RC} = t_{RC}$ min.)							
Average V_{CC} supply current during hyper page mode (EDO):	I_{CC4}						
-50 version		–	1120	–	1260	mA	2) 3)
-60 version		–	880	–	990	mA	4)
-70 version		–	720	–	810	mA	
($\overline{RAS}$ = $V_{IL,}$ $\overline{CAS}$, address cycling $t_{PC} = t_{PC}$ min.)							
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V, one address change)	I_{CC5}	–	16	–	18	mA	–
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode:	I_{CC6}						
-50 version		–	1600	–	1800	mA	2) 4)
-60 version		–	1440	–	1620	mA	
-70 version		–	1280	–	1440	mA	
($\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min.)							

AC Characteristics 5)6)

16E

T_A = 0 to 70 ˚C, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit	Notes
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
Common Parameters									
Random read or write cycle time	t_{RC}	84	–	104	–	124	–	ns	
$\overline{\text{RAS}}$ precharge time	t_{RP}	30	–	40	–	50	–	ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	8	10k	10	10k	12	10k	ns	
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	8	–	10	–	12	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	12	37	14	45	14	53	ns	
$\overline{\text{RAS}}$ to column address delay	t_{RAD}	10	25	12	30	12	35	ns	
$\overline{\text{RAS}}$ hold time	t_{RSH}	13		15	–	17	–	ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	40		50	–	60	–	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns	
Transition time (rise and fall)	t_T	1	50	1	50	1	50	ns	7
Refresh period for 2k-refresh	t_{REF}	–	32	–	32	–	32	ms	
Refresh period for 4k-refresh	t_{REF}	–	64	–	64	–	64	ms	
Read Cycle									
Access time from $\overline{\text{RAS}}$	t_{RAC}	–	50	–	60	–	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	–	13	–	15	–	17	ns	8, 9
Access time from column address	t_{AA}	–	25	–	30	–	35	ns	8, 10
$\overline{\text{OE}}$ access time	t_{OEA}	–	13	–	15	–	17	ns	
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	25	–	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	11
Read command hold time referenced to $\overline{\text{RAS}}$	t_{RRH}	0	–	0	–	0	–	ns	11

AC Characteristics (cont'd) 5)6)

16E

T_A = 0 to 70 ˚C, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit	Notes
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	–	0	–	0	–	ns	8
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	17	ns	12
Output turn-off delay from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	17	ns	12
Data to $\overline{CAS}$ low delay	t_{DZC}	0	–	0	–	0	–	ns	13
Data to $\overline{OE}$ low delay	t_{DZO}	0	–	0	–	0	–	ns	13
$\overline{CAS}$ high to data delay	t_{CDD}	10	–	13	–	15	–	ns	14
$\overline{OE}$ high to data delay	t_{ODD}	10	–	13	–	15	–	ns	14
Write Cycle									
Write command hold time	t_{WCH}	8	–	10	–	10	–	ns	
Write command pulse width	t_{WP}	8	–	10	–	10	–	ns	
Write command setup time	t_{WCS}	0	–	0	–	0	–	ns	15
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	–	15	–	17	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13	–	15	–	17	–	ns	
Data setup time	t_{DS}	0	–	0	–	0	–	ns	16
Data hold time	t_{DH}	8	–	10	–	12	–	ns	16
Read-modify-write Cycle									
Read-write cycle time	t_{RWC}	113	–	138	–	162	–	ns	
$\overline{RAS}$ to WE delay time	t_{RWD}	64	–	77	–	89	–	ns	15
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	27	–	32	–	36	–	ns	15
Column address to $\overline{WE}$ delay time	t_{AWD}	39	–	47	–	54	–	ns	15
$\overline{OE}$ command hold time	t_{OEH}	10	–	13	–	15	–	ns	
Hyper Page Mode (EDO) Cycle									
Hyper page mode (EDO) cycle time	t_{HPC}	20	–	25	–	30	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	–	10	–	10	–	ns	

AC Characteristics (cont'd) [5)6)] 16E
T_A = 0 to 70 ˚C, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit	Notes
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	27	–	32	–	37	ns	7
Output data hold time	t_{COH}	5	–	5	–	5	–	ns	
$\overline{RAS}$ pulse width in EDO mode	t_{RAS}	50	200k	60	200k	70	200k	ns	
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHPC}	27	–	32	–	37	–	ns	
Hyper Page Mode (EDO) Read-modify-write Cycle									
Hyper page mode (EDO) read-write cycle time	t_{PRWC}	58	–	68	–	77	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$	t_{CPWD}	41	–	49	–	56	–	ns	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle									
$\overline{CAS}$ setup time	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ hold time	t_{CHR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	5	–	ns	
Write to $\overline{RAS}$ precharge time	t_{WRP}	10	–	10	–	10	–	ns	
Write hold time referenced to $\overline{RAS}$	t_{WRH}	10	–	10	–	10	–	ns	

Capacitance
T_A = 0 to 70 ˚C; V_{CC} = 3.3 V ± 0.3 V; f = 1 MHz

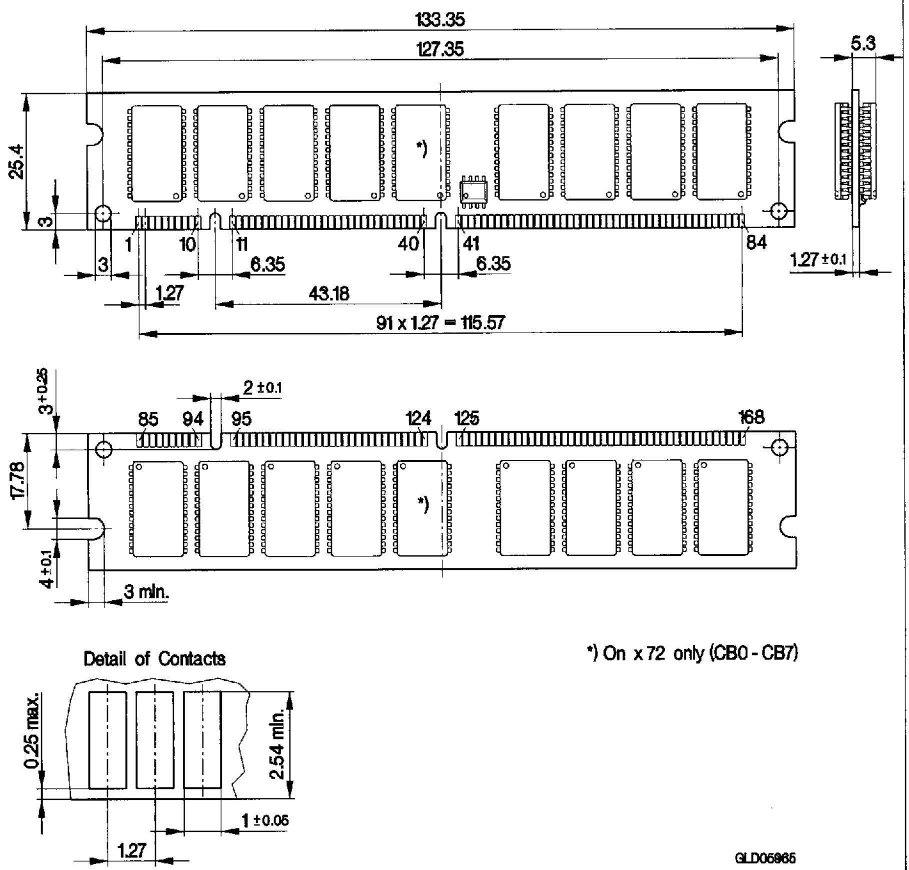
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input Capacitance (A0 to A11)	C_{I1}	–	100	pF
Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	–	75	pF
Input Capacitance ($\overline{CAS0}$-$\overline{CAS7}$)	C_{I3}	–	18	pF
Input Capacitance ($\overline{WE0}$,$\overline{WE2}$,$\overline{OE0}$,$\overline{OE2}$)	C_{I4}	–	75	pF
I/O Capacitance (DQ0-DQ63,CB0-CB8)	C_{IO1}	–	11	pF
Input Capacitance (SCL, SA0-2)	C_S	–	8	pF
Input/Output Capacitance (SDA)	C_S	–	10	pF

Notes:

1) All voltages are referenced to V_{SS}.
2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
3) I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
4) Address can be changed once or less while RAS = V_{IL}. In case of I_{CC4} it can be changed once or less during a hyper page mode (EDO) cycle
5) An initial pause of 200 µs is required after power-up followed by 8 RAS cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 CAS-before-$\overline{\text{RAS}}$ initialization cycles instead of 8 RAS cycles are required.
6) AC measurements assume t_T = 2 ns.
7) $V_{IH\,(min.)}$ and $V_{IL\,(max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
8) Measured with the specified current load and 100 pF at V_{ol} = 0.8 V and V_{oh} = 2.0 V. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{AA}, t_{CPA} , t_{OEA}. t_{CAC} is measured from tristate.
9) Operation within the $t_{RCD\,(max.)}$ limit ensures that $t_{RAC\,(max.)}$ can be met. $t_{RCD\,(max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD\,(max.)}$ limit, then access time is controlled by t_{CAC}.
10) Operation within the $t_{RAD\,(max.)}$ limit ensures that $t_{RAC\,(max.)}$ can be met. $t_{RAD\,(max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD\,(max.)}$ limit, then access time is controlled by t_{AA}.
11) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12) $t_{OFF\,(max.)}$, $t_{OEZ\,(max.)}$ define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels. t_{OFF} is referenced from the rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.
13) Either t_{DZC} or t_{DZO} must be satisfied.
14) Either t_{CDD} or t_{ODD} must be satisfied.
15) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\,(min.)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\,(min.)}$, $t_{CWD} > t_{CWD\,(min.)}$ and $t_{AWD} > t_{AWD\,(min.)}$, the cycle is a read-write cycle and I/O will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.
16) These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{WE}}$ leading edge in read-write cycles.

Package Outlines

L-DIM-168-12
(Double In-line Module)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".
SMD = Surface Mounted Device

Dimensions in mm

Packing Information

DRAM Modules

Type	Packing	Modules per Box
72 pin SIMM	Boxes with Trays	80
72 pin Small Outline DIMM	Boxes with Trays	80
168 pin DIMM	Boxes with Trays	40