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Honeywell

VDTDemod

VARIABLE DIFFERENTIAL TRANSFORMER DEMODULATOR

Preliminary

This is a Boeing owned design manufactured by Honeywell

FEATURES

- Programmable electronic interface between a LVDT or RVDT sensor for servo loop control
- Built-in Self Test features to test the integrity of the sensor and the VDTDemod circuits
- Kelvin switches in demodulator eliminate switch resistance errors
- Synchronous demodulation completely cancels offset using 50% duty cycle
- One uncommitted Opamp per channel for optional 2 pole filtering

OTHER

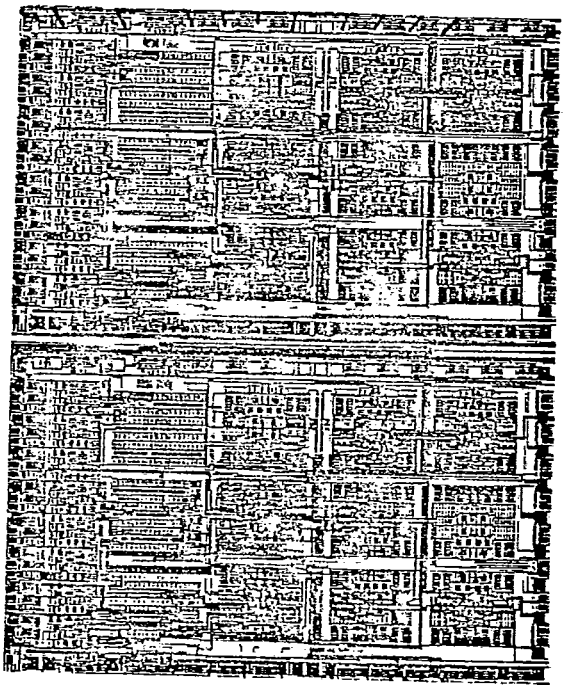
- Full Military Temperature Range
- Low Power: < 370 mW with +5V, ±15V supplies
- Input Voltage Range: ±8 Volts
- DOUT Output V_{OFFSET} <3 mV (over Temp.)
- Filter Opamp Input V_{OFFSET} <1.4 mV (over Temp.)
- Gain Error < 0.09 % (over Temp.)
- Linearity: < 0.02 % (over Temp.)
- Die Size: 233 x 288 mil²

GENERAL DESCRIPTION

The VDTDemodulator is a programmable, self contained electronic interface used to synchronously demodulate a rotary variable differential transformer (RVDT) or a linear variable differential transformer (LVDT) position transducer. It provides two identical, independent channels that synchronously demodulate two differential ac input signals with respect to reference signals. The reference signals may be either independent or a common signal. The two outputs are dc levels proportional to the amplitude of their inputs, with a polarity dictated by the phase relationships between the input signals and their references. The device is configured to provide means for high accuracy ratiometric compensation for variations due to changes in the amplitude of the reference signal powering the transducer. This involves using half of the device to convert the reference signal level to dc and externally providing the ratio of the transducer output to its input. A typical implementation is shown in block diagram form at the end of this data sheet.

The VDTDemodulator provides increased packaging efficiency, lower cost, reduced failure rates and lower power supply requirements than conventional circuit implementations. It also features built-in-test and transducer monitoring capability to allow for system reconfiguration and maintenance monitoring. Each channel has an input multiplexer that can be used for system reconfiguration, system self-calibration, or multiplexing of additional transducers, as required.

The VDTDemod is fabricated with Honeywell's Advanced Linear Bipolar technology (ALB-1A), and is designed using the ALBERTA semi-custom analog array.



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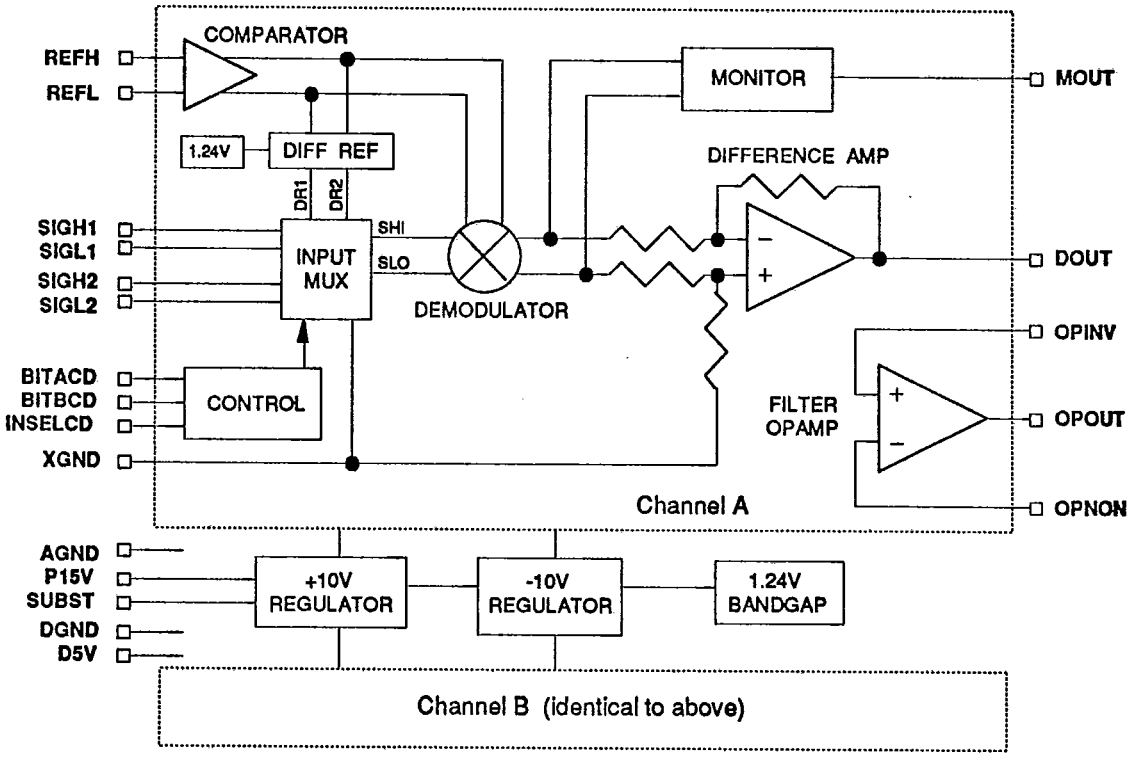
FUNCTIONAL DIAGRAM



FUNCTIONAL BLOCK DESCRIPTION

The Block Diagram above shows the functional equivalent blocks in a single channel of the VDTDemod integrated circuit. There are two identical circuits on the IC that provide the following functions for channels A and B.

The INPUT MUX cell provides multiplex switching of the differential signal paths between Signal 1 high/low pins, and Signal 2 high/low pins.

The control of the INPUT MUX state for the seven operating modes is provided by the CONTROL cell. These are TTL logic input levels. These include the choice of two inputs: transducer tests or self-test.

The differential voltage comparator (COMPARATOR) monitors the reference levels (REFH/REFL) and provides the synchronization signal used in the demodulation process. A multiplexing cell in the demodulator monitors the synchronization signal and reverses the differential amplifier inputs at each zero crossing. The result of the switching action controlled by the comparator is that the DIFFERENCE AMP gain changes sign from +1 to -1 every half cycle, causing a full-wave rectified synchronous demodulation of the input sinusoid differential signal to be present at the DOUT pin.

The DIFF REF provides a square-wave signal controlled by the synchronization signal that is used by the DEMODULATOR to provide one of the self-test features.

Buffer amplifiers on signal lines SHI and SLO along with an OP20 configured amplifier are used to build the 3-op amp instrumentation amplifier (DIFFERENCE AMP) whose gain is being switched from +1 to -1.

The MONITOR cell is used to provide a half-wave rectified positive output named MOUT that is proportional to the common mode signal input. The common mode amplitude MOUT can be used to determine the health of the transducer and system wiring.

The FILTER OPAMPs whose inputs are wired to external pins are uncommitted OP20 operational amplifier useful in completing the position measuring system.

One VREF band gap reference circuit is used to set the output voltage of the +10V and -10V regulator cells that reduce the +15V/-15V power supply voltages. The other 1.24V BANDGAP reference cell is used by the reference COMPARATOR cell in the self-test mode.

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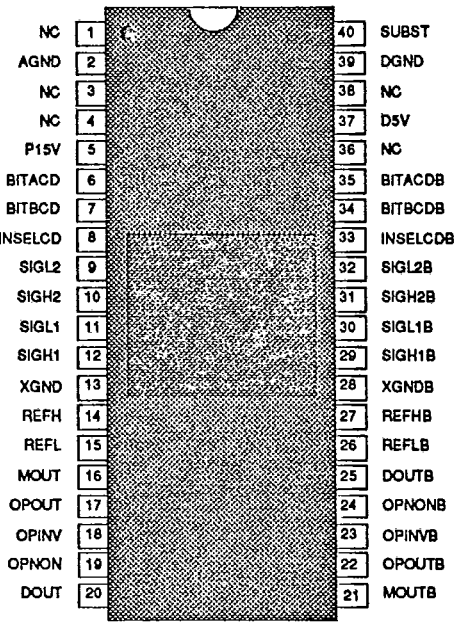
PIN DEFINITIONS AND ASSIGNMENTS

Channel A	Channel B	Signal Name
SIGH1	SIGH1B	Signal Source 1 Input High
SIGL1	SIGL1B	Signal Source 1 Input Low
SIGH2	SIGH2B	Signal Source 2 Input High
SIGL2	SIGL2B	Signal Source 2 Input Low
BITACD	BITACDB	Built-In-Test A Command
BITBCD	BITBCDB	Built-In-Test B Command
INSELCD	INSELCDB	Input Select Command
REFH	REFHB	Reference Input High
REFL	REFLB	Reference Input Low
DOUT	DOUTB	Demodulated Output
MOUT	MOUTB	Monitor Output
OPINV	OPINVB	Opamp Inverting Input
OPNON	OPNONB	Opamp Non-Inverting Input
OPOUT	OPOUTB	Opamp Output
XGND	XGNDB	Output Ground for DOUT
P15V		+15V Power Supply Input
SUBST		-15V Power Supply Input
D5V		+5V Digital Power Supply Input
AGND		±15V Power Supply Ground
DGND		+5V Power Supply Ground



NC = No Connect

40 pin DIP

VDTDemod PINOUT DIAGRAM

CONTROL INPUT LOGIC DEFINITION (1)

BITACD	BITBCD	INSELCD	Operating Mode	DOUT	MOUT	SHI	SLO
0	0	X	1.2V Gain Test	between 1.1V and 1.3V dc	between 0.52V and 0.68V dc	DR1 (2)	DR2 (2)
0	1	0	Low Signal Leg Source 2	synchronous demodulation of SIGL2	positive half-wave rectified SIGL2	XGND	SIGL2
0	1	1	Low Signal Leg Source 1	synchronous demodulation of SIGL1	positive half-wave rectified SIGL1	XGND	SIGL1
1	0	0	High Signal Leg Source 2	synchronous demodulation of SIGH2	positive half-wave rectified SIGH2	SIGH2	XGND
1	0	1	High Signal Leg Source 1	synchronous demodulation of SIGH1	positive half-wave rectified SIGH1	SIGH1	XGND
1	1	0	Signal Source 2	synchronous demodulation of (SIGH2-SIGL2)	positive half-wave rectified (SIGH2+SIGL2)/2	SIGH2	SIGL2.
1	1	1	Signal Source 1	synchronous demodulation of (SIGH1-SIGL1)	positive half-wave rectified (SIGH1+SIGL1)/2	SIGH1	SIGL1

(1) Logic Definition: 0=TTL Low, V_{IL}=0.8V maximum; 1=TTL High, V_{IH}=2.0 minimum; X=Don't Care
(2) DR1 and DR2 are precision 1.24V square wave signals generated from the synchronization signal

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ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating		Units
		Min.	Max.	
P15V	Positive Supply Voltage (2)	-0.5	18	V
SUBST	Negative Supply Voltage (2)	-18	0.5	V
D5V	Digital Supply Voltage (3)	-0.5	7	V
VSIG	Signal Input/Output Voltage (2)	SUBST-0.5	P15V+0.5	V
VCP	Control Pin Voltage (3)	-0.5	D5V+0.5	V
PD	Power Dissipation (Free Air)		600	mW
TJ	Junction Temperature		150	°C
TSTG	Storage Temperature (Zero Bias)	-60	175	°C

(1) Stresses in excess of those listed above may result in permanent damage to the VDTDemod. These are stress ratings only and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to AGND.
(3) Voltage referenced to DGND.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Description			Units
		Min.	Typ.	Max.	
P15V	Positive Supply Voltage (1)	14	15	16	V
SUBST	Negative Supply Voltage (1)	-16	-15	-14	V
D5V	Digital Supply Voltage (2)	4.5	5.0	5.5	V
Tc	Case Temperature	-55	25	125	°C
Fin	Input Frequency	300		2000	Hz
Vin	Input Voltage Range (REF/SIG pins)	-8.0		+8.0	Vpk
VFSout	Full Scale Output Swing (DOUT,OPOUT,MOUT)	-8.0		+8.0	Vpk

(1) Voltage referenced to AGND.
(2) Voltage referenced to DGND.

ELECTRICAL CHARACTERISTICS (Tc= -55 to +125°C, P15V=15V, SUBST=-15V, D5V=5V unless otherwise noted)

Symbol	Parameter	Description			Units
		Min.	Typ.	Max.	
I+	Power Supply Current, Analog (P15V)			12.5	mA
I-	Power Supply Current, Analog (SUBST)			-11	mA
ID	Power Supply Current, Digital (D5V)			3.5	mA
RINS	Input Resistance (SIG pins)	100			Mohm
VIOS	Input Offset Voltage (SIG pins)			3.0	mV
IIBS	Input Bias Current (SIG pins); 0V on all signal pins			60	nA

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter	Description			Units
		Min.	Typ.	Max.	
I_{IOS}	Input Offset Current (SIG pins)			20	nA
V_{IOR}	Input Offset Voltage (REF pins); T_C= 25°C			10	mV
I_{IL}	Low Level Input Current (Ctl pins); D5V=5.5V, Vin=0.4V	-100		+100	µA
I_{IH}	High Level Input Current (Ctl pins); D5V=5.5V, Vin=2.4V	-50		+50	µA
V_{IOO}	Input Offset Voltage (Filter Opamp); V_{CM}=0			1.4	mV
I_{IBO}	Input Bias Current (Filter Opamp); V_{CM}=0			60	nA
I_{IOO}	Input Offset Current (Filter Opamp); V_{CM}=0			20	nA
NL	Nonlinearity (SIG pins); measured using 0.05 FS steps			0.02	% FS
G_{DEM}	Gain of Demodulator (tested)	0.9991		1.0009	Vdc/Vdc
CMRR	Common Mode Rejection Ratio; f=dc	50			dB
V_{IND}	Differential Voltage Input (REF and SIG pins); FS			8	Vpk
V_{INP}	Full Scale Input Range (REF and SIG pins)	-8.0		+8.0	Vpk
V_{OPP}	FS Output Swing (output pins); R_L=5K, C_L=100pF	-8.0		+8.0	Vpk

NOTE: All voltages are measured with respect to ground (AGND, DGND) unless otherwise indicated.

ELECTRICAL CHARACTERISTICS GUARANTEED BY DESIGN

(T_C= -55 to +125°C, P15V=15V, SUBST=-15V, D5V=5V unless otherwise noted)

Symbol	Parameter	Description			Units
		Min.	Typ.	Max.	
PSRR	Power Supply Rejection Ratio; f=1000Hz	60			dB
C_{IN}	Input Capacitance (SIG pins)			100	pF
Ø	Phase Shift of COMPARATOR; @ 400 and 1800 Hz			1.0	° Shift
GBW	Gain Bandwidth (Filter Opamp)	600			KHz
A_V	Open Loop Voltage Gain (Filter Opamp)	100			dB
G_{DEM}	Gain of Demodulator (over lifetime) (1)	0.9982		1.0018	V/V
V_{IH}	High Level Input Voltage (control pins)	2.0			V
V_{IL}	Low Level Input Voltage (control pins)			0.8	V
Z_{IN}	Input Impedance Reference Inputs; f=400Hz	400			Kohm
CMRR1	DEMODULATOR CMRR; f=400Hz	50			dB
CMRR2	DEMODULATOR CMRR; f=1800Hz	40			dB

NOTE: All voltages are measured with respect to ground unless otherwise indicarted.
(1) Maximum deviation over lifetime (Life=1000 Hrs @ 125°C in Burn-In test)

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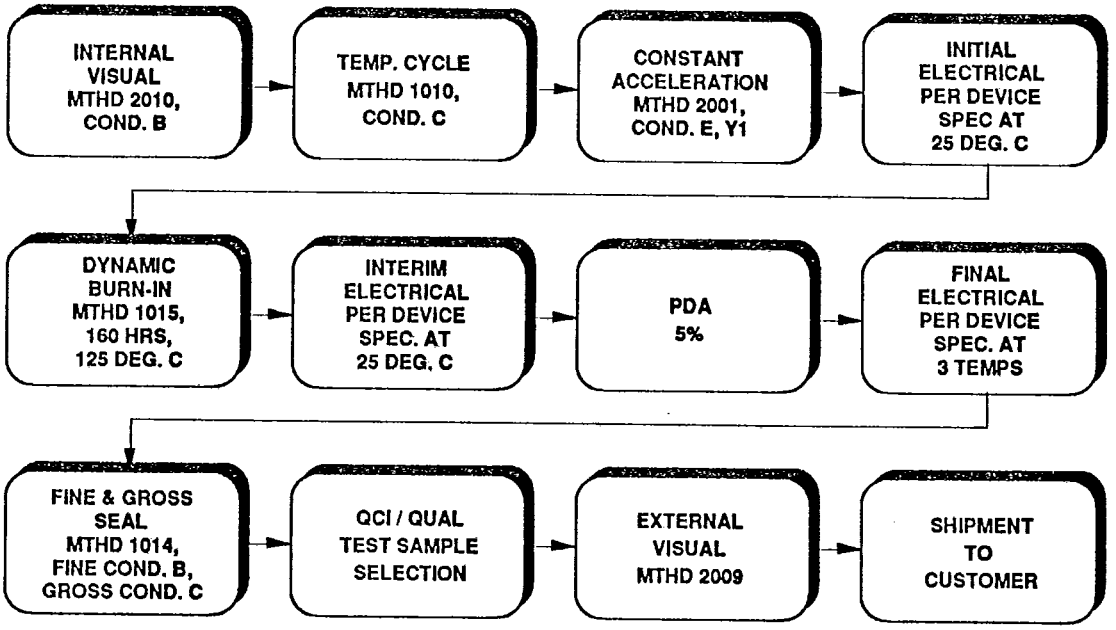
QUALIFICATION AND SCREENING

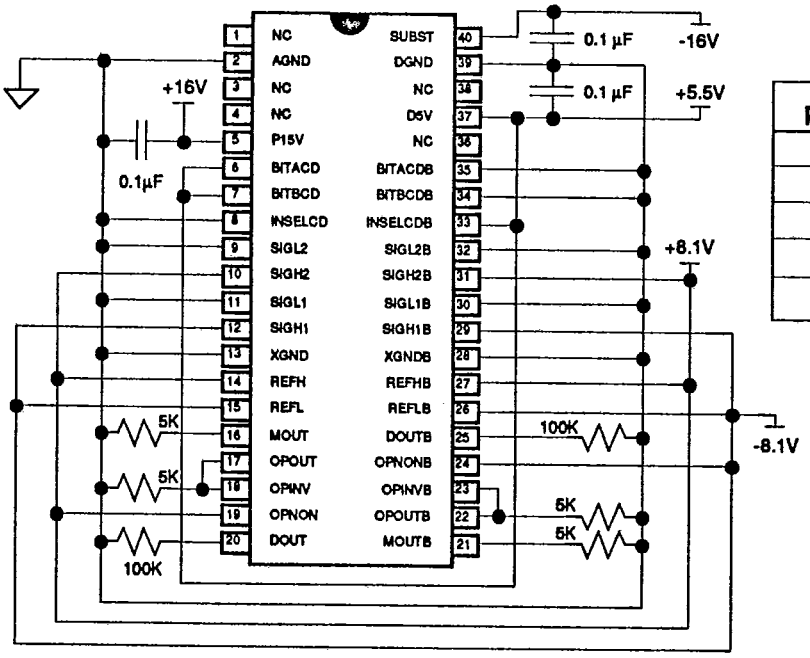
Honeywell maintains a high level of product integrity through process control, utilizing statistical process control, a complete "Total Quality Assurance System," and a computer data based process performance tracking system.

The VDTDemod will be qualified and screened to the most advanced military standards. The Figure below illustrates the MIL-STD-883C Class B flow. Customer specific qualification flows are available upon request.



MIL-STD-883C CLASS B PRODUCT FLOW

BURN-IN AND LIFE TEST CIRCUIT



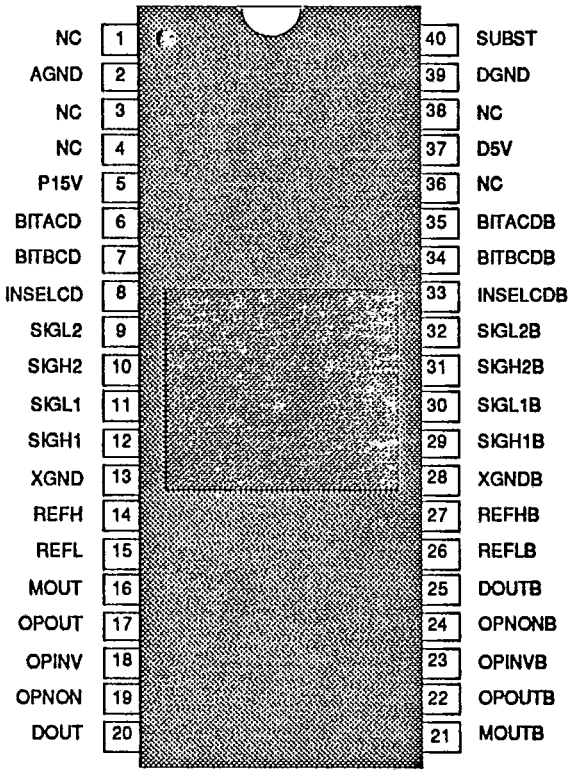
Power Supplies	Tolerance	Current/Device
+ 16V max	± 0.1V	15 mA
- 16V max	± 0.1V	15 mA
+ 8.1V max	± 0.1V	1 mA
- 8.1V max	± 0.1V	1 mA
+ 5.5V max	± 0.1V	2 mA

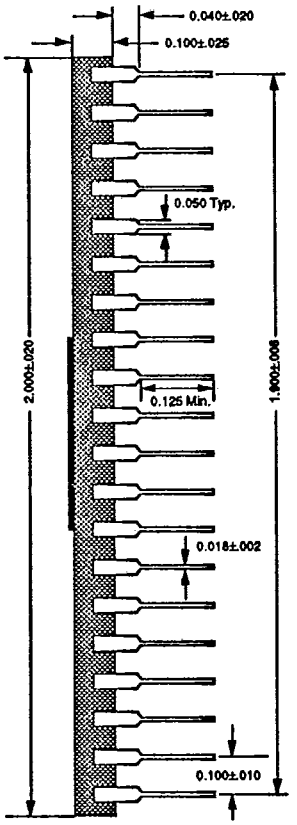
Burn-in Conditions:

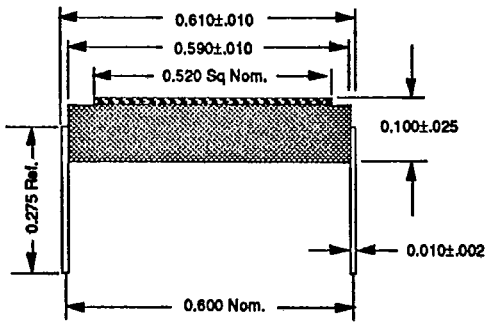
160 Hrs. min.
Tc= 125°C
Life Test: 1000 Hrs.
Read Points:
0,168,500,1000

PACKAGE CONFIGURATION

40 PIN CERAMIC DIP (SIDE BRAZED)







Notes:

1. Pins are gold-plated Kovar or Alloy 42
2. Cap is gold-plated Kovar or Alloy 42
3. Base is Al_2O_3
4. Pins are intended for insertion in hole rows on 0.600" centers
5. Package material is Ceramic
6. Board drilling dimensions should equal 0.020" diameter pin

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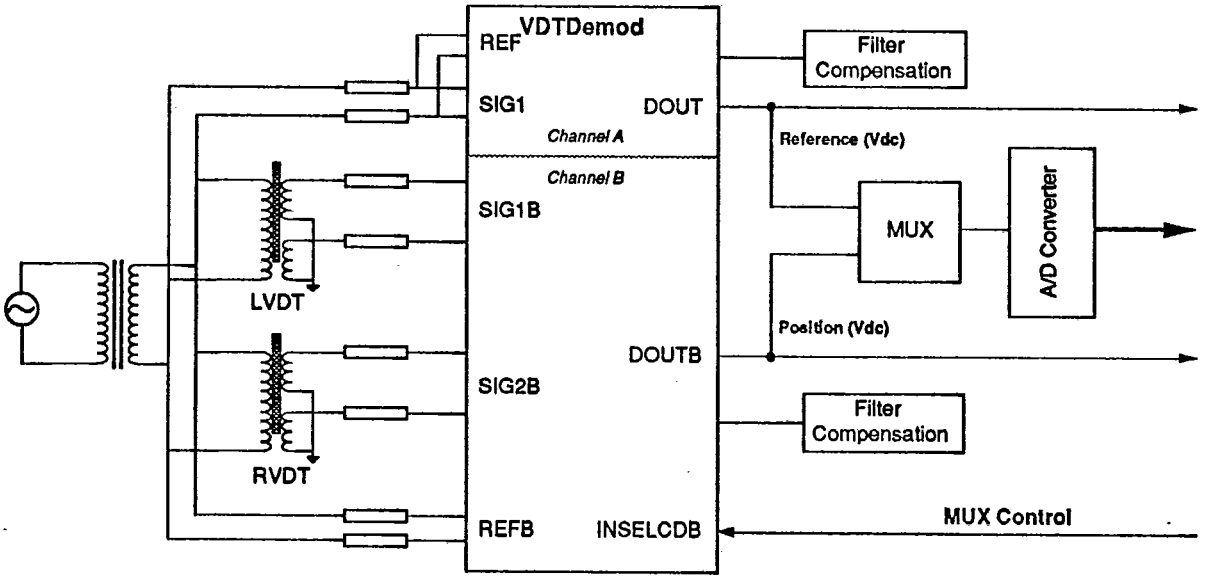
TYPICAL APPLICATION

The diagram below illustrates an application of the VDTDemod in a Linear Variable Differential Transformer (LVDT) and a Rotary Variable Differential Transformer (RVDT) configuration. The VDTDemod in this application replaces many discrete components compared to traditional systems of the same type.

A transducer excitation signal is supplied to both the linear and rotary transducers. Each transducer produces a signal based on the reference and the position of the core within the transducer. Using the VDTDemod, four seperate input signals can be processed. In this example, linear and rotary motion from two different transducers are multiplexed through Channel B. Channel A is dedicated to demodulating the excitation level for ratiometric compensation. The output signals from the VDTDemod can be multiplexed as shown to make more efficient use of a single analog to digital converter. The VDTDemod is also equipped with two uncommitted operational amplifiers. These operational amplifiers typically are used to filter/condition the output signals. The VDTDemod allows designers to fully integrate and test the LVDT/RVDT interface electronics in the system application.



Application showing the Reference signal on Channel A and a LVDT and RVDT multiplexed on Channel B

For more information on the VDTDemod contact:

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