TECHNICAL MANUAL

E-1110
10/100/1000 Mbits/s Ethernet MAC

Preliminary

April 2001

LSI LOGIC®

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This document is preliminary. As such, it contains data derived from functional simulations and performance estimates. LSI Logic has not verified either the functional descriptions, or the electrical and mechanical specifications using production parts.

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This document describes LSI Logic Corporation's E-1110 10/100/1000 Mbits/s Ethernet MAC and will remain the official reference source for all revisions/releases of this product until rescinded by an update.

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Preface

This manual is the primary reference for the Ethernet-1110 (E-1110) core. The E-1110 includes the Media Access Controller (MAC) core for Gigabit Ethernet, the Flow Control module for 10/100 Mbits/s Ethernet operation, and a common Host Interface module that allows both the Gigabit MAC and Ethernet-110 (E-110) core to interface to a host. The E-1110 provides a complete 10/100/1000 Ethernet MAC solution. The manual also contains a functional description for the E-1110 core and complete electrical and physical specifications. Details for E-110 core operation and signals are found in the *Ethernet-110 Core Technical Manual*.

Audience

This manual assumes that you have complete familiarity with Ethernet protocols and related support devices. It also assumes that you are familiar with the IEEE 802.3 standard and all applicable clauses describing Gigabit operation. The people who benefit from this manual are:

- Engineers and managers who are evaluating the E-1110 core for possible use in ASIC applications
- Engineers who are designing the E-1110 core into an ASIC.

Organization

This document has the following chapters:

- Chapter 1, **Introduction**
- Chapter 2, **Functional Description**
- Chapter 3, **Signals**
- Chapter 4, **Functional Timing**
- Chapter 5, **Specifications**

Related Publications

- *IEEE 802.3z MAC Parameters, Physical Layer, Repeater and Management Parameters for 1000 Mbits/s Operation*.
- *IEEE 802.3 and 802.3u (for 10/100 Mbits/s operation*.)
- *Ethernet-110 Core Technical Manual*, Order Number R14004.B

Conventions Used in This Manual

The first time a word or phrase is defined in this manual, it is *italicized.*

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive. Signals that are active-LOW end in an “n.”

Hexadecimal numbers are indicated by the prefix “0x” —for example, 0x32CF. Binary numbers are indicated by the prefix “0b” —for example, 0b0011.0010.1100.1111.

Contents

Chapter 1
Introduction

This chapter provides an overview of the E-1110 10/100/1000 Mites/s Ethernet MAC and lists its features. This chapter contains the following sections:

- Section 1.1, “General Description”
- Section 1.2, “Applications”
- Section 1.3, “Features”

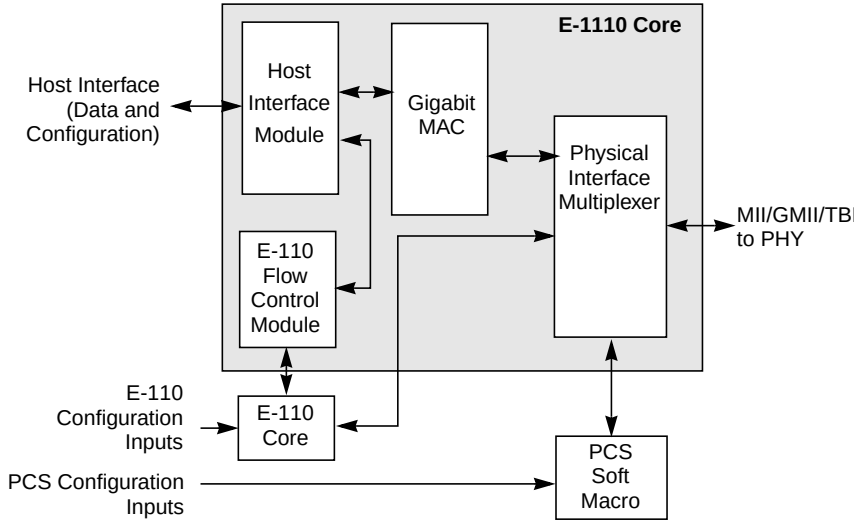
1.1 General Description

The E-1110 core 10/100/1000BASE-T/TX MAC solution is capable of operating in Fast Ethernet or Gigabit Ethernet modes. The E-1110 core provides a single platform to support applications requiring speeds of 10, 100, and 1000 Mbits/s.

The E-1110 core consists of a Gigabit Ethernet MAC, a Flow Control Module for the E-110 core, a Physical Interface Multiplexer, and a common Host Interface Module. An interface is provided that allows easy connection to an external E-110 core. Typically, the E-1110 core supports only a Media Independent Interface (MII) or a Gigabit Media Independent Interface (GMII). If a Serial Media Independent Interface (SMII) is required, the Physical Interface Multiplexer must be bypassed in the core and an external multiplexer added for SMII.

For Ten-Bit Interface (TBI) support, a Physical Coding Sublayer (PCS) soft macro must be added outside the E-1110 core. If only Gigabit operation is desired, all the E-110 related signals can be tied LOW. If complete 10/100/1000 functionality is desired, the E-1110 core must be connected to the E-110 core. Figure 1.1 is a block diagram of the core, showing the connections to the external PCS soft macro and E-110 core.

Figure 1.1 E-1110 Block Diagram



1.2 Applications

The E-1110 fits applications in:

- 10/100/1000 Mbits/s capable node cards
- Switches with 10/100/1000 Mbits/s capable ports
- High speed uplink ports (backbone)

1.3 Features

The E-1110 core has the following features:

- Complete 10/100/1000 Mbits/s solution, from the host processor interface to the PHY interface (MII, GMII, or fiber TBI).
- MAC Layer IEEE 802.3 compliant.
- Programmable 10/100/1000 Mbits/s data rate.
- Half-duplex operation in 10/100 Mbits/s mode and full-duplex operation (only) in 1000 Mbits/s mode.

- Huge frame support (up to 10,000 bytes per frame).
- Programmable maximum packet size (1518, 1522, or unlimited). Unlimited is up to 9,000 bytes.
- IEEE 802.3 compliant flow control (Symmetric/Asymmetric pause frame control).
- VLAN frame support (detection).
- Statistics vector support for remote monitoring (RMON).
- Option to accept or discard pause frames.
- Programmable autopadding of frames less than 64 bytes on transmit.
- Programmable interpacket gap (IPG).
- Indicator for multicast/broadcast/unicast addresses.
- Programmable option to append a CRC and Preamble.
- Programmable option to send frames without a Preamble.
- Programmable option to strip CRC upon receive.
- LSI Logic G12™-p CMOS process.

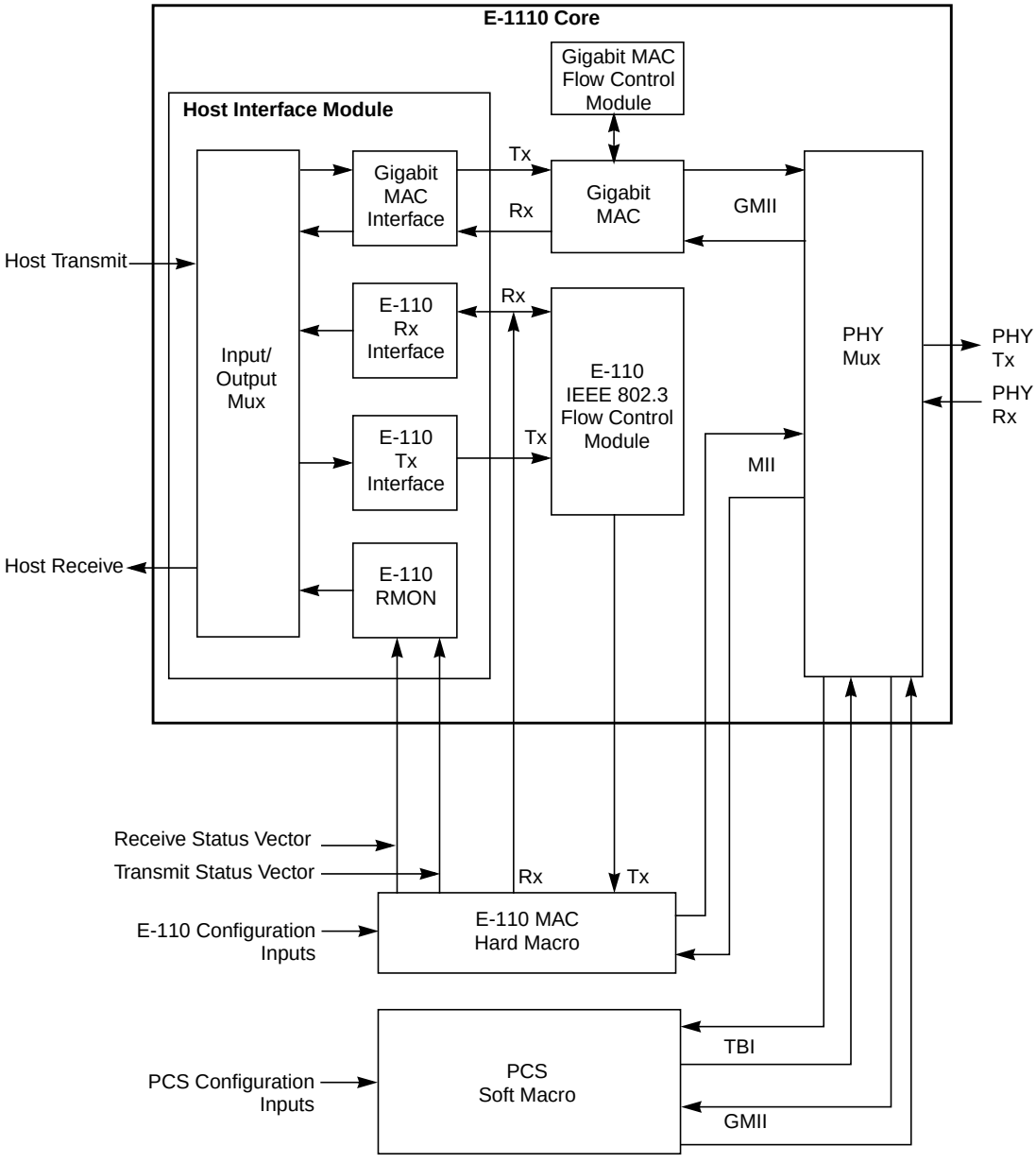
Chapter 2
Functional Description

This chapter describes the functional blocks and operation of the E-1110. The chapter contains the following sections:

2.1 E-1110 Core Functional Description

This section describes in detail the operation of the functional blocks in the E-1110 core. A block diagram of the core is shown in Figure 2.1.

Figure 2.1 E-1110 Block Diagram



As shown in the block diagram (Figure 2.1), the E-1110 core consists of the following blocks:

- Host Interface Module
- Gigabit MAC
- Gigabit MAC Flow Control Module
- E-110 Flow Control Module[1]
- Physical Interface Multiplexer

2.1.1 Host Interface Module

The Host Interface module provides an 8-bit, 125 MHz interface that allows the host to communicate with the E-110 MAC core, the E-110 Flow Control module, and the Gigabit MAC. The Host Interface module contains the required buffers and FIFOs to transfer data to and from the E-110 core at 2.5 MHz or 25 MHz as well as to manage data transfers to the Gigabit MAC at 125 MHz. The Host Interface module also contains all the required multiplexing and demultiplexing logic for the interface signals. In addition, the Host Interface module reads the remote monitoring (RMON) vector from the E-110 MAC core and converts it into a detailed RMON vector similar to the one the Gigabit MAC generates.

The Gigabit MAC has an 8-bit, 125 MHz interface. The Host Interface module buffers the data transferred to and from the Gigabit MAC and remaps the control interface protocol defined in the E-1110 packet interface (start of packet, data valid, end of packet, and acknowledge). The signals are then multiplexed with the related data and control signals coming from the E-110. The result is that the host sees common start of packet, data valid, end of packet, and acknowledge signals whether they originate with the E-110 or the Gigabit MAC. The RMON vectors from the E-110 core and the Gigabit MAC are also multiplexed into a single RMON vector as described in Chapter 3, “Signals.” The host interface thus provides the same look and feel for the data and packet transfer control protocol for both the E-110 core and the Gigabit MAC.

The E-110 core transfers data to and from the Host Interface module over an 8-bit interface using a 2.5 or 25 MHz MII clock. The receive data

1. Please refer to the E-110 documentation for more details on the operation of the E-110 Flow Control module.

from the E-110 is written to a small, 4-deep, 4 x 8 FIFO structure using the 2.5/25 MHz MII receive clock. The data is then read out of the FIFO using the 125 MHz host interface clock. The receive state machine controls the FIFO and remaps the packet transfer protocol from the E-110 to the E-1110. The state machine also implements a strip CRC function that is not supported in the E-110 hard macro such that the feature set for the E-110 and the Gigabit MAC are mapped one-to-one. Besides providing the data and control interface logic, the Host Interface module also generates a new RMON vector for the E-1110 from the E-110 RMON vector and maps it exactly to the RMON vector generated from the Gigabit MAC.

To interface to the transmit MAC engine of the E-110, the Host Interface module uses a ping-pong buffer concept to ensure that the data is properly synchronized to the 10/100 transmit MAC interface and the MAC is never starved of any data during the packet transfer. The transmit interface state machine handles the control protocol translation from the E-110 transmit packet control protocol (E110_TPSF, E110_TPEF, and E110_TPUD to MTX_SOP, MTX_DVALID, and MTX_ACK, respectively) to the E-1110 transmit packet interface protocol.

The RMON vector from the E-110 is latched and synchronized to 125 MHz. A common multiplexed RMON vector is output to the host interface over the RMON status vector pins of the E-1110.

The Host Interface module thus provides a common interface to the system that hides the underlying MACs. The host then sees a single set of clock and interface signals, even though the underlying MAC is either the E-110 core operating at 10/100 Mbits/s or the Gigabit MAC operating at 1000 Mbits/s.

2.1.2 Gigabit MAC Transmit Control Block

The Gigabit MAC transmit control block provides all of the logic required to implement IEEE 802.3-compliant frame transmission. Data is accepted from the host transmit interface through the Host Interface Module using a synchronous handshake, processed through MAC data encapsulation and frame assembly, and then delivered to the MAC GMII interface for synchronous transfer to the PHY. The process of frame assembly includes the attachment of preamble, start of frame delimiter, destination address, source address, length, frame check sequence verification and generation.

The Gigabit MAC transmit function does not provide IEEE 802.3 compliant transmit media access management services such as carrier deference, interframe spacing, collision handling, collision detection, collision enforcement, collision backoff, or retransmission due to half-duplex operation. The Gigabit MAC supports only the full-duplex mode of operation. The transmit function enforces minimum frame size, including the required padding function for small frames. The transmit function also takes the programmed preamble length for preamble generation during frame assembly. The preamble length provides the length of the preamble in terms of octets, including the start of frame delimiter (SFD). The MTX_NOPRE signal, when asserted, causes the transmit function to skip the preamble and SFD generation during frame assembly.

The transmit function does not specifically calculate and maintain MAC transmit statistics. The Gigabit MAC module does provide a transmit statistics output vector, which is a set of status and error signals that external logic can use to calculate and maintain transmit statistics.

Autopadding, when enabled, causes frames less than 60 bytes long to be padded with zeros. In the Gigabit MAC, frames with 60 to 63 bytes are appended with a cyclic redundancy code (CRC) and frames with 64 or more bytes are transmitted as is. In 10/100 mode, frames of 60 bytes or more are always appended with a valid CRC value.

The 10/100 MAC checks for a CRC in the transmit frame when the append CRC function is not enabled, and flags a CRC error if it does not find a valid frame check sequence (FCS) at the end of the packet. This is true when a undersized packet is to be transmitted from the 10/100 MAC that has padding enabled but append CRC is disabled. In the Gigabit MAC, the CRC is checked only for packets where it does not append the CRC. If the padding is enabled and the packet is smaller than 64 bytes, the CRC is not checked.

Another difference between the 10/100 MAC and the Gigabit MAC in transmit operation concerns the maximum packet length. The 10/100 MAC truncates packets whose length exceeds the programmed maximum packet length in the huge mode. The Gigabit MAC transmit function ignores the maximum packet length and keeps transmitting the frame as long as the host keeps sending data.

2.1.2.1 Gigabit MAC Transmit Block Functional Description

The Gigabit MAC transmit function complies with the IEEE 802.3 standard. This section provides a detailed functional description of the Gigabit MAC transmit block.

Frame Transmission Model – The Gigabit MAC frame transmission model complies with the IEEE 802.3 standard. The Gigabit MAC transmit function consists of the transmit data encapsulation function and the transmit media access management function.

Transmit Data Encapsulation and Frame Assembly – The Gigabit MAC transmit data encapsulation and frame assembly function complies with the IEEE 802.3 standard. The Gigabit MAC transmit function assembles outgoing transmit frames from the fields provided from the host transmit frame structure and the frame check sequence generator. The transmit frame is assembled from the preamble, start of frame delimiter, destination address, source address, link layer control (LLC) data, padding (if required), and frame check sequence fields.

Frame Check Sequence Generation – The Gigabit MAC frame check sequence generation function complies with the IEEE 802.3 standard. The Gigabit MAC transmit function generates and optionally inserts the IEEE 802.3 standard FCS into transmit frames. The Gigabit MAC frame check sequence is generated using a 32-bit CRC algorithm. The FCS calculation includes the destination address, source address, length, LLC data, and pad (if any) fields. In cases where the Gigabit MAC does not append the FCS at the end of frame, the MAC then compares the frame FCS with the calculated FCS. If there is a miscompare, the Gigabit MAC flags an error using the transmit RMON vector.

Transmit Media Access Management – The Gigabit MAC transmit media access management function complies with the IEEE 802.3 standard. The Gigabit MAC transmit media access management function includes carrier deference, interframe spacing, collision handling, collision detection and enforcement, and collision backoff and retransmission functions. The required functions are detailed below.

- Carrier Deference. Not supported because the Gigabit MAC operates in the full-duplex mode.

- Interframe Spacing. The Gigabit MAC interframe spacing function complies with the IEEE 802.3 standard. The interframe gap is required to allow the proper recovery time between frames for physical layer components and the medium. The Gigabit MAC supports the basic back-to-back transmit interframe gap (IFG). The IEEE 802.3 standard requires an interframe gap of 0.096 μs for back-to-back transmits.
- Collision Handling and Slot Time. The transmit function operates in full-duplex mode, which means it does not defer to the CRS signal and does not respond to the COL signal.
- Collision Detection and Enforcement. Not supported because the Gigabit MAC operates in the full-duplex mode.
- Collision Back Off and Retransmission. Not supported because the Gigabit MAC operates in the full-duplex mode.

Minimum Frame Size and Padding – The Gigabit MAC minimum frame size and padding function complies with the IEEE 802.3 standard. The carrier sense multiple access collision detect (CSMA/CD) media access protocol for shared media requires that a minimum frame size be enforced. Host frames that are presented to the Gigabit MAC with a length of less than the minimum frame size in bits are optionally padded with bytes of arbitrary data to produce a frame of the minimum required length. The padding is appended after the LLC data field but prior to the calculation and appending of the FCS. The number of bytes of padding must be sufficient to ensure that the frame as counted from the destination address field through the FCS field inclusive be of at least the minimum frame size in bits. The IEEE 802.3 standard requires that the minimum frame size parameter be set to 64 bytes (512 bits). The padding option is turned on when the MTX_APPEND_CRC signal is asserted.

Preamble Generation and Start Of Frame Sequence – The Gigabit MAC preamble generation and start of frame sequence functions comply with the IEEE 802.3 standard. The Gigabit MAC upon request from the host, transmits a preamble and start of frame sequence that complies with the IEEE 802.3 standard. The preamble and start of frame sequence is designed to allow the physical layer (PHY) circuitry at receiving stations to acquire both bit and symbol level synchronization to the receive data stream. The preamble length and whether the preamble

and SFD insertion is required or not can be optionally controlled from the host with the MTX_NOPRE signal.

IEEE 802.3 Carrier Extension – Not supported because the Gigabit MAC operates in the full-duplex mode.

IEEE 802.3 Frame Bursting – Not supported because the Gigabit MAC operates in the full-duplex mode.

Transmit Statistics Generation – The Gigabit MAC transmit statistics generation function complies with the IEEE 802.3 standard. The Transmit Status Vector[40:0] (MACTX_STATUS[40:0]) output bus contains transmit statistics information presented on a frame-by-frame basis. The E-1110 MAC transmit function updates the MACTX_STATUS[40:0] output bus on the rising edge of the TX_STATUS_ACTIVE output signal. The E-1110 MAC issues a transmit statistics vector update at the end of the final or only attempt to transmit each frame. The MACTX_STATUS[40:0] signals remain stable until the subsequent rising edge of the TX_STATUS_ACTIVE output. The condition associated with each signal is valid when the signal is asserted HIGH.

The MAC transmit function provides transmit statistics that can be used for the RMON and simple network management (SNMP) protocols. However, the MAC does not collect the statistics specifically mentioned in the RMON and SNMP standards specifications. The MAC only provides the basic per frame information that can be collected with an application built on top of the E-1110 core. The collected information can then be used for RMON and SNMP statistics.

2.1.2.2 Gigabit MAC Transmit Sequence

A packet transmission from the host begins when the host asserts the MTX_SOP and MTX_DVALID signals and drives valid the MTX_DATA[7:0] signal lines to the E-1110 core. When this occurs, the E-1110 recognizes a valid packet transfer and in turn sends the data to the Gigabit MAC or E-110 MAC, depending on the speed of operation.

Gigabit Mode – In the Gigabit mode, the data along with the start of frame information is sent to the Gigabit MAC. The Gigabit MAC then begins sending the preamble and SFD on the GMII bus after adding the required programmed IPG. If the core is configured for TBI mode, the GMII signals are routed to the PCS module. The PCS then encodes the

GMII data into an 8B/10B TBI stream and sends it back to the E-1110 PHY Multiplexer. The E-1110 PHY Multiplexer then sends out the TBI signals to the PHY device. In the GMII mode, the GMII signals from the Gigabit MAC are sent to the PHY device through the PHY Multiplexer. The Gigabit MAC asserts the MTX_ACK signal on every clock to start responding to the host interface for more data after sending the preamble and SFD. The host outputs new data on every clock when MTX_ACK is sampled active. The end of packet is indicated when the host asserts the MTX_EOP signal. If a transmit underrun occurs, the Host Interface Module generates the MTX_ABORT signal to the host to abort the rest of the transmit data transfer.

10/100 Mode – In 10/100 mode, the data is sent to the E-110 MAC through the assertion of the E110_TPSF signal. The E-110 core transmits the preamble and SFD after properly adding the required IPG and then asserts E110_TPUD to start the next data transfer. Subsequently, the E-110 expects valid data every alternate clock until the end of the packet. The E-1110 core appropriately asserts MTX_ACK to get the next byte from the host interface. The assertion of MTX_ACK is not continuous in the 10/100 mode due to the lower speed of operation. The host packet interface is designed to operate at a speed of 1 Gbit/s. In 10/100 mode, due to handshake of MTX_DVALID and MTX_ACK, this interface operates at the required 1/100 or 1/10 speed, depending upon the 10/100 mode of operation. If a collision occurs, the E-110 core asserts the E110_TPRT signal, which is synchronized and asserted as MTX_RETRY. The host then can retry the packet transmission. If an abort condition occurs (late collision, excess collisions, or transmit underrun), the E-110 core asserts TPAB, which is synchronized and asserted as MTX_ABORT. The host then can abort the current transmission attempt. In the case of an underrun, the E-1110 core detects the underrun condition and asserts E110_TPUR to the E-110 core. All the configuration signals except those mentioned in the Signals chapter are directly connected from the host interface to the E-110 core.

The MII input and output signals from the E-110 core are fed back into the E-1110 core, where they are multiplexed and sent out over the PHY interface in the MII mode.

The E-1110 then asserts TX_STATUS_ACTIVE along with MACTX_STATUS[40:0] as a RMON vector.

2.1.3 Gigabit MAC Receive Control Block

The MAC receive block provides all of the logic required to implement IEEE 802.3-compliant frame reception and filtering. Data is accepted from the GMII interface using a synchronous handshake, processed through MAC data decapsulation and frame disassembly, and then delivered to the host interface, through the Host Interface Module for synchronous transfer to the host receive data buffer. The process of frame decapsulation and disassembly includes stripping the preamble and the start of frame delimiter and optionally stripping the CRC.

The MAC receive function provides IEEE 802.3-compliant receive media access management services such as frame reception, receive data decapsulation, frame disassembly, frame check sequence validation, and framing detection. The receive function also enforces minimum and maximum frame sizes, including the required padding function for small frames.

The receive block does not specifically calculate and maintain MAC receive statistics. The Gigabit MAC does provide a receive statistics output vector. The receive statistics output vector is a set of status and error signals that external logic can use to calculate and maintain receive statistics.

The common RMON vector for 10/100 and 1000 modes is output through the MACRX_STATUS[41:0] lines at the end of reception of the frame.

The ACCEPT_CRC, ACCEPT_RUNT, ACCEPT_LONG, and ACCEPT_CTRL signals only cause the REJECT bit (RSXV36) to be set under specified error conditions. The MAC does not drop or pass any received frame on its own. All the received frames are passed to the host as is, including collision frames in 10/100 half-duplex mode. The host looks at the RMON vector at the end of the frame to make the decision whether to drop or pass the frames.

2.1.3.1 Gigabit MAC Receive Block Functional Description.

The Gigabit MAC receive block complies with the IEEE 802.3 standard. This section provides a detailed functional description of the Gigabit MAC's receive block.

Frame Reception Model – The Gigabit MAC frame reception model complies with the IEEE 802.3 standard. The frame reception function consists of the receive media management function and the receive data decapsulation function.

Receive Data Decapsulation – The Gigabit MAC receive data decapsulation function complies with the IEEE 802.3 standard. The receive data decapsulation function consists of the address recognition function, the frame check sequence validation function, and the frame disassembly function.

Address Recognition – The Gigabit MAC address recognition function complies with the IEEE 802.3 standard.

IEEE 802.3 Standard Address Recognition Requirements – The IEEE 802.3 standard calls for a MAC Sublayer to recognize both individual, group, and broadcast addresses. The MAC Sublayer has the following requirements:

- Recognize and accept any frame whose destination address field contains the individual or unicast address of the station.
- Recognize and accept any frame whose destination address field contains the broadcast address.
- Recognize and accept any frame whose destination address field contains an active group address.
- Be capable of activating and deactivating multiple group addresses.

Gigabit MAC Address Recognition – The Gigabit MAC address recognition function complies with the IEEE 802.3 standards. The Gigabit MAC can provide the MAC level address recognition functions required by the IEEE 802.3 standard.

The Gigabit MAC host receive function interface provides the required handshaking logic signals, detailed below, to support detection and latching of the receive frame's destination address field. Outputs are also provided that indicate the destination address type. Individual, group, and broadcast address types are supported.

The Receive Status Vector (MACRX_STATUS[41:0]) outputs provide a vector similar to the transmit function for generation of RMON/SNMP statistics.

Frame Check Sequence Validation – The Gigabit MAC frame check sequence function complies with the IEEE 802.3 standard. The Gigabit MAC's receive function validates the frame check sequence field of an incoming frame with a logic function identical to that used in the transmit function. The resulting value should be identical to that found in the frame FCS field of the incoming frame. If the two FCS values are not identical, the received frame is invalid and should be discarded.

Frame Disassembly – The Gigabit MAC frame disassembly function complies with the IEEE 802.3 standard. When the frame disassembly function detects the start of frame (SOF) delimiter at the end of the preamble sequence, the MAC's receive function accepts the frame, and if there are no errors, passes it to the host by means of the receive function interface with a synchronous handshaking protocol. The frame disassembly function strips the preamble and start of frame delimiter fields from the received frame. The destination address, source address, length, LLC data, and optionally FCS fields are delivered to the host.

Receive Media Access Management – The Gigabit MAC receive media access management function complies with the IEEE 802.3 standard. The receive media access management function consists of the framing function and the collision filtering function.

Framing – The Gigabit MAC framing function complies with the IEEE 802.3 standard. The framing function monitors the received data stream for length errors that may indicate a framing error. Frames that exceed the MAX_PKT_LEN[15:0] threshold when HUGE_PKT_EN is active are considered to be of erroneous length.

The MAX_PKT_LEN[15:0] input bus indicates to the Gigabit MAC receive function the size or value of the receive frame threshold. The MAX_PKT_LEN[15:0] threshold is used for receive frame rejection of long frames and for statistics generation of oversize and jabber frames. The MAX_PKT_LEN[15:0] input bus is synchronous to the rising edge of the CLK125 signal. IEEE 802.3-compliant operation requires the value of the MAX_PKT_LEN[15:0] input bus to be set to 1518.

The ACCEPT_LONG input signal, when asserted, instructs the Gigabit MAC's receive function to accept frames longer than the value specified by the MAX_PKT_LEN[15:0] threshold. However, all frames longer than the maximum packet length are truncated and the MAC considers them to be jabber frames. When deasserted, the ACCEPT_LONG input signal

instructs the Gigabit MAC receive function to reject frames longer than the value specified with the MAX_PKT_LEN[15:0] threshold. The ACCEPT_LONG input signal is synchronous to the rising edge of the RX_CLK output signal.

In the E-110 MAC and the Gigabit MAC, when huge mode is disabled, the frame cutoff occurs at 1536 bytes. All the frames between 1518 or 1522 to 1536 are considered to be oversized frames. If VLAN is enabled and the received frame is a valid VLAN frame, the frame size threshold is changed to 1522 automatically and only frames larger than 1522 are considered to be oversized frames. However, in huge mode, the VLAN_EN signal has no effect on the allowed frame size. The system design needs to allocate a buffer of four extra bytes for VLAN frames.

When the Gigabit MAC receives a frame with the ACCEPT_LONG input signal deasserted, the OVERSIZE bit (RXSV27) of the Receive Status Vector (MACRX_STATUS[41:0]) output bus is asserted when the chosen MAX_PKT_LEN[15:0] threshold is just crossed or exceeded. The frame is truncated at a the maximum packet length + 1 bytes. Any frame larger than this is considered to be a jabber frame.

Collision Filtering – Not Required in the full-duplex mode.

Preamble Reception and Start Of Frame Sequence – The Gigabit MAC preamble generation and start of frame sequence function complies with the IEEE 802.3 standard. The Gigabit MAC, upon request from the host, transmits a preamble and start of frame sequence that complies with the IEEE 802.3 standard. The preamble and start of frame sequence is designed to allow the PHY of a receiving station to acquire both bit and symbol level synchronization with the receive data stream.

The Gigabit MAC receive function recognizes and properly receives otherwise good frames, with preamble lengths of as little as zero bytes, followed with a properly formed start of frame delimiter.

Receive Statistics Generation – The Gigabit MAC receive statistics generation function complies with the IEEE 802.3 standard. The Receive Status Vector (MACRX_STATUS[41:0]) output bus contains the receive statistics vector and is updated on rising edges of the RX_STATUS_ACTIVE signal. The statistics vector is issued at the end of any minimally qualified receive event. A minimally qualified receive event

occurs when the MAC receives at least one byte of data beyond a valid preamble and SFD symbol sequence.

The receive statistics provided through the MAC receive function can be used for RMON and SNMP support. However, the MAC does not collect the statistics specifically mentioned in the RMON and SNMP standard specifications. The MAC provides the basic per frame information that can be collected with an application built on top of the MAC. The collected information can then be used for RMON and SNMP support.

Gigabit MAC Bit Budget – Not Required in the full-duplex mode.

2.1.3.2 Gigabit MAC Receive Sequence

Gigabit Mode – The Gigabit MAC always receives data over the GMII interface. In the TBI mode, the data is received from the PHY interface through the PHY Multiplexer and sent to the PCS block. The PCS then outputs the data after 8B/10B decoding to the Gigabit MAC over the GMII interface. The Gigabit MAC detects the preamble and SFD according to IEEE 802.3. It then sends the frame without the SFD and preamble to the host through the host interface module. The MRX_SOP signal indicates the start of packet. The MRX_DVALID signal indicates the validity of data and MRX_EOP indicates the end of packet. The E-1110 core needs an MRX_ACK transition for every MRX_DVALID. If MRX_DVALID is asserted and MRX_ACK is not received on the same clock, the Gigabit MAC assumes an underrun condition and aborts the receive operation. Similarly, the host can assert MRX_ABORT to abort the receive operation. The Gigabit MAC checks the CRC value and checks for error conditions according to the IEEE 802.3 protocol.

A new RMON vector is output at the end of the receive operation through assertion of RX_STATUS_ACTIVE and an update of MACRX_STATUS[41:0].

10/100 Mode – In the 10/100 mode, the E-1110 PHY interface is configured in the MII mode. The demultiplexed signals are output over the MII bus to the E-110 core, which receives the frame and starts sending it to the E-1110 core. The E-1110 core detects the start of a new frame from the E-110 and asserts MRX_SOP and MRX_DVALID on the host packet interface. The E-110 outputs data on every alternate E110_MRXC clock cycle to the E-1110. The E-1110 synchronizes the data to the host clock and sends it over the host interface with assertion

of MRX_DVALID. The assertion of MRX_DVALID is used to adjust the transfer rate of the host bus. The host packet interface is designed to operate at 1 Gbit/s. With the combination of MRX_DVALID and MRX_ACK, the transfer rate is controlled to 1/10 or 1/100 depending on the 10 or 100 Mbits/s mode of operation. The MRX_EOP indicates the end of packet. The packet overflow condition is caused when the E-1110 detects MRX_DVALID asserted with MRX_ACK deasserted. The Gigabit MAC aborts the packet reception upon detecting an overflow condition. Similarly, the host can assert the MRX_ABORT to abort receive operation.

The Gigabit MAC asserts RX_STATUS_ACTIVE and updates MACRX_STATUS[41:0] to output a new RMON vector at the end of the receive operation.

All the input and output signals between the E-1110 core and the host are synchronous to the CLK125 clock signal.

Whenever Gigabit mode is selected, the E-110 core is held reset. However, it may not receive clocks due to the multiplexing of clocks on the PHY interface. Similarly, when the E-1110 core is configured for 10/100 mode, the Gigabit MAC is held reset.

In the scan-test mode, all the input clocks are always routed out to their output pins.

2.1.4 Gigabit MAC Flow Control Module

The Gigabit MAC Flow Control module provides the logic required to implement an IEEE 802.3-compliant flow control scheme based on transmission and reception of pause frames. The design supports IEEE 802.3 full-duplex operation while maintaining 1000 Mbits/s IEEE 802.3 standard compliance. Both symmetric and asymmetric flow control are supported.

The implementation of IEEE 802.3 flow control requires the ability to receive, process, and transmit pause frames. The Gigabit MAC Flow Control module can receive pause frames, recognize their meaning, parse the control fields, and use the resulting information to control the MAC transmit function. Upon reception and processing of a pause flow control frame, the Gigabit MAC Flow Control module implements the required pause. The MAC flow control block implements the pause timer

function, which, upon timeout, allows the MAC transmit function to restart. The Gigabit MAC Flow Control module also implements a control input signal that allows the receiver to ignore and drop pause frames. This control function is required because the use of the pause function is network topology dependent. A network interface card (NIC) is required to act on pause frames, while a switch may ignore them except for switch-to-switch links.

The host controls transmission of IEEE 802.3 pause flow control frames. The host assembles and formats the frames, including the calculation and insertion of the pause time value in units of slot time. Once assembled, the pause frames are transmitted by means of the host transmit function interface similar to any normal host data frame. The host may assert the MTX_HIGH_PRIORITY input signal to expedite timely transmission of pause flow control frames. Alternatively, the MAC can assemble and send flow control frames through transmit flow control operation.

The high priority (MTX_HIGH_PRIORITY) input signal, when asserted, instructs the MAC transmit function to transmit the requested frame regardless of the pause state of the transmit function. The MTX_HIGH_PRIORITY input signal is sampled during the CLK125 clock cycle when the MTX_SOP input signal is asserted. The MTX_HIGH_PRIORITY input signal is synchronous with the rising edge of the CLK125 output signal.

When the receive enable pause (FLCTRL_CFG[1]) input signal is asserted, the Gigabit MAC's IEEE 802.3 receive flow control scheme is enabled. When the flow control block receives a properly formatted pause control frame from the MAC's receive function, the pause timer is started and frame transmission pauses. The transmit function remains in the pause state until the pause timer expires, at which time normal frame transmission resumes. When the Accept Control Frames (ACCEPT_CONTROL) input signal is asserted, MAC passes all received IEEE 802.3 flow control pause frames to the host by means of the host receive function interface. When the ACCEPT_CONTROL signal is deasserted, the MAC asserts the REJECT bit (RXSV36) in the receive status to filter all IEEE 802.3 flow control pause frames that are received at the receive function interface. The MAC also provides the DA_MATCH signal along with the status to indicate that the received pause control frame has a destination address match for the unicast or reserved multicast address for the pause frames.

The E-1110 core outputs the following pause frame qualifiers:

- A MAC Control Frame has been received
- Whether the Control Frame has a proper opcode
- Whether the Control Frame has a destination address match for global reserved multicast address or programmed unicast destination address

The rest of the frame status is also sent along with the RMON vector. When the pause frame is received, the MAC checks for frame integrity through valid length and good CRC. It checks for a destination address match for the reserved multicast address 01-80-C2-00-00-01, or a preprogrammed unicast address on the MAC_ADDRESS[47:0] lines.

Flow control operation is controlled through the FLCTRL_CFG[1:0] configuration signals. The FLCTRL_CFG[1] signal, when set, enables the reception of pause frames and configures the MAC for entering in a paused state upon reception of valid pause frames.

Transmit flow control enables the Gigabit MAC Flow Control module to assemble and transmit pause frames upon assertion of the FLOWCTRL_EN signal. When this signal is asserted, a pause frame with the pause time contained in PAUSE_TIME[15:0] is transmitted at the first earliest opportunity. When FLOWCTRL_EN is deasserted, a pause frame with a pause time of zero is transmitted. With the transmission of a pause frame, the Gigabit MAC Flow Control module starts a mirrored pause time timer. If the FLOWCTRL_EN signal is still asserted and the pause timer is about to expire, the transmit flow control function transmits another pause frame before the pause timer actually expires. This function is enabled when the FLCTRL_CFG[0] signal is HIGH.

In half-duplex 10/100 mode, backpressure must be used instead of pause frames. The host asserts the E110_BACKPRESS signal to accomplish this. As long as the E110_BACKPRESS signal is asserted, the 10/100 MAC continually sends out false carrier over the media.

2.1.5 Physical Interface Multiplexer

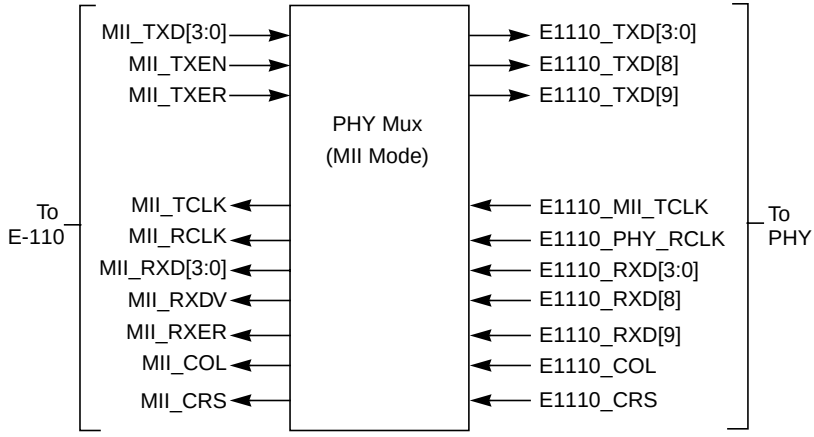
The Physical Interface Multiplexer (PHY MUX) multiplexes the PHY interface signals and provides a unified overlapped set of signals that assumes different meaning depending on the mode of operation (GMII, MII, or TBI). The purpose for multiplexing the MII, GMII and TBI signals into a single overlapped set of signals is:

- To reduce the number of I/O pins
- To close the timing constraints and meet all of the stringent timing requirements for modes such as GMII
- Provide a single set of pins that can assume any interface based on the configuration of a few control signals.

2.1.5.1 MII Mode

The MII mode is used when the E-110 core needs to communicate with an MII-compatible external PHY. Figure 2.2 is a diagram of the signal flow through the PHY multiplexer mapping when it is operating in the MII mode.

Figure 2.2 PHY Multiplexer Signal Mapping in MII Mode



In MII Mode, the E-110 MII_TXD[3:0], MII_TXEN, and MII_TXER signals are mapped to the PHY E1110_TXD[3:0], E1110_TXD[8], and E1110_TXD[9] pins, respectively. The E1110_MII_TCLK transmit clock and the E1110_PHY_RCLK are each separate input pins on the E-1110 core. Similarly, the PHY E1110_RXD[3:0], E1110_RXD[8],

E1110_RXD[9], E1110_CRS, and E1110_COL signals are demultiplexed and mapped onto the E-110 MII_RXD[3:0], MII_RXDV, MII_RXER, MII_CRS, and MII_COL pins, respectively. In addition to the multiplexing and demultiplexing of the signals, the PHY Mux also maintains the same timing relationship for all incoming and outgoing MII signals when operating in the MII mode.

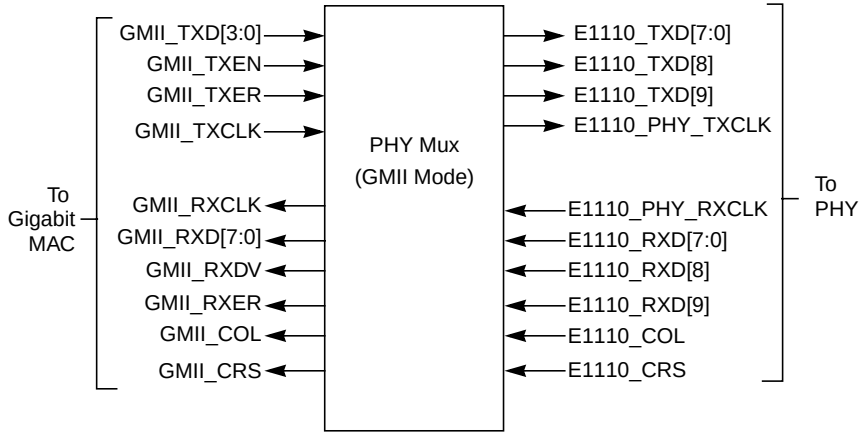
2.1.5.2 GMII Mode

The GMII mode is used when the Gigabit MAC needs to communicate with an external GMII-compatible PHY. Figure 2.2 is a diagram of the signal flow through the PHY multiplexer when it is operating in the GMII mode.

When operating at 1000 Mbits/s, the Gigabit MAC always operates in the GMII mode regardless of the PHY interface mode (GMII/TBI)

However, when configured in the GMII mode, the E1110_TXD, E1110_RXD, E1110_PHY_TXCLK, and E1110_PHY_RXCLK signals are mapped to the Gigabit MAC GMII signals as shown in Figure 2.3.

Figure 2.3 PHY Multiplexer Signal Mapping in GMII Mode

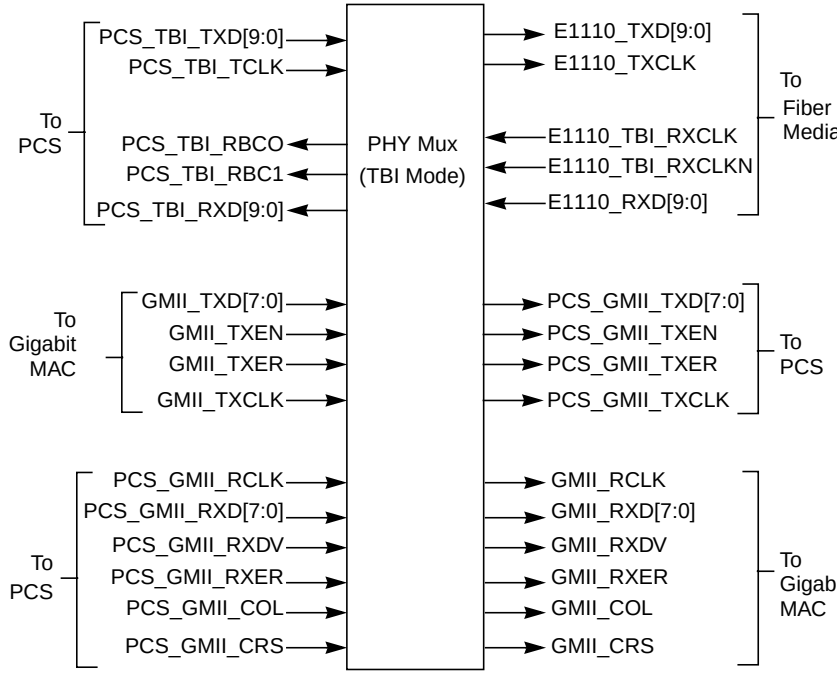


The PHY module maintains the timing relationship of all incoming and outgoing signals such that GMII specifications are met.

2.1.5.3 TBI Mode

In the TBI mode of operation, the E-1110 PHY signals are mapped to the TBI signals. However, the TBI clocks are derived from separate pins as shown in Figure 2.4. The Gigabit MAC must interface to the GMII signals that come from the PCS module when operating in the TBI mode, as shown in the figure. The GMII signals hence have an additional level of multiplexing apart from the PHY signals to accommodate the GMII signals coming from the PCS module.

Figure 2.4 PHY Multiplexer Signal Mapping in TBI Mode



2.1.6 Frame Structure

This section describes the IEEE 802.3 standard MAC frame format.

2.1.6.1 MAC Layer Frame Structure Support Requirement.

By default, the Gigabit MAC supports the IEEE 802.3 standard MAC frame format. The default operating mode is determined from the state of the host transmit and receive configuration interface signals. The IEEE 802.3 standard MAC frame structure is shown in Table 2.1.

Table 2.1 Standard MAC Frame Structure for IEEE 802.3

Field Description	Size	
	Minimum	Maximum
Preamble	7 Octets	7 Octets
Start of Frame Delimiter (SFD)	1 Octet	1 Octet
Destination Address (DA)	6 Octets	6 Octets
Source Address (SA)	6 Octets	6 Octets
Type/Length	2 Octets	2 Octets
LLC Data	46 Octets	1500 Octets
Frame Check Sequence (FCS)	4 Octets	4 Octets
Total Frame Length	64 Octets	1518 Octets

The IEEE 802.3 standard requires padding of frames to provide a minimum frame length of 64 bytes, where the frame length is the sum of the following fields:

- Destination Address
- Source Address
- Type/Length
- LLC Data
- Frame Check Sequence

The Gigabit MAC transmit function optionally pads frames of less than 64 bytes. The pad bytes are added after the LLC data field and before the frame check sequence field so that the minimum frame size of 64 bytes is maintained. The pad bytes are arbitrary, and are typically zeroes.

Note: The preamble and start frame delimiter fields are not included in the total frame length count.

The Gigabit MAC also supports various types of nonstandard frames, which can be used to provide support for customized applications or testing functions. These options are under the control of the host transmit and receive configuration interface signals defined in Chapter 3, "Signals."

2.1.6.2 Host Frame Structure Support Requirement.

The E-1110 MAC host frame structure consists of the following fields:

- Destination Address
- Source Address
- Type/Length
- LLC Data

This structure is maintained in the E-1110 MAC host transmit function interface and the host receive function interface. The Gigabit MAC's host frame structure is shown in Table 2.1.

Table 2.2 E-1110 MAC Host Frame Structure

Frame Field	Size Min	Size Max
Destination Address (DA)	6 Octets	6 Octets
Source Address (SA)	6 Octets	6 Octets
Type/Length	2 Octets	2 Octets
LLC Data	46 Octets	1500 Octets/9,982 Octets for HUGE Mode
Frame Check Sequence (FCS)	4 Octets	4 Octets
Total	64 Octets	1518 Octets/9,000 Octets for HUGE Mode

The IEEE 802.3 standard requires padding of host frames to provide a minimum frame length of 60 bytes at the host interface (64 bytes at the media, including the FCS). The frame length is the sum of the lengths of the destination address field, source address field, type/length field, and LLC data field. The MAC's transmit function pads host frames of less than 60 bytes. Arbitrary pad bytes (typically zeroes) are added after the LLC data field so that the minimum frame size of 60 bytes is maintained, not counting the four byte FCS sequence. The MAC transmit function, when enabled, automatically performs the padding function. The result is that the host may present frames to the MAC with LLC data fields as small as one byte for successful transmission. The minimum frame size

supported on the media is 64 bytes, including the fields listed in Table 2.1, with the required padding and the four-byte FCS field.

In the Gigabit mode, the MAC is designed to operate with an IPG of 64 ns and transmit and receive packets of sizes up to 9,000 bytes. Attempting to receive longer packets may cause packet data corruption. However there is no limit on the transmit side packet size. The 10/100 MAC limits the transmit frame size to the maximum programmed packet length.

2.2 Physical Layer Device (PHY) Interface

The E-1110 core supports three different MAC to PHY interfaces:

- 1000 Mbits/s GMII
- 1000 Mbits/s TBI
- 10/100 Mbits/s MII

Note: in 10/100 mode, the PHY interface is always MII; in 1000 mode, the PHY interface can be GMII or TBI.

The E-1110 core implements a simple 2:1 or 3:1 multiplexer, which is controlled with the MAC_SPEED_MODE and MAC_PHY_MODE configuration signals.

The MAC_PHY_MODE signal selects between the GMII mode and the TBI mode. If TBI mode is selected, the Gigabit MAC is connected to the GMII interface of the PCS module instead of the PHY. Depending upon the configuration, the definition of the signals changes to suit the interface requirements.

2.3 Clock Operation

This section describes the operation of the clocks in the E-1110 core.

2.3.1 Clocks for 10/100 Mbits/s Mode

The core uses the following clocks for 10/100 Mbits/s operation:

- Clocks from the PHY to the E-1110 MAC core:
  - E1110_PHY_RCLK
  - E1110_MII_TCLK.
- Clocks from the E-1110 to the E-110 MAC core:
  - MII_TCLK
  - MII_RCLK
- Clocks from the E-110 to the E-1110 MAC core:
  - E110_MTXC
  - E110_MRXC
- Clock for the host packet bus interface: CLK125

The E-1110_PHY_RCLK, E1110_MII_TCLK, MII_TCLK, MII_RCLK, E110_MTXC, and E110_MRXC clocks are basically the same transmit and receive clocks from the PHY device to operate the core in the 10/100 mode. The E-1110 core, when configured in the 10/100 mode, configures the PHY interface for the MII mode. The clocks input to the E-1110 PHY interface are output over to the E-110 interface as MII signals after passing through the multiplexer logic. The same MII clocks are input to the E-1110 core as E110_MTXC and E110_MRXC instead of directly using them internally. This is done to support a serial MII (SMII) interface, if required. If an SMII interface is used, the entire Physical Interface Multiplexer can be bypassed in the E-1110 core; however, in this case, a separate multiplexer must be added outside the E-1110 core.

The transmit and receive clocks described above are input to the E-1110 core and used for flow control and part of the Host Interface module. The clock frequencies are 2.5 MHz or 25 MHz. When the E-1110 core is configured in Gigabit mode, the E-110 core drives the MII_TCLK and MII_RCLK signals LOW. The clock frequency is 25% of the transmit data rate. A PHY operating at 100 Mbits/s provides the E110_MTXC and

E110_MRXC clocks at a frequency of 25 MHz. The duty cycle can be between 30% and 60%.

The host packet interface operates at 125 MHz and all the configuration and control signals are synchronous to that clock.

2.3.2 Clocks for 1000 Mbits/s GMII Mode

The core uses the following clocks for 1000 Mbits/s GMII operation:

- Clock from the PHY to the E-1110 core: E1110_PHY_RCLK
- Clock to the PHY from the E-1110 core: E1110_PHY_TCLK
- Clock from the host packet bus interface: CLK125

The E1110_PHY_RCLK and E1110_PHY_TCLK signals are 125 MHz, ±100 ppm GMII interface clocks. The data from the PHY is received synchronously with E1110_PHY_RCLK and the data is output to the PHY synchronously with E1110_PHY_TCLK. The E1110_PHY_TCLK is the same clock as the input CLK125 clock.

The CLK125 signal is a 125 MHz, ±50 ppm clock used for the Gigabit MAC and the host packet bus interface logic in the E-1110 core.

2.3.3 Clocks for 1000 Mbits/s TBI Mode

The core uses the following clocks for 1000 Mbits/s TBI operation:

- Clocks from the PHY to the E-1110 core:
  - E1110_TBI_RCLK
  - E1110_TBI_RCLKN
- Clock to the PHY from the E-1110 core: E1110_PHY_TCLK
- Clocks from the PCS to the E-1110 core:
  - PCS_GMII_RCLK
  - PCS_TBI_TCLK
- Clocks between the PCS and E-1110 cores:
  - PCS_TBI_RCLK
  - PCS_TBI_RCLKN
  - PCS_GMII_TCLK
- Clock from the host packet bus interface: CLK125

All the clocks are 125 MHz, ±100 ppm. The data from the PHY is received synchronously with the E1110_TBI_RCLK and E1110_TBI_RCLKN signals and the data is output to the PHY synchronously with the E1110_PHY_TCLK signal.

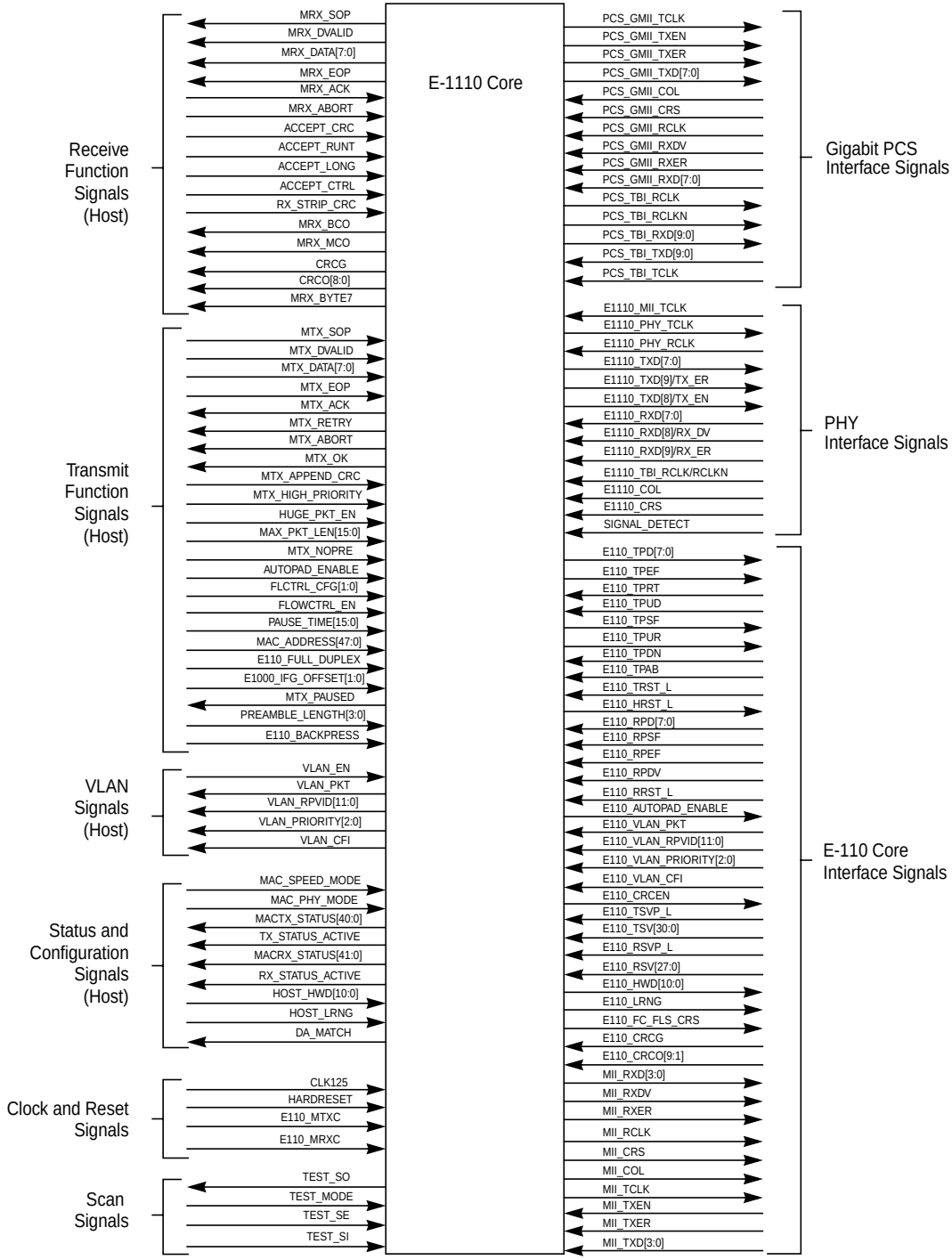
In TBI mode, the E-1110 core multiplexes out TBI mode signals to the PCS module. The E-1110 core also receives GMII signals from the PCS module and routes them to the Gigabit MAC.

The CLK125 signal is a 125 MHz, ±50 ppm clock used for the Gigabit MAC and Host Interface logic in the E-1110 core.

Chapter 3
Signals

This chapter contains detailed descriptions of each of the E-1110 signals. Because the E-1110 is a core and not a physical package, there are no actual pins, so this chapter describes the functions of the core signals. The chapter contains the following sections:

Figure 3.1 E-1110 System Interfaces



3.1 Receive Function Signals

The host communicates with the E-1110 Gigabit MAC receive function using the signals listed in this section. Signal direction is from the perspective of the E-1110 core.

MRX_SOP **Receive Start of Packet** **Output**

The Receive Start of Packet (MRX_SOP) output signal, when asserted, indicates that a new packet has been received. This signal is asserted along with MRX_DVALID and kept asserted until the host asserts the MRX_ACK signal. The MAC asserts MRX_SOP synchronously with the 125 MHz clock.

MRX_DVALID **Receive Data Valid** **Output**

MRX_DVALID when asserted, indicates that valid data is present on the MRX_DATA[7:0] output pins. When MRX_ACK is sampled active with MRX_DVALID, the MAC causes valid data to be placed on the MRX_DATA[7:0] pins. If the MAC asserts the MRX_DVALID output signal and the MRX_ACK input is deasserted, a receive overflow error condition is declared. This signal is discontinuous in the 10/100 mode of operation due to the MAC's lower throughput. The MAC synchronously asserts MRX_DVALID at 125 MHz.

MRX_DATA[7:0]

Receive Data **Output**

The MRX_DATA[7:0] output signals form the receive data bus. Each 8-bit data byte is clocked out of the MAC to the host receive data buffer on each clock cycle when both the MRX_DVALID and MRX_ACK signals are asserted. Data is valid on the MRX_DATA[7:0] output bus for one RX_CLK clock cycle. Bit ordering is maintained between E1110_RXD[7:0] and MRX_DATA[7:0]. The MAC outputs the data synchronously at 125 MHz.

MRX_EOP **Receive End of Packet** **Output**

MRX_EOP is asserted for one clock cycle to indicate the end of packet. When MRX_EOP is asserted, the last word is present on the MRX_DATA[7:0] pins. This signal is asserted under all conditions, including aborted or

overflow error packets, to indicate an end of the received packet for the MAC.

MRX_ACK **Receive Data Acknowledge** **Input**

MRX_ACK, when asserted, indicates that the host receive data buffer function is ready to accept data. If the MAC asserts the MRX_DVALID output signal and the MRX_ACK input signal is deasserted, a receive overflow error condition is declared and the packet being received is rejected. The MAC samples MRX_ACK synchronously at 125 MHz whenever MRX_DVALID is asserted.

Generally, the host interface should always assert this signal unless the host bus is unable to adequately buffer and manage the data being received.

MRX_ABORT **Abort Packet Receive** **Input**

This signal, when asserted for one clock cycle, aborts the receive packet process. It can be asserted anytime between the assertion of MRX_SOP and assertion of MRX_EOP.

The MAC ignores MRX_ABORT if it is asserted when the MRX_EOP signal is active; otherwise it generates an overflow error condition for the MAC.

ACCEPT_CRC **Accept Packets With CRC error** **Input**

ACCEPT_CRC, when asserted, instructs the MAC to mask the REJECT bit (RXSV36) of the Receive Statistics Vector and allow the MAC receive function to accept frames with CRC errors. Note that all frames received by the Gigabit MAC are passed to the host's receive function interface.

ACCEPT_RUNT

Accept Runt Frames **Input**

ACCEPT_RUNT, when asserted, instructs the MAC receive function to mask the REJECT bit (RXSV36) of the Receive Statistics Vector and accept short frames.

ACCEPT_LONG

Accept Long Frames **Input**

ACCEPT_LONG, when asserted, instructs the MAC receive function to mask the REJECT bit (RXSV36) in the Receive Statistics Vector (RXSV36) and accept frames

longer than 1518 bytes and smaller than 1536 bytes if the huge mode is disabled.

ACCEPT_CTRL

Accept Control Frames **Input**

ACCEPT_CTRL, when asserted, instructs the MAC receive function to mask the REJECT bit of the Receive Statistics Vector and accept all IEEE 802.3 pause flow control frames

RX_STRIP_CRC

Receive Packet Strip CRC **Input**

RX_STRIP_CRC, when asserted, instructs the MAC receive function to strip off the 32-bit CRC field from the end of each received frame as it is passed to the host receive function interface. When deasserted, RX_STRIP_CRC instructs the MAC receive function to pass the 32-bit CRC field received at the end of each frame to the host receive function interface.

RX_STRIP_CRC is a configuration input and should be changed only when the receive engine is idle or during reset. This signal must not be changed any time between the assertion of MRX_SOP and the assertion of MRX_EOP.

MRX_BCO **Broadcast Frame Received** **Output**

When asserted, MRX_BCO indicates that the received packet is a broadcast packet. MRX_BCO is asserted with MRX_BYTE7. The host interface can then decide to reject or accept broadcast packets.

MRX_MCO **Multicast Frame Received** **Output**

When asserted, MRX_MCO indicates that the received packet is a multicast packet. MRX_MCO is asserted with MRX_BYTE7. The host interface can then decide to reject or accept multicast packets.

CRCG **CRCO Output Good** **Output**

When asserted, CRCG indicates that the host can now sample the CRCO[8:0] signals. This signal is asserted on the seventh data byte after MRX_SOP is asserted and it is valid until the end of the packet. The host interface can then decide to reject or accept multicast packets using CRCO[8:0] to index into hashing tables.

CRCO[8:0] **CRCO Output** **Output**

The CRCO[8:0] signals reflect the state of the receive function FCS register after the first six bytes of a receive packet have been examined. CRCO[8:0] reflects the 9 MSBs of the 32-bit CRC computed on the destination address of the received packet.The host interface can then decide to reject or accept the packet.

MRX_BYTE7 **Byte 7 Valid Indicator** **Output**

When asserted, MRX_BYTE7 indicates that the host can now sample the MRX_BCO and MRX_MCO signals. This signal is asserted on the seventh data byte after MRX_SOP is asserted and it is valid for one clock cycle. The host interface can then decide to reject or accept broadcast packets.

3.2 Transmit Function Signals

The host communicates with the E-1110 Gigabit MAC transmit function using the signals listed in this section. Signal direction is from the perspective of the E-1110 core.

MTX_SOP **Transmit Start of Packet** **Input**

The host asserts MTX_SOP to request that the MAC start frame transmission. When the MTX_SOP input signal is asserted, the first byte of frame data is present on the MTX_DATA[7:0] input bus. Once asserted, the MTX_SOP signal remains asserted until the MAC asserts the MTX_ACK output signal. The host is then committed to the transmission of at least part of a frame or a frame fragment. If, after the assertion MTX_SOP, the host desires to cancel the frame transmission request, it may deassert the MTX_DVALID input signal while the MTX_ACK output signal is asserted to cause a data underrun abort condition. The MAC then asserts MTX_ABORT, which requests the host to abort the current transmit cycle.

In Gigabit mode, maintenance of maximum system transmit performance, relative to the IEEE 802.3 minimum interframe gap (IFG), requires that the MTX_SOP input signal be reasserted within a maximum of six CLK125 cycles after the deassertion of the last

received MTX_ACK signal. This assumes the host requires the minimum IEEE 802.3 interframe gap (IFG) of 96 bits (12 bytes).

MTX_SOP is synchronous to CLK125 (125 MHz clock).

MTX_DVALID **Transmit Data Valid** **Input**

MTX_DVALID, when asserted, indicates to the MAC that valid frame data is present on the MTX_DATA[7:0] input bus. If the MTX_DVALID input signal is deasserted while the MTX_ACK output signal is asserted, a transmit data underrun error condition is declared. The host interface should change the data on the data bus only when the MTX_DVALID and MTX_ACK are sampled active with the rising edge of CLK125.

This signal is synchronous to CLK125 (125 MHz clock).

MTX_DATA[7:0]

Transmit Data **Input**

The MTX_DATA[7:0] signals form the transmit data input bus to the MAC. The data byte is clocked into the MAC from the host transmit data buffer on each clock cycle when both the MTX_DVALID and MTX_ACK signals are asserted.

In Gigabit mode, MTX_DATA[7:0] is passed to E1110_TXD[7:0] at the GMII, while maintaining the bit ordering.

In the 10/100 Mbits/s mode, the data output sequence in nibbles is MTX_DATA[0:3], then MTX_DATA[7:4]. Due to the lower bandwidth requirement of the E-110 MAC, the data transfer may not occur in a burst but rather in a discontinuous manner.

The data is sampled synchronously with the positive edge of the 125 MHz system clock.

MTX_EOP **Transmit End of Packet** **Input**

MTX_EOP, when asserted, indicates to the MAC that the last byte or word of data for the current frame is present on the MTX_DATA[7:0] input bus. The MTX_EOP input signal should be asserted for the last transfer and should be kept asserted until the host samples the MTX_ACK signal on the positive edge of CLK125.

MTX_ACK **Transmit Data Acknowledge** **Output**

MTX_ACK, when asserted indicates that the MAC has accepted the data present on the MTX_DATA[7:0] input bus and that the host transmit data buffer should present the next word of transmit frame data.

New transmit frame data is expected on every CLK125 cycle where MTX_ACK is asserted except when the MTX_EOP input signal is asserted. The assertion of MTX_ACK may also be interpreted as an acknowledgment of the assertion of the MTX_DVALID input signal. Note that MTX_ACK is not continuous when in 10/100 mode due to the lower speeds of operation. Similarly, data transfer in 10/100 mode is also not continuous)

MTX_RETRY **Transmit Frame Retry.** **Output**

MTX_RETRY, when asserted, instructs the host to retry the current frame. The MTX_RETRY output is asserted as the result of a collision during transmission of the current frame in half-duplex[1] mode. Collisions can occur during the transmission of preamble, frame data, or carrier extension, and occur only in the half-duplex[1] mode. MTX_RETRY is output only when the MAC is configured in the E-110 mode.

In the Gigabit mode, MTX_RETRY is always LOW (inactive).

MTX_ABORT **Transmit Packet Abort** **Output**

MTX_ABORT, when asserted, indicates that the current packet transmission was aborted. A transmit packet abort is for any of the following conditions: a late collision, excessive collisions, transmit underrun, long packet size (unless specifically enabled using the HUGE_PKT_EN and MAX_PKT_LEN[15:0] configuration signals), or excess deferrals. The MTX_ABORT output is asserted anytime between MTX_SOP and MTX_EOP. Once asserted, it stays asserted until the start of the next packet or the next assertion of SOP.

In the Gigabit mode, MTX_ABORT is asserted only when a transmit underrun occurs.

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1. In the Gigabit mode, only full-duplex is supported, so MTX_RETRY is only active for 10 or 100 Mbits/s operation.

MTX_OK **Transmit Packet Successful** **Output**

MTX_OK, when asserted, acknowledges that the MAC was successful in transmitting the current frame. The MTX_OK output signal is asserted for one cycle of CLK125, with a minimum delay of one clock cycle from the assertion of MTX_EOP.

The MAC is ready to begin transmission of the next frame, if available, one clock cycle after the assertion of MTX_OK.

MTX_APPEND_CRC

Append CRC During Transmit **Input**

MTX_APPEND_CRC, when asserted, instructs the MAC to append its calculated 32-bit CRC value to the end of the frame currently being transmitted. This signal should stay stable throughout the transmit cycle from the assertion of MTX_SOP to the assertion of MXT_EOP.

MTX_HIGH_PRIORITY

Transmit Packet High Priority **Input**

MTX_HIGH_PRIORITY, when asserted, instructs the MAC transmit function to transmit the requested frame regardless of the pause state of the transmit function. MTX_HIGH_PRIORITY is sampled during the CLK125 clock cycle when the MTX_SOP input is asserted. MTX_HIGH_PRIORITY should be stable throughout the MAC transmit operation from the assertion of MTX_SOP to the assertion of MTX_EOP.

HUGE_PKT_EN

Huge Packet Enable Configuration **Input**

This signal, when asserted, allows the transmit MAC to transmit packets of sizes up to 9,000 bytes. This signal is sampled along with the MTX_SOP signal.

HUGE_PKT_EN is a configuration input that is sampled during normal MAC operation by the Gigabit MAC and the E-110 core. This signal can be derived from the configuration port logic of the host interface. Care should be taken to ensure these inputs are stable during normal operation and during packet transmissions.

When enabled, the maximum packet value is derived from the MAX_PKT_LEN[15:0] value controlled from the host. All received packets are truncated if the packet

length exceeds the allowed maximum packet length. In 10/100 mode, transmit frames are also truncated if they are found to exceed the programmed limit. In Gigabit mode, transmit operation does not take into account the huge mode or the maximum packet length. The Gigabit MAC transmits as long as the host sends data to the MAC.

MAX_PKT_LEN[15:0]

Maximum Packet Length **Input**

The MAX_PKT_LEN[15:0] input bus indicates the size or value of the receive frame threshold to the MAC receive function. The threshold defined with MAX_PKT_LEN[15:0] is used for receive frame truncation of long frames and for statistics generation of oversize and jabber frames. The packet length should always be between 1518 and 9,000 bytes (the MAC ignores maximum packet lengths smaller than 1518). The maximum value that can be programmed is 0x2328. The MAX_PKT_LEN[15:0] is in effect only when the HUGE_PKT_EN signal is asserted. If HUGEN_PKT_EN is deasserted, packets are accepted up to 1536 bytes and a cutoff occurs at packet size 1536. However, frames larger than 1518 are marked as oversized frames.

In 10/100 mode, transmit cutoff occurs similar to receive cutoff. In the Gigabit mode, however, the MAC does not cut off any frames, depending on the programmed packet length. The transmit process lasts as long as the host sends data to the MAC.

MTX_NOPRE **No Preamble** **Input**

When asserted the MTX_NOPRE signal instructs the MAC transmit engine to transmit the packet as input from the host and disable internal addition of a preamble.

The MAC samples MTX_NOPRE during packet transmission. MTX_NOPRE can be derived from the configuration port logic of the host interface. Care should be taken to ensure that these inputs are stable during normal operation and during packet transmissions.

AUTOPAD_ENABLE

Transmit Packet Padding Enable **Input**

This signal, when asserted, instructs the transmit MAC to pad packets that are less than 64 bytes with zeros. The MAC appends the CRC whenever the padding is performed on the packet.

AUTOPAD_ENABLE can be changed only when the transmit engine is idle or during reset. During transmit operation, this signal must be stable and can be derived from the configuration port logic of the host interface. Care should be taken to ensure that these inputs are stable during normal operation and during packet transmissions.

There is a difference in the way AUTOPAD_ENABLE affects the MAC function in the Gigabit and E-110 modes.

In the Gigabit mode, all packets of less than 60 bytes are padded and then a new CRC is computed and appended to the end of the packet. For packets between 60 and 63 bytes, only a CRC is calculated and appended to the packet. All packets greater than 64 bytes are untouched and no action is performed. During padding, the MAC does not perform a CRC check on the incoming packet.

In E-110 mode, packets less than 60 bytes are padded with zeroes and the CRC is appended to the end of the packet. For all packets greater than 59 bytes, a CRC is appended to the end of the packet. However, if MTX_APPEND_CRC is not asserted, the MAC checks for the CRC on the incoming packet from the host and reports a CRC error if there is one.

FLCTRL_CFG[1:0]

Flow Control Configuration **Input**

The FLCTRL_CFG[1:0] signals control the full-duplex flow control configuration as shown in the table.

FLCTRL_CFG[1:0]	Meaning
0b00	No flow control
0b01	Transmit-only flow control
0b10	Receive-only flow control
0b11	Transmit and receive flow control

The FLCTRL_CFG[1:0] signals can be derived from the configuration port logic of the host interface. Care should be taken to ensure that these inputs are stable during normal operation and during packet transmissions.

FLOWCTRL_EN

Flow Control Enable **Input**

FLOWCTRL_EN, when asserted, sends a pause frame with the host-programmed pause time. When it is deasserted, a pause frame with zero time is transmitted. The flow control module also contains a mirror pause time counter to send another pause frame if FLOWCTRL_EN remains asserted and the pause timer expires. This signal is internally synchronized for the E-110. The Gigabit MAC synchronously samples the signal on a continuous basis at 125 MHz.

PAUSE_TIME[15:0]

Pause Time **Input**

PAUSE_TIME[15:0] specifies the pause time value used while sending pause frames when FLOWCTRL_EN is asserted.

PAUSE_TIME[15:0] can be derived from the configuration port logic of the host interface. Care should be taken to ensure that these inputs are stable during normal operation and during packet transmissions.

MAC_ADDRESS[47:0]

MAC Address **Input**

The MAC address value is used to match Unicast addresses in the received packets. It is also used as a source address in pause frames sent out by the transmit function.

E110_FULL_DUPLEX

E-110 Full-Duplex Control **Input**

This signal is used to select the half- or full-duplex mode of operation for 10/100 mode. In Gigabit mode, this input is a don't care and the MAC is always configured for full-duplex mode regardless of the status of this signal.

The E-110 MAC and the flow control module both synchronously sample E110_FULL_DUPLEX during MAC operations. This signal can be derived from the configuration port logic of the host interface. Care should

be taken to ensure that these inputs are stable during normal operation and during packet transmissions or receptions.

E1000_IFG_OFFSET[1:0]

E1000 Interframe Gap Offset **Input**

The value on the E1000_IFG_OFFSET[1:0] lines selects the length of the Gigabit MAC interframe gap in bits.

E1000_IFG_OFFSET[1:0] can be changed only when the transmit engine is idle or during reset. During transmit operation, this signal must be stable in the normal mode of operation. For more details refer to Section 2.1.2.1, "Gigabit MAC Transmit Block Functional Description," page 2-6.

The IPG Value configured in the Gigabit MAC is as follows:

E1000_IFG_OFFSET[1:0]	IPG (ns)
0b00	64
0b01	80
0b10	96
0b11	112

MTX_PAUSED

Transmit Pause Status **Output**

MTX_PAUSED, when asserted, indicates that the MAC transmit function is in the paused state. The MAC transmit function enters the paused state only after the MAC receive function receives a valid flow control pause frame. When deasserted, MTX_PAUSED indicates that the MAC transmit function is enabled to transmit any frames requested from the host.

When the MAC is in a paused state, only flow control packets or high-priority packets can be transmitted.

PREAMBLE_LENGTH[3:0]

Preamble Length **Input**

PREAMBLE_LENGTH[3:0] is the preamble length in bytes used by the Gigabit MAC to encapsulate the transmit frame with preamble and SFD. The length includes the SFD, so the minimum value is 2 (0b0010), which corresponds to one byte of preamble plus one byte of SFD and the maximum value is 15 (0b111), which

corresponds to 14 bytes of preamble plus one byte of SFD. By default it should be configured to a value of 8 (0b1000).

E110_BACKPRESS

Back Pressure Flow Control **Input**

In 10/100 mode, E110_BACKPRESS is used for back-pressure control. This signal is synchronously sampled on the positive edge of the CLK125 signal. This signal can be derived from the configuration port logic of the host interface. Care should be taken to ensure that these inputs are stable during normal operation and during packet transmissions. In Gigabit mode, the E110_BACKPRESS signal is a don't care.

3.3 VLAN Signals

The signals listed in this section allow the host to detect and process VLAN frames. Signal direction is from the perspective of the E-1110 core.

VLAN_EN **VLAN Enable** **Input**

This signal, when asserted, enables the detection of VLAN frames.

VLAN_PKT **VLAN Frame Detected** **Output**

This signal is asserted during a frame receive operation any time after 16 clock cycles from the start of frame to indicate the detection of a VLAN frame. VLAN_PKT is deasserted with the next start of frame, when MRX_SOP is asserted.

VLAN_RPVID[11:0]

Extracted VLAN Receive Packet ID **Output**

VLAN_RPVID[11:0] is the extracted 12-bit VLAN ID from the received frame. This information is valid whenever the VLAN_PKT signal is asserted. The format is defined in the IEEE 802.1 VLAN standard.

VLAN_PRIORITY[2:0]

Extracted VLAN Packet Priority **Output**

VLAN_PRIORITY[2:0] contains the extracted 3-bit VLAN priority from the received frame. This information is valid whenever the VLAN_PKT signal is asserted. The format is specified in the IEEE 802.1 VLAN standard.

VLAN_CFI **Extracted VLAN CFI** **Output**

The VLAN_CFI signal is the Canonical Format Indicator bit in the received frame. This information is valid whenever the VLAN_PKT signal is asserted. The format is specified in the IEEE 802.1 VLAN standard.

3.4 Status and Configuration Signals

The signals listed in this section allow the host to read status from the E-1110 core and to configure its operation. Signal direction is from the perspective of the E-1110 core.

MAC_SPEED_MODE

MAC Speed Mode **Input**

This signal selects the speed of the MAC. When asserted, MAC_SPEED_MODE selects the Gigabit mode of operation. When deasserted, the signal selects the 10/100 mode of operation. This signal must be stable under all conditions and after HARDRESET is deasserted.

MAC_PHY_MODE

PHY Interface Mode for the MAC **Input**

This signal selects the PHY interface mode for the Gigabit MAC. When MAC_PHY_MODE is HIGH, the interface is configured to TBI mode. When the signal is LOW, the interface is configured in GMII mode. This signal is don't care or ignored if the MAC is configured in the 10/100 mode of operation. The PHY interface mode in 10/100 mode is always MII. This signal must be stable under all conditions and after the HARDRESET signal is deasserted.

MACTX_STATUS[40:0]

MAC Transmit Status Vector **Output**

This status word is a combination of E-1110 and E-110 status output during transmit operation. The details are shown in the following table.

Description	Vector Bit Number
Reserved	TXSV40
Transmit Packet Cutoff (for packets longer than 9,000 bytes)	TXSV39[1]
Transmit Packet CRC Error (when APPEND_CRC is inactive)	TXSV38
Transmit Packet Underrun	TXSV37
Transmit Packet Transmitted (after deferral)	TXSV36[1]
Transmit Packet Aborted (excess deferral)	TXSV35[1]
Transmit Packet Transmitted (after retry late collision)	TXSV34[1]
Transmit Packet Aborted (late collision)	TXSV33[1]
Transmit Packet Aborted (excess collisions, > 15)	TXSV32[1]
Transmit Packet Collision Count	TXSV[31:28][1]
Flow Control Packet Transmitted	TXSV27
Unicast Packet Transmitted	TXSV26
Broadcast Packet Transmitted	TXSV25
Multicast Packet Transmitted	TXSV24
Transmit Successful	TXSV23
Transmit Packet Length 1519 (packet length between 1519 to maximum packet length indicated by MAX_PKT_LEN)	TXSV22
Transmit Packet Length 1024 (packet length between 1024–1518)	TXSV21
Transmit Packet Length 512 (packet length between 512–1023)	TXSV20
Transmit Packet Length 256 (packet length between 256–511)	TXSV19
Transmit Packet Length 128 (packet length between 128–255)	TXSV18

Description	Vector Bit Number
Transmit Packet Length 65 (packet length between 65–127)	TXSV17
Transmit Packet Length 64 (packet length 64 or smaller)	TXSV16
Transmit Packet Byte Count (including CRC field)	TXSV[15:0]

1. Always 0 when operating in Gigabit mode

TX_STATUS_ACTIVE

Transmit Status Indicator **Output**

TX_STATUS_ACTIVE is asserted for one clock cycle every time there is any change in the MACTX_STATUS[40:0] transmit status vector.

MACRX_STATUS[41:0]

MAC Receive Status Vector **Output**

This status word is a combination of E-1110 and E-110 status output during receive operation. The details are shown in the following table.

Description	Vector Bit Number
Received Packet Byte Count (includes CRC field)	RXSV[15:0]
Received Packet CRC Error (when APPEND_CRC is inactive)	RXSV16
Received a Frame Fragment (collision/undersized with bad CRC)	RXSV17
Received JABBER (packet length > MAX_PKT_LEN with invalid CRC)	RXSV18
Received an Undersized frame (good CRC)	RXSV19
Received Packet Length 64 (packet length 64 or smaller)	RXSV20
Received Packet Length 65 (packet length between 65–127)	RXSV21
Received Packet Length 128 (packet length between 128–255)	RXSV22
Received Packet Length 256 (packet length between 256–511)	RXSV23
Received Packet Length 512 (packet length between 512–1023)	RXSV24

Description	Vector Bit Number
Receive Packet Length 1025 (packet length between 1024–1518)	RXSV25
Receive Packet Length 1519 (packet Length between 1519 to Maximum Packet length indicated by MAX_PKT_LEN)	RXSV26
Received Oversized packet (packet Length > MAX_PKT_LEN with valid CRC)	RXSV27[1]
Good Packet Received	RXSV28
Multicast Packet Received	RXSV29
Broadcast Packet Received	RXSV30
Unicast Packet Received	RXSV31
Received MAC Control Packet with Unsupported Opcode	RXSV32
Received Pause Control Frame	RXSV33
Receive Packet Overflow	RXSV34
8B/10B or 4B/5B Code Violation Error	RXSV35
Reject the Received Frame (Bad Packet)	RXSV36
Carrier Event Previously Seen/Invalid SFD	RXSV37
Long Event Previously Seen	RXSV38[2]
Invalid Preamble in the Received Packet	RXSV39
Dribble Nibble Seen in the Received Packet	RXSV40[2]
False Carrier	RXSV41

1. The maximum packet is always 9,000 bytes. Received or transmitted packets larger than 9,000 bytes are truncated. The errors for oversize packets assume that the packet size is greater than MAX_PKT_LEN and less than 9,000 bytes
2. Always 0 (or indicated status) when operating in Gigabit mode.

RX_STATUS_ACTIVE

Receive Status Indicator **Output**

This signal is asserted for one clock cycle every time there is a change in the MACRTX_STATUS[41:0] receive status vector. It also is asserted for a minimum of two clock cycles after the deassertion of the MRX_EOP signal.

HOST_HWD[10:0]

Host Write Data for E-110 **Input**

The HOST_HWD[10:0] signals contain the value of the random number that the E-1110 loads into the MAC's Linear Feedback Shift Register (LFSR) to generate the random number sequence used in collision backoff timing.

HOST_LRNG

Load Random Number Generator **Input**

The Host asserts the HOST_LRNG signal to indicate that the HOST_HWD[10:0] signals are valid. This signal is synchronous to the 125 MHz transmit clock.

The HOST_HWD[10:0] and HOST_LRNG signals are valid for 10/100 mode only and are don't care for Gigabit mode.

DA_MATCH **Destination Address Match** **Output**

DA_MATCH is asserted along with the MACRX_STATUS[41:0] signals to indicate that the currently received frame is a MAC control frame with a unicast destination address match. The state of this pin is updated every time MACRX_STATUS[41:0] changes.

3.5 Clock and Reset Signals

This section describes the clock and reset signals used in the E-1110 core. Signal direction is from the perspective of the E-1110 core.

CLK125 **Gigabit Transmit/Host Interface Clock Ref** **Input**

CLK125 is the transmit clock reference input signal. Its runs at 125 MHz with a 50% duty cycle and a frequency of ±100 ppm. The MAC and host interface logic is driven from the CLK125 clock input.

HARDRESET **Hardware Reset** **Input**

This is an asynchronous reset signal to the entire MAC and associated logic.

E110_MTXC **E-110 Transmit Clock** **Input**
In 10/100 mode, E110_MTXC is the clock input from the E-110. The frequency is 25 MHz or 2.5 MHz, depending on the mode of operation. The transmit interface logic in the E-1110 core operates using this clock.

E110_MRXC **E-110 Receive Clock** **Input**
In 10/100 mode, E110_MRXC is the clock input from the E-110. The frequency is 25 MHz or 2.5 MHz, depending on the mode of operation. The receive interface logic in the E-1110 core operates using this clock.

3.6 Scan Signals

The signals in this section are used for E-1110 testing. Signal direction is from the perspective of the E-1110 core.

TEST_SO **Test Scan Out** **Output**
The TEST_SO is a serial scan chain output pin.

TEST_MODE
ATPG Test Mode Enable **Input**
When TEST_MODE is asserted, the MAC enters the test mode.

TEST_SE **Test Scan Enable** **Input**
When TEST_SE is asserted, all the internal flip-flops accept data on the TEST_SI input pin.

TEST_SI **Test Scan In** **Input**
TEST_SI is a serial scan chain input pin.

3.7 Gigabit PCS Interface Signals

The signals in this section are used to interface the E-1110 core to the external PCS. Signal direction is from the perspective of the E-1110 core.

PCS_GMII_TCLK
PCS GMII 125 MHz Transmit Clock **Output**
See the definition for E1110_MII_TCLK**.**

PCS_GMII_TXEN

PCS GMII Interface Transmit Enable **Output**

See the definition for E1110_TXD[8]/E1110_TX_EN.

PCS_GMII_TXER

PCS GMII Interface Transmit Error **Output**

See the definition for E1110_TXD[9]/E1110_TX_ER.

PCS_GMII_TXD[7:0]

PCS GMII Interface TX Data **Output**

See the definition for E1110_TXD[7:0].

PCS_GMII_COL

PCS GMII Interface Collision **Input**

See the definition for E1110_COL.

PCS_GMII_CRS

PCS GMII Interface Carrier Sense **Input**

See the definition for E1110_CRS.

PCS_GMII_RCLK

PCS GMII Interface 125-MHz Receive Clock **Input**

See the definition for E1110_PHY_RCLK.

PCS_GMII_RXDV

PCS GMII Interface RX_DV **Input**

See the definition for E1110_RXD[8]/E1110_RX_DV.

PCS_GMII_RXER

PCS GMII Interface RX_ER **Input**

See the definition for E1110_RXD[9]/E1110_RX_ER.

PCS_GMII_RXD[7:0]

PCS GMII Interface Receive Data **Input**

See the definition for E1110_RXD[7:0].

PCS_TBI_RCLK

PCS TBI Interface RXCLK **Output**

See the definition for E1110_TBI_RCLK. This signal is also driven during test scan mode from E1110_TBI_RCLK.

PCS_TBI_RCLKN

PCS TBI Interface RCLKN. **Output**

See the definition for E1110_TBI_RCLKN. This signal is also driven during test scan mode from E1110_TBI_RCLKN.

PCS_TBI_RXD[9:0]

PCS TBI Interface Receive Data **Output**

See the definition for E1110_TBI_RXD[9:0].

PCS_TBI_TXD[9:0]

PCS TBI Interface Transmit Data **Input**

See the definition for E1110_TBI_TXD[9:0].

PCS_TBI_TCLK

PCS TBI Interface Transmit Clock **Input**

See the definition for E1110_MII_TCLK.

3.8 PHY Interface Signals

The signals in this section are used to interface the E-1110 core to the external PHY. Signal direction is from the perspective of the E-1110 core.

E1110_MII_TCLK

PHY GMII/TBI 125 MHz Transmit Clock **Input**

In the MII mode, this clock input is an MII transmit clock running at either 2.5 or 25 MHz. The MII transmit data is synchronized and output with respect to this clock.

In the test scan mode, this clock is output on the MII_TCLK pin for scan mode testing of the E-110 core.

E1110_PHY_TCLK

PHY Transmit Clock in GMII/TBI **Output**

E1110_PHY_CLK is a GMII/TBI transmit 125 MHz clock output signal. The MAC continuously drives this signal to the PHY device. It is used to synchronize the data in the 1000BASE-T GMII mode or in the 1000BASE-SX/CX/LX TBI mode.

E1110_PHY_RCLK

PHY Receive Clock **Input**

In GMII mode, this is a GMII Receive 125 MHz clock Input signal. It is used to synchronize the data in GMII mode. In MII mode, this is a MII Receive 2.5/25 MHz clock Input signal. It is used to synchronize the data in MII mode. In TBI mode, this is a TBI Receive 125 MHz clock input signal. It is used to synchronize the data in 1000BASE-SX/CX/LX TBI mode. The even byte lane data is clocked out of the Physical Medium Attachment (PMA) on this clock.

In the test scan mode, this clock acts as a scan clock and is also output on MII_RCLK for scan mode testing of E-110 core.

E1110_TXD[7:0]

MII/GMII/TBI Transmit Data **Output**

E1110_TXD[7:0] is the transmit data to the PHY and is synchronous to the GMII/TBI or MII clock. TXDATA[7] is the most-significant bit. In the MII mode, only the E1110_TXD[3:0] signals are valid. In the TBI mode, the data is 10 bits wide with E1110_TXD[9] as the MSB.

E1110_TXD[8]/E1110_TX_EN

Transmit Enable **Output**

E1110_TX_EN is the active-HIGH transmit enable signal. When it is asserted, the data on TXD[7:0] is encoded and transmitted over the twisted-pair cable. This signal is shared with bit 8 of the TBI transmit stream in the MII/GMII/TBI mode of operation.

E1110_TXD[9]/E1110_TX_ER

Transmit Error **Output**

E1110_TX_ER is an active-HIGH signal. When it is asserted, it indicates an error to the PHY device. The PHY then sends a “bad code” indication over the cable.

This signal is shared with bit 9 of the TBI transmit stream in the MII/GMII/TBI mode of operation.

E1110_RXD[7:0]

MII/GMII/TBI Receive Data **Input**

E1110_RXD[7:0] is the receive data from the PHY and is synchronous to the GMII or MII clock. E1110_RXD[7] is the most-significant bit. In the MII mode, only

E1110_RXD[3:0] are valid. In TBI mode the data is 10 bits wide with E1110_RXD[9] as the MSB.

E1110_RXD[8]/E1110_RX_DV

Receive Data Valid **Input**

E1110_RX_DV is an active-HIGH signal. When it is asserted, the receive data (E1110_RXD[9:0]) can be sampled synchronously with E1110_PHY_RCLK. This signal is valid only in MII/GMII modes and is shared with bit 8 of the TBI receive data input stream in the MII/GMII/TBI mode.

E1110_RXD[9]/E1110_RX_ER

Receive Error **Input**

E1110_RX_ER, when asserted, indicates that a data error has been detected during the frame receive operation. This signal is valid only in MII/GMII modes and is shared with bit 9 of the TBI receive data input stream input in the MII/GMII/TBI mode.

E1110_TBI_RCLK

TBI Receive Clock (RBC1) **Input**

In the TBI Mode, E1110_TBI_RCLK is a TBI receive 62.5 MHz clock input signal. It is used to synchronize the data in 1000BASE-X TBI mode. The even byte lane data is clocked out of the PMA on this clock.

In the test scan mode, this clock is output on PCS_TBI_RCLK for scan mode testing of the PCS soft macro.

E1110_TBI_RCLKN

TBI Receive Clock (RBC0) **Input**

In the TBI Mode, E1110_TBI_RCLKN is a TBI receive 62.5 MHz clock input signal. It is used to synchronize the data in 1000BASE-X TBI mode. The odd byte lane data is clocked out of the PMA on this clock. This clock is 180° phase shifted from E1110_TBI_RCLK and the data is sampled on both the clocks with respect to the positive edges.

In the test scan mode, this clock is output on PCS_TBI_RCLKN for scan mode testing of the PCS soft macro.

E1110_COL **Collision Detect** **Input**
When E1110_COL is asserted, it indicates that a collision has been detected in the link. E1110_COL is an asynchronous input.

E1110_CRS **Carrier Sense** **Input**
When E1110_CRS is asserted, it indicates the presence of a non-idle medium. It is also asserted during transmission of packets. It is deasserted whenever idle or end of stream delimiter is detected in the receive data stream.

SIGNAL_DETECT
Signal Detect for Gigabit MAC **Input**
SIGNAL_DETECT is the signal detection input from the TBI PCS module. The Gigabit MAC uses this signal to keep the MAC under reset in the absence of signal detection. The MAC also generates a reset pulse whenever it sees SIGNAL_DETECT change from LOW to HIGH.

3.9 E-110 Core Interface Signals

The signals in this section are used to interface the E-1110 core to the external E-110 core. Signal direction is from the perspective of the E-1110 core.

E110_TPD[7:0]
E-110 Transmit Data **Output**
The E110_TPD[7:0] signals are the transmit data bus. The E-1110 holds the TPD[7:0] signals valid for exactly two MII_TCLK clock cycles.

E110_TPEF **E-110 Transmit Packet End of Frame** **Output**
The E-1110 asserts the E1110_TPEF signal to indicate the last byte of the transmit packet is available from the host. E110_TPEF must be valid for two MII_TCLK clock periods before it is deasserted.

E110_TPRT **E-110 Transmit Retry Due to Collision/Error** **Input**
The E-110 MAC asserts the E110_TPRT signal to indicate that the E-110 MAC function encountered at least one collision during a transmit attempt. The MAC

asserts E110_TPRT until the MAC receives a fresh request to transmit, which is indicated when the E110_TPSF signal is asserted.

E110_TPUD **E-110 Transmit Packet Data Used** **Input**
The E-110 MAC asserts the E110_TPUD signal to indicate that the preamble has been transmitted. Every two clocks thereafter, the E-1110 must place the E110_TPD[7:0] signals on the bus for the E-110 MAC. The MAC keeps E110_TPUD asserted until the MAC accepts all the data bytes in the transmit packet from the E-1110.

E110_TPSF **E-110 Transmit Packet Start of Frame** **Output**
The E-1110 asserts the E110_TPSF signal to request the E-110 core to transmit a new packet. The E-1110 keeps the E110_TPSF signal asserted for one transmit clock period after the E-110 core asserts the E110_TPUD signal. The E110_TPSF signal is synchronous to MII_TCLK.

E110_TPUR **E-110 Transmit Data Underrun Error** **Output**
When the E-1110 MAC asserts the E110_TPUR signal, the E-110 MAC discontinues transmission. If the E-1110 is unable to supply transmit packet data bytes in a timely manner to the E-110 core (an underrun condition), the E-1110 asserts TPUR.

The E-1110 asserts E110_TPUR for at least two MII_TCLK clock cycles. The MAC asserts E110_TPAB and MII_TXER in the very next clock cycle and deasserts MII_TXEN one cycle after MII_TPAB and MII_TXER are asserted. Deassertion of MII_TXEN indicates the end of transmission.

E110_TPDN **E-110 Transmit Done** **Input**
When asserted, the E110_TPDN signal indicates successful completion of the packet transmit process. The MAC keeps E110_TPDN asserted until the MAC receives a fresh request to transmit, which is indicated when the E-1110 asserts the E110_TPSF signal.

E110_TPAB

E-110 Transmit Abort **Input**

When asserted, the E110_TPAB signal indicates that the transmission was discontinued. E110_TPAB remains asserted until the E-110 MAC receives a request to transmit, which is indicated when the E-1110 asserts E110_TPSF. When deasserted, E110_TPAB indicates that the transmission was not aborted. The following circumstances cause the transmission to be halted:

- *Excess deferrals*, which occur when the media is busy longer than twice the maximum frame length (greater than 24,288[1] bits when the HUGE_PKT_EN signal is deasserted or greater than 524,288[2] bits when HUGE_PKT_EN is asserted)
- Late collision
- Multiple collisions (greater than 15)
- Transmit underrun
- Larger than normal packet, which is 1518 bytes (see the HUGE_PKT_EN signal description)

E110_TRST_L

E-110 Transmit Reset **Input**

Other modules in an ASIC can use the active-LOW E110_TRST_L signal as a host reset synchronized to the transmit clock (MII_TCLK). Because the MII_TCLK clock can be slow with respect to a host reset pulse, or even stopped, the E-1110 reset signal (E110_HRST_L) is captured in the E-110 MAC transmit function. The transmit function asserts E110_TRST_L asynchronously to MII_TCLK when the E110_HRST_L signal occurs and deasserts E110_TRST_L synchronously on the positive transition of MII_TCLK. Modules can use E110_TRST_L to initialize transmit logic.

1. 24,288 bits = 1518 bytes x 8 bits/byte x 2 (242.88 µs for 100 Mbits/s operation or 2.4288 ms for 10 Mbits/s operation)
2. 524,288 bits = 32 Kbytes x 8 bits/byte x 2 (5242.88 µs for 100 Mbits/s operation or 52.43 ms for 10 Mbits/s operation)

E110_HRST_L

Asynchronous System Reset **Output**

The E110_HRST_L signal is an active-LOW signal from the E-1110 that initializes the E-110 MAC function. When E110_HRST_L is asserted, the MAC asserts the synchronized transmit and receive reset signals, E110_TRST_L and E110_RRST_L, which are inputs to the MAC transmit function and receive function, respectively. Other modules in an ASIC may use these signals for initialization. Both E110_TRST_L and E110_RRST_L are asserted LOW asynchronously when E110_HRST_L occurs and are deasserted synchronously with their respective clocks (E110_TRST_L with MII_TCLK and E110_RRST_L with MII_RCLK).

The MAC assumes that E110_HRST_L is asynchronous to all clocks. The minimum reset width is 400 ns for the 100 Mbits/s mode of operation and 4000 ns for the 10 Mbits/s mode.

E110_RPD[7:0]

E-110 Receive Data to Host **Input**

The E110_RPD[7:0] signals are the receive data bus. The signals hold the received data byte for two MII_RCLK clock cycles. The E110_RPD[7:0] signals are connected to the E-1110.

E110_RPSF **E-110 Receive Start of Frame** **Input**

The E-110 MAC asserts the E110_RPSF signal for one MII_RCLK clock cycle to indicate that the first byte of a receive packet is available to the host on E110_RPD[7:0].

E110_RPEF **E-110 Receive End of Frame** **Input**

The MAC asserts the E110_RPEF signal for one MII_RCLK clock cycle to indicate that the last byte of the receive packet is available to the E-1110 on E110_RPD[7:0].

E110_RPDV **E-110 Receive Packet Data Valid** **Input**

A packet transmission from the MAC receive function to the E-1110 begins when the receive function asserts the E110_RPSF and E110_RPDV signals at the first byte of the received packet data on E110_RPD[7:0] after removing the preamble and SFD. For subsequent data

bytes, the receive function asserts only the E110_RPDV signal until the last byte, when it asserts both E110_RPDV and E110_RPEF.

E110_RRST_L

Receive Reset **Input**

Other modules in an ASIC can use the E110_RRST_L signal as a host reset synchronized to the receive clock (MII_RCLK). Because the MII_RCLK clock can be slow with respect to a host reset pulse, or even stopped, the host reset signal (E110_HRST_L) is captured in the E-110 MAC receive function, which asserts E110_RRST_L asynchronously to MII-RCLK when E110_HRST_L occurs and deasserts E110_RRST_L synchronously on the positive transition of MII_RCLK.

E110_AUTOPAD_ENABLE

E-110 Autopadding Enable **Output**

The E110_AUTOPAD_ENABLE signal, when asserted, instructs the transmit function to pad packets of fewer than 60 bytes with a sufficient number of bytes of zero such that the minimum packet size (64 bytes, including data plus an FCS of 4 bytes) specified by IEEE 802.3 is maintained.

When deasserted, E110_AUTOPAD_ENABLE disables the padding of packets. For padding to take place, both E110_AUTOPAD_ENABLE and E110_CRCEN must be asserted. E110_AUTOPAD_ENABLE is synchronous with the rising edge of the MII_TCLK clock and may be asserted or deasserted when the transmit engine is idle (either during reset or when no packet is being transmitted).

E110_VLAN_PKT

E-110 VLAN Packet Detect **Input**

The MAC asserts the E110_VLAN_PKT signal to indicate that the current received packet has a valid Ethernet-encoded Tag Protocol Identifier (TPID). The encoded TPID for the MAC is 81-00. Assertion of E110_VLAN_PKT also indicates that the E110_VLAN_CFI, E110_VLAN_PRIORITY[2:0], and E110_VLAN_RPVID[11:0] signals are valid. The MAC deasserts E110_VLAN_PKT at the beginning of the next packet.

E110_VLAN_RPVID[11:0]

E-110 VLAN Packet ID **Input**

These signals contain the VLAN identifier extracted from the tag control information (TCI) field of the current received packet. If E110_VLAN_RPVID[11:0] is 0 and E110_VLAN_PKT is asserted, the current received packet is a priority-tagged frame. E110_VLAN_PKT must be asserted for E110_VLAN_RPVID[11:0] to be valid.

E110_VLAN_PRIORITY[2:0]

E-110 VLAN Packet Priority **Input**

These signals contain the user priority of the current received packet, extracted from the tag control information (TCI) field. E110_VLAN_PKT must be asserted for E110_VLAN_PRIORITY[2:0] to be valid.

E110_VLAN_CFI

E-110 VLAN Packet Canonical Format Indicator Input

The E110_VLAN_CFI signal, when asserted, indicates that the RIF field is present in the tag header. When the E110_VLAN_CFI signal is asserted, the NCFI bit in the RIF field determines whether any MAC address information in the MAC header is in noncanonical or canonical format. E110_VLAN_PKT must be asserted for CFI to be valid.

When deasserted, the E110_VLAN_CFI signal indicates that the RIF field is not present in the tag header, and that all MAC address information in the MAC header is in canonical format.

The E110_VLAN_CFI signal is extracted from the TCI field of the current received packet.

For more information regarding the RIF field in the tag header and the NCFI bit in that field, see the IEEE P802.1Q document.

E110_CRCEN **E-110 CRC Append Enable** **Output**

The E-1110 asserts the E110_CRCEN signal to instruct the MAC transmit function to append the FCS calculated by the MAC to the end of the transmitted data. When the E-1110 deasserts E110_CRCEN, the E-110 core still calculates the FCS of the transmitted packet data, but allows the FCS that comes from the E-1110 to be transmitted with the packet. The E-110 core checks the

E-1110-generated FCS to see if it is valid except when the host asserts the MTX_NOPRE signal. If the FCS is not valid, the E-110 core asserts the FCS error signal (TSV21, which is equivalent to the E-1110 TSV38 signal) in the Transmit Statistics Vector. E110_CRCEN is synchronous with the rising edge of the MII_TCLK clock and may be changed when the transmit engine is idle (either during reset or when no packet is being transmitted).

E110_TSVP_L **E-110 Transmit Status Vector Pulse** **Input**

The E110_TSVP_L signal is active-LOW. When asserted, it indicates that the E110_TSV[30:0] signals have been updated with a new transmit statistics vector. When deasserted, it indicates that there has been no update.

E110_TSV[30:0]

E-110 Transmit Status Vector **Input**

The E110_TSV[30:0] signals contain the transmit statistics information. The MAC function updates the E110_TSV[30:0] signals on the falling edge of the E110_TSVP_L signal. The MAC issues the statistics vector at the end of the final or only attempt to transmit each packet, whether the packet is transmitted or not. The E110_TSV[30:0] signals are stable until the subsequent E110_TSVP_L pulse. The condition associated with each signal is valid when the signal is HIGH.

The MAC function provides transmit statistics that can be used for RMON and SNMP. However, the MAC does not collect the statistics specifically mentioned in the RMON and SNMP specifications. The MAC provides basic per packet information that can be collected by an application built on top of the MAC. The collected information can then be used for RMON and SNMP.

The signals in E110_TSV[30:0] have the following functions:

TSV30 Transmit canceled because of excess deferral. Excess deferrals occur when the network is constantly busy (greater than 24,288 bit times when the host HUGE_PKT_EN signal is deasserted or greater than 524,288 bit times when HUGE_PKT_EN is asserted).

TSV29 Transmit dropped because of late collision. A late collision is one that occurs greater than 512 bit times into packet transmission.

TSV28 Transmit dropped because of excessive collisions (15 transmit retries).

TSV27 Transmit aborted because of underrun. If the host is unable to supply transmit packet data bytes in a timely manner to the E-110 core an underrun condition exists.

TSV26 Transmit aborted because of excessive length. The transmission is aborted if the packet exceeds 1518 bytes with the host HUGE_PKT_EN signal LOW, or 32 Kbytes with the HUGE_PKT_EN signal HIGH.

TSV25 Packet transmitted successfully.

TSV24 Packet deferred on transmission attempt. A packet is deferred when the network is busy.

TSV23 Broadcast packet transmitted or attempted.

TSV22 Multicast packet transmitted or attempted.

TSV21 FCS error seen on transmission attempt. When the host deasserts E110_CRCEN, indicating that the host provides the FCS field in transmitted packets, the MAC verifies the host FCS against its internally computed FCS. The E-110 core asserts the TSV21 signal to indicate a mismatch in the two FCSs. If the host asserts the E110_CRCEN signal, the MAC both calculates and provides the FCS in transmitted packets. In this case, the MAC does not assert the TSV21 signal.

TSV20 Late collision (a collision that occurs more than 512 bits times into the packet) seen on transmission attempt.

TSV19 (msb)	Collision count bit 3. The collision count can range from 0 to 15 for a packet ultimately transmitted, but can never be 16. After 15 retries, the packet is dropped because of excessive collisions. Bits 3 through 0 form a 4-bit binary counter, with the least significant bit = 1 collision.
TSV18	Collision count bit 2.
TSV17	Collision count bit 1.
TSV16 (lsb)	Collision count bit 0.
TSV15 (msb)	Packet length bit 15. The Packet Length bits indicate the length of the packet in bytes. The packet includes the Source Address, Destination Address, Data Length, Data, and FCS fields. Bits 15 through 0 form a 16-bit binary counter, with the least significant bit (TSV0) = 1 byte.
TSV14	Packet length bit 14.
TSV13	Packet length bit 13.
TSV12	Packet length bit 12.
TSV11	Packet length bit 11.
TSV10	Packet length bit 10.
TSV9	Packet length bit 9.
TSV8	Packet length bit 8.
TSV7	Packet length bit 7.
TSV6	Packet length bit 6.
TSV5	Packet length bit 5.
TSV4	Packet length bit 4.
TSV3	Packet length bit 3.
TSV2	Packet length bit 2.
TSV1	Packet length bit 1.
TSV0 (lsb)	Packet length bit 0.

E110_RSVP_L

E-110 Receive Status Vector PulseInput

The E110_RSVP_L signal is active-LOW. When the MAC asserts E110_RSVP_L, it indicates that the E110_RSV[27:0] signals have been updated with a new receive statistics vector. When deasserted, it indicates that there has been no update. The RSVP_L signal is also connected to the optional MAC control module core.

E110_RSV[27:0]

E-110 Receive Status Vector **Input**

The E110_RSV[27:0] signals contain the receive statistics vector and are updated on the falling edge of E110_RSVP_L. The statistics vector is issued at the end of any *minimally qualified receive event*. A minimally qualified receive event occurs when the MAC receives at least one nibble of data beyond a valid preamble and SFD.

The E110_RSV[27:0] signals are stable until the subsequent E110_RSVP_L pulse. The condition associated with each signal is valid when the signal is HIGH.

The receive statistics provided by the MAC function can be used for RMON and SNMP. However, the MAC does not collect the statistics specifically mentioned in the RMON and SNMP specifications. The MAC provides basic per packet information that can be collected by an application built on top of the MAC. The collected information can then be used for RMON and SNMP.

The signals in E110_RSV[27:0] have the following functions:

RSV27 Oversize packet received. This signal is asserted when the MAC receives a packet larger than 1518 bytes, or 1522 bytes when the host VLAN_EN signal is asserted in normal mode. When HUGE_PKT_EN is asserted, RSV27 is asserted if the packet received is larger than MAX_PKT_LEN[15:0].

RSV26 Receive false carrier sense status. When the MII_RXDV signal is deasserted, the MII_RXER signal is asserted, and MII_RXD[3:0] is 0b1110, this bit is set and reported with the next received packets.

RSV25 Carrier event previously seen. When the MAC asserts the RSV25 signal, it indicates that at some time since the last receive vector a carrier was detected, noted, and reported with this vector. The carrier event is not associated with this packet. A carrier event is defined as activity on the receive channel that does not result in a *packet receive attempt*. An example would be receiving a preamble but no SFD, or receiving more than seven octets of preamble. A carrier event can occur in either full- or half-duplex modes. If RSV25 is deasserted, a carrier was not detected.

RSV24 Good packet received. For 100 Mbits/s operation, a good packet has no 4B/5B receive code-group violations, no dribble nibbles, a valid FCS, and a proper packet length (at least 64 bytes but not more than 1518 bytes or 32 Kbytes). 4B/5B code-group violations include the following: 0b00100, 0b00000, 0b00001, 0b00010, 0b00011, 0b00101, 0b00110, 0b01000, 0b01100, 0b10000, and 0b11001. For 10 Mbits/s operation, a good packet has no *dribble nibbles*, a valid FCS, and a proper packet length (at least 64 bytes but not more than 1518 bytes or 32 Kbytes).

RSV23 Bad packet received. For 100 Mbits/s operation, a bad packet contains at least one of the following problems: 4B/5B code violations, bad FCS, less than 64 bytes (short packet), or more than 1518 bytes or 32 Kbytes (long packet). For 10 Mbits/s operation, a bad packet contains at least one of the following problems: A bad FCS, less than 64 bytes (short packet), or more than 1518 bytes or 32 Kbytes (long packet).

RSV22 *Long event* previously seen. When the MAC asserts the RSV22 signal, it indicates that at some time since the last receive vector a long event was detected, noted, and reported with this vector. The long event is not associated with this packet. A long event is activity on the network in excess of 50,000 bit times. A long event is not detected in full-duplex mode. If RSV22 is deasserted, it indicates that a long event was not seen.

RSV21 *Invalid preamble* content (not 55H) or code (0x50555) seen in the last reception.

RSV20 Broadcast packet received (all ones in the destination address field).

RSV19 Multicast packet received. (The first bit in the destination address field, which is also the least significant bit, is equal to a one - the least significant bit is transmitted first.)

RSV18 FCS error detected in the received packet. The FCS bytes in the received packet do not match those the MAC calculates at the destination while the packet is being received.

RSV17 Dribble nibble seen in the received packet. Each byte consists of two nibbles, so the number of received nibbles should always be even. If there is an odd number of nibbles, the last nibble is the dribble nibble.

RSV16 Receive code violation detected. There is a 4B/5B code violation. See the RSV24 signal description for a definition of code-group violations. The PHY asserts E1110_RX_ER whenever a receive code-group violation occurs.

RSV15 (msb) Packet length bit 15. If the host asserts the HUGE_PKT_EN signal, the Packet Length (Source Address, Destination Address, Data Length, Data, and FCS fields) as indicated by the Packet Length bits can be up to 32 Kbytes. Bits 15 through 0 form a 16-bit binary counter, with the least significant bit (RSV0) = 1 byte.

RSV14 Packet length bit 14.

RSV13 Packet length bit 13.

RSV12 Packet length bit 12.

RSV11 Packet length bit 11.

RSV10 Packet length bit 10.

RSV9 Packet length bit 9.

RSV8 Packet length bit 8.

RSV7 Packet length bit 7.

RSV6 Packet length bit 6.

RSV5 Packet length bit 5.

RSV4 Packet length bit 4.

RSV3 Packet length bit 3.

RSV2 Packet length bit 2.

RSV1 Packet length bit 1.

RSV0 (lsb) Packet length bit 0.

E110_HWD[10:0]

Host Random Number Generator **Output**

The E110_HWD[10:0] signals contain the value of the random number that the E-1110 loads into the MAC's Linear Feedback Shift Register (LFSR) to generate the random number sequence used in collision backoff timing. E110_HWD[10:0] must remain stable for two MII_TCLK cycles after E110_LRNG is asserted.

E110_LRNG

Load Random Number Generator **Output**

The E-1110 asserts the E110_LRNG signal to indicate that the E110_HWD[10:0] signals are valid and the MAC function should latch them. When the E-1110 deasserts E110_LRNG, the E110_HWD[10:0] signals are not valid. E110_LRNG must be synchronous to the MII_TCLK clock and at least one MII_TCLK clock cycle wide, which is 40 ns for 100 MHz operation and 400 ns for 10 MHz operation The E110_HWD[10:0] signals must be stable when the host pulses E110_LRNG.

E110_FC_FLS_CRS **Output**

E-110 False Carrier Sense (Backpressure Control)

The E-1110 may use the E-110 core E110_FC_FLS_CRS input pin to implement backpressure. Backpressure makes the medium look busy to other stations on the network who wish to send data to the E-110 core. The E-1110 asserts the E110_FC_FLS_CRS signal when a congestion threshold for the port's input buffer is reached. The E-1110 selects the congestion threshold in such a way that it leaves enough room in the buffer for the frame in progress. When the E110_FC_FLS_CRS pin is asserted, the E-110 core waits until 44 bit times after the medium becomes inactive (MII_CRS deasserted) and then starts sending out a false carrier data pattern (alternate ones and

zeroes). The E-110 core continues sending this data pattern as long as the host continues to assert the E110_FC_FLS_CRS signal. If the E-110 core is already sending out normal packet data on the MII, assertion of the E110_FC_FLS_CRS pin only goes into effect after the current transmission is completed. If the E-110 core is already sending out a false carrier data pattern on the MII, any transmit requests from the host are kept pending until the E110_FC_FLS_CRS pin is deasserted. It is the responsibility of the host to disable the *jabber* timer if the E-110 core is being used in the 10BASE-T mode and if the E110_FC_FLS_CRS pin is asserted for more than 20 ms. The E-110 core ignores collisions during transmission of data while the E110_FC_FLS_CRS pin is asserted. Standard management information related to the Ethernet interface is not affected by the E110_FC_FLS_CRS signal.

E110_CRCG **E-110 CRCG Output** **Input**

The E110_CRCG signal, when asserted, indicates that the E110_CRCO[9:1] signals are valid. The E110_CRCG signal, when deasserted, indicates that the E110_CRCO[9:1] signals are not valid.

E110_CRCO[9:1]

E-110 CRCO[9:1] **Input**

The E110_CRCO[9:1] signals reflect the state of the receive function FCS register after the first six bytes of the receive packet have been received. When the destination address bits that are received in the frame contain a multicast address, the E-110 core uses its built-in FCS generator to compute a nine-bit polynomial (the nine MSBs of the 32-bit FCS generator) from the incoming address. The value of this polynomial can be used as an index into an external multicast filter hash table.

MII_RXD[3:0] **MII Receive Nibble Data** **Output**

MII_RXD[3:0] consists of four data signals that the E-1110 drives synchronously on the rising edge of the MII_RCLK clock. For each MII_RCLK period in which MII_RXDV is asserted, the E-1110 transfers four bits of data over the MII_RXD[3:0] signals to the E-110 MAC. MII_RXD[0] is the least significant bit. When MII_RXDV

is deasserted, the MII_RXD[3:0] signals have no effect on the E-110 MAC.

For a frame to be correctly interpreted by the E-110 MAC, a completely formed SFD must be passed across the interface. A completely formed SFD is the octet 0b1010.1011, which follows seven identical octets of preamble (0b1010.1010).

MII_RXDV **MII Receive Data Valid** **Output**

The E-1110 asserts the MII_MRXDV signal to indicate that the E-1110 is presenting recovered and decoded nibbles on the MII_RXD[3:0] signals and that MII_RCLK is synchronous to the recovered data. The E-1110 asserts MII_RXDV synchronously on the rising edge of MII_RCLK. The E-1110 keeps MII_RXDV asserted from the first recovered nibble of the frame through the final recovered nibble and deasserts it prior to the first MII_RCLK that follows the final nibble. MII_RXDV encompasses the frame, starting no later than the SFD and excluding any *end of frame delimiter*. The E-1110 may also assert MII_RXDV for transferring a validly decoded preamble.

MII_RXER **MII Receive Error** **Output**

The E-1110 asserts the MII_RXER signal to indicate to the E-110 MAC that a media error (for example, a coding error) was detected somewhere in the frame presently being transferred from the E-1110 to the E-110 MAC. The E-1110 asserts MII_RXER synchronously on the rising edge of MII_RCLK for one or more MII_RCLK periods and then deasserts it. The E-1110 asserts MII_RXER for at least one MII_RCLK clock period during the frame.

MII_RCLK **MII Receive Clock.** **Output**

The MII_RCLK signal is a continuous clock that provides a timing reference for transfer of the MII_RXDV, MII_RXD[3:0], and MII_RXER signals from the E-1110 to the E-110 MAC.

MII_RCLK is also driven during test scan mode from the E1110_PHY_RCLK signal.

MII_CRS **MII Carrier Sense** **Output**

The E-1110 asserts the MII_CRS signal asynchronously with minimum propagation delay from the detection of a nonidle medium. The E-1110 deasserts MII_CRS when it detects an idle medium. The E-1110 also asserts MII_CRS with minimum propagation delay in response to MII_TXEN.

The E-1110 ensures that MCRS remains asserted throughout the duration of a collision condition.

MII_COL **MII Collision Detected** **Output**

The E-1110 asserts the MII_COL signal asynchronously with minimum delay from the start of a collision on the media. The PHY deasserts MII_ MCOL to indicate no collision. MII_MCOL is internally synchronized to the MII_TCLK clock and in the worst case may take up to two clock cycles to be detected by the E-110 MAC transmit function.

MII_TCLK **MII Transmit Clock.** **Output**

The MII_TCLK signal operates at a frequency of 25 or 2.5 MHz. MII_TCLK is a continuous clock that provides a timing reference for transfer of the MII_TXEN, MII_TXD[3:0], and MII_TXER signals from the E-110 MAC to the E-1110. The E-1110 provides MII_TCLK.

The MII_TCLK frequency is 25% of the transmit data rate. When the E-1110 operates at 100 Mbits/s, it provides an MII_TCLK frequency of 25 MHz ± 100 ppm. When the E-1110 operates at 10 Mbits/s, it provides a MII_TCLK frequency of 2.5 MHz ± 100 ppm. The duty cycle of the MII_TCLK signal is between 35% and 60%, inclusively.

MII_TCLK is also driven during test scan mode from E1110_MII_TX_CLK.

MII_TXEN **MII Transmit Enable** **Input**

The MII_TXEN signal indicates that the E-110 MAC is presenting MII_TXD[3:0] nibbles to the E-1110 for transmission. The MAC asserts MII_TXEN synchronously with the first nibble of the preamble. MII_TXEN remains asserted while all nibbles to be transmitted are presented to the MII. The MAC deasserts MII_TXEN prior to the first MII_TCLK following the final nibble of a frame. MII_TXEN is synchronous to the rising edge of MII_TCLK, and the E-1110 samples MII_TXEN synchronously.

MII_TXER **MII Transmit Coding Error** **Input**

The E-110 MAC function asserts the MII_TXER signal synchronously on the rising edge of MII_TCLK, and the E-1110 samples MII_TXER synchronously. When the MAC asserts MII_TXER for one MII_TCLK clock period while MII_TXEN is also asserted, MII_TXER causes the E-1110 to transmit one or more symbols that are not part of the valid data or delimiter set somewhere in the frame being transmitted to indicate that there has been a transmit coding error. If the MAC asserts the MII_TXER signal when the E-1110 is operating at 10 Mbits/s or when MII_TXEN is deasserted, the E-1110 must not allow the transmission of data to be affected.

MII_TXD[3:0] **MII Transmit Data** **Input**

The MII_TXD[3:0] signals are synchronous to the rising edge of MII_TCLK.

MII_MTXD[3:0] consists of four data signals that are synchronous to MII_TCLK. For each MII_TCLK period in which MII_TXEN is asserted, the E-1110 accepts the MII_TXD[3:0] signals for transmission. MII_TXD[0] is the least significant bit. When MII_TXEN is deasserted, the MII_TXD[3:0] signals have no effect on the E-1110.

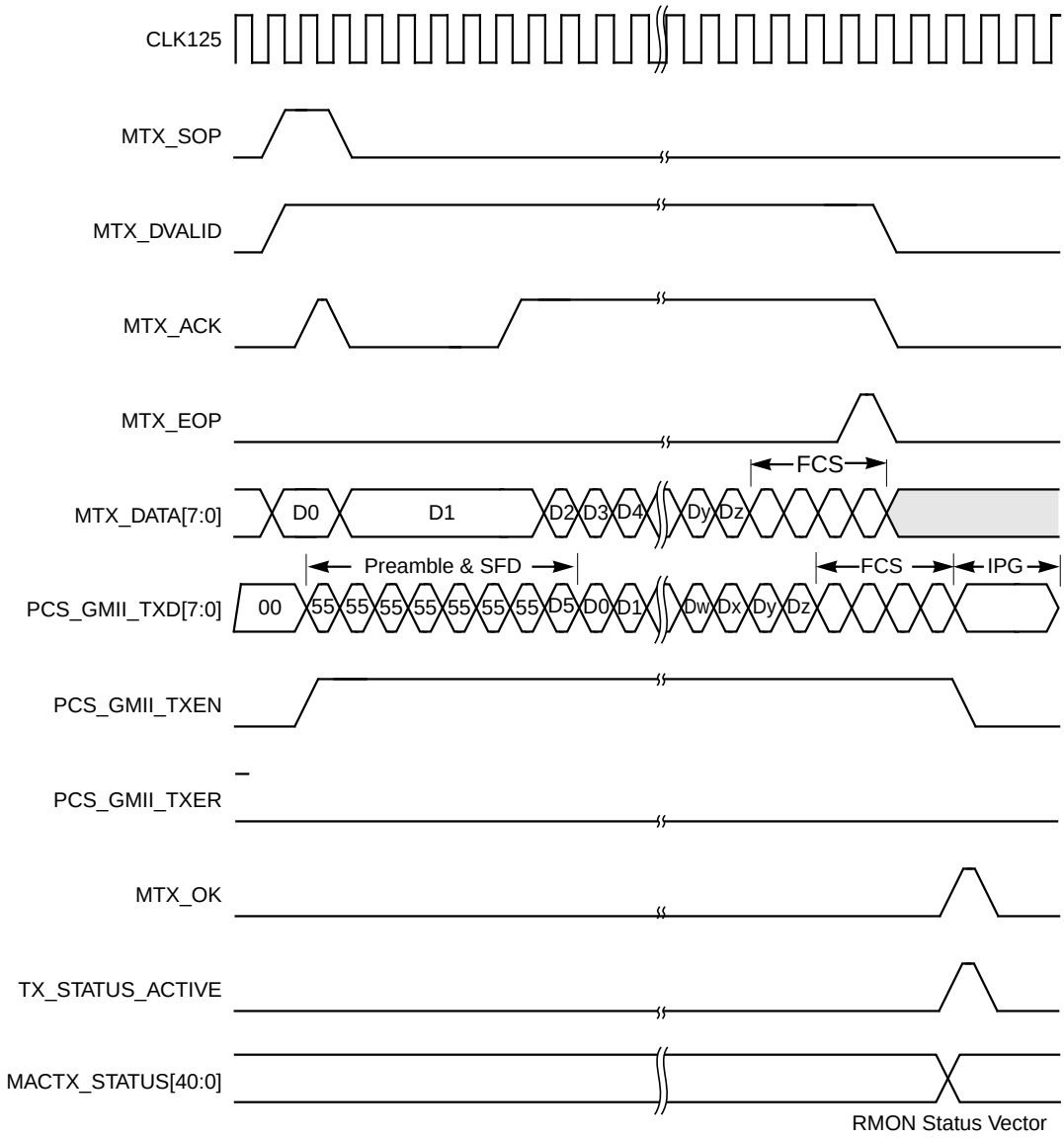
Chapter 4
Functional Timing

This chapter describes functional timing for various scenarios. The chapter contains the following sections:

4.1 1000 Mbits/s Transmit Packet Transfer

Figure 4.1 shows the typical timing for a 1000 Mbits/s transmit packet transfer.

Figure 4.1 Timing Diagram for 1000 Mbits/s Transmit Packet Transfer



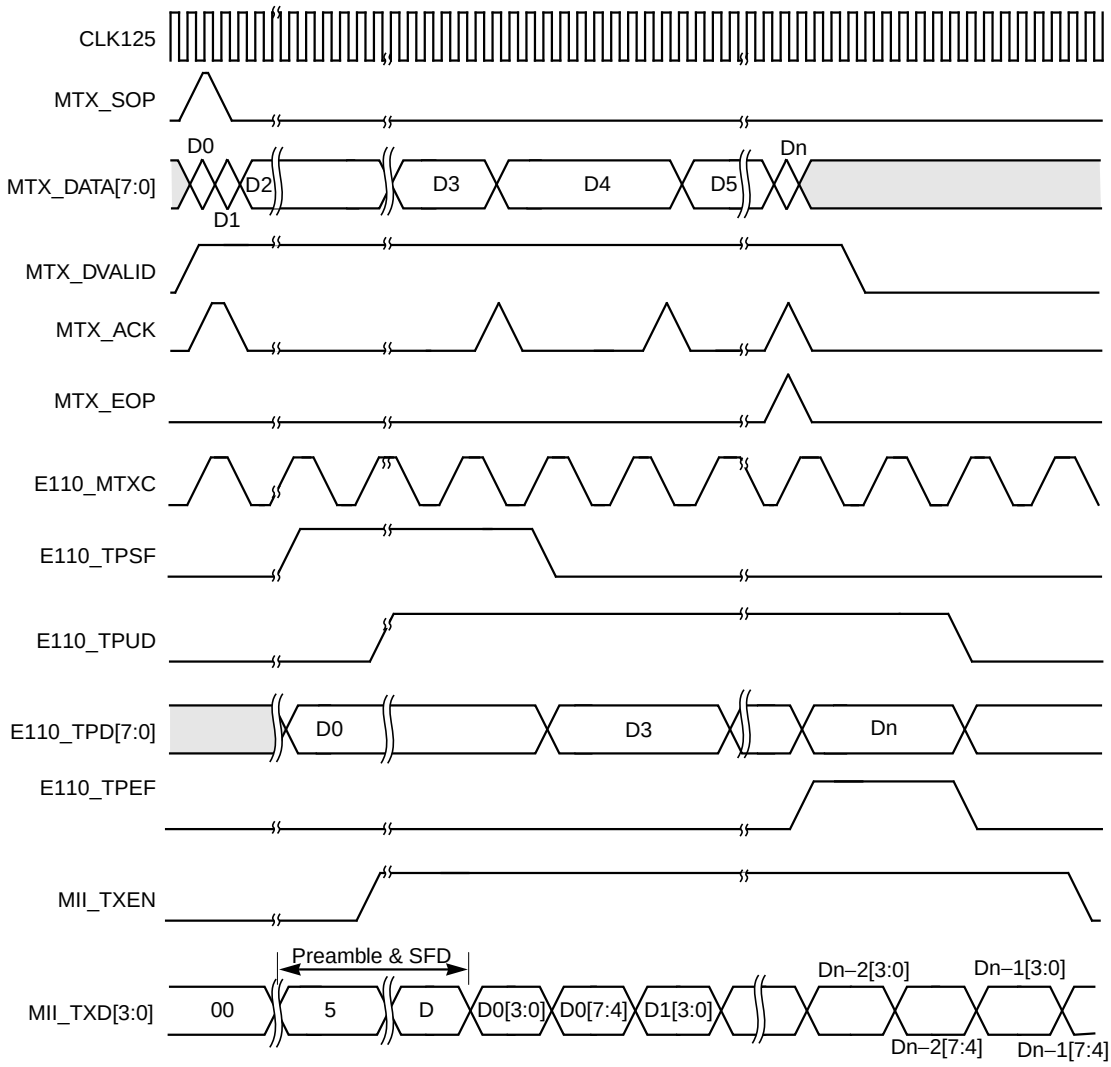
The host asserts MTX_SOP, MTX_DVALID, and drives valid data on the MTX_DATA[7:0] lines to start the transmit packet transfer. After the link is up and initialized, the transmit MAC asserts MTX_ACK to respond to the start of frame. As this point, the MAC transmit function is committed to transmitting a packet. The MAC then starts transmitting the preamble and SFD sequence. After the SFD is transmitted, the data transfer starts. At this point the MAC again starts asserting the MTX_ACK signal to the host. With every clock on which the MTX_ACK is sampled active, the host drives new data on MTX_DATA[7:0]. The end of the frame is indicated when MTX_EOP is asserted. At the end of a frame, the MAC samples signals such as AUTOPAD_ENABLE to perform padding for frames smaller than 64 bytes or MTX_APPEND_CRC to append an FCS. If these signals are inactive, the frame is transmitted just as it is received from the host.

After the frame is completely transmitted on the media, the MAC starts sending the IPG. It then responds to the host for the next transfer only at the end of the programmed IPG period. The MAC also asserts MTX_OK, indicating that the packet has been successfully transmitted. Assertion of the TX_STATUS_ACTIVE signal indicates that the new RMON Status Vector is now available on MACTX_STATUS[40:0] and that the host can sample it on rising edges of the CLK125 signal.

4.2 10/100 Mbits/s Transmit Packet Transfer

Figure 4.2 shows the typical timing for a 10/100 Mbits/s transmit packet transfer.

Figure 4.2 Timing Diagram for 10/100 Mbits/s Transmit Packet Transfer



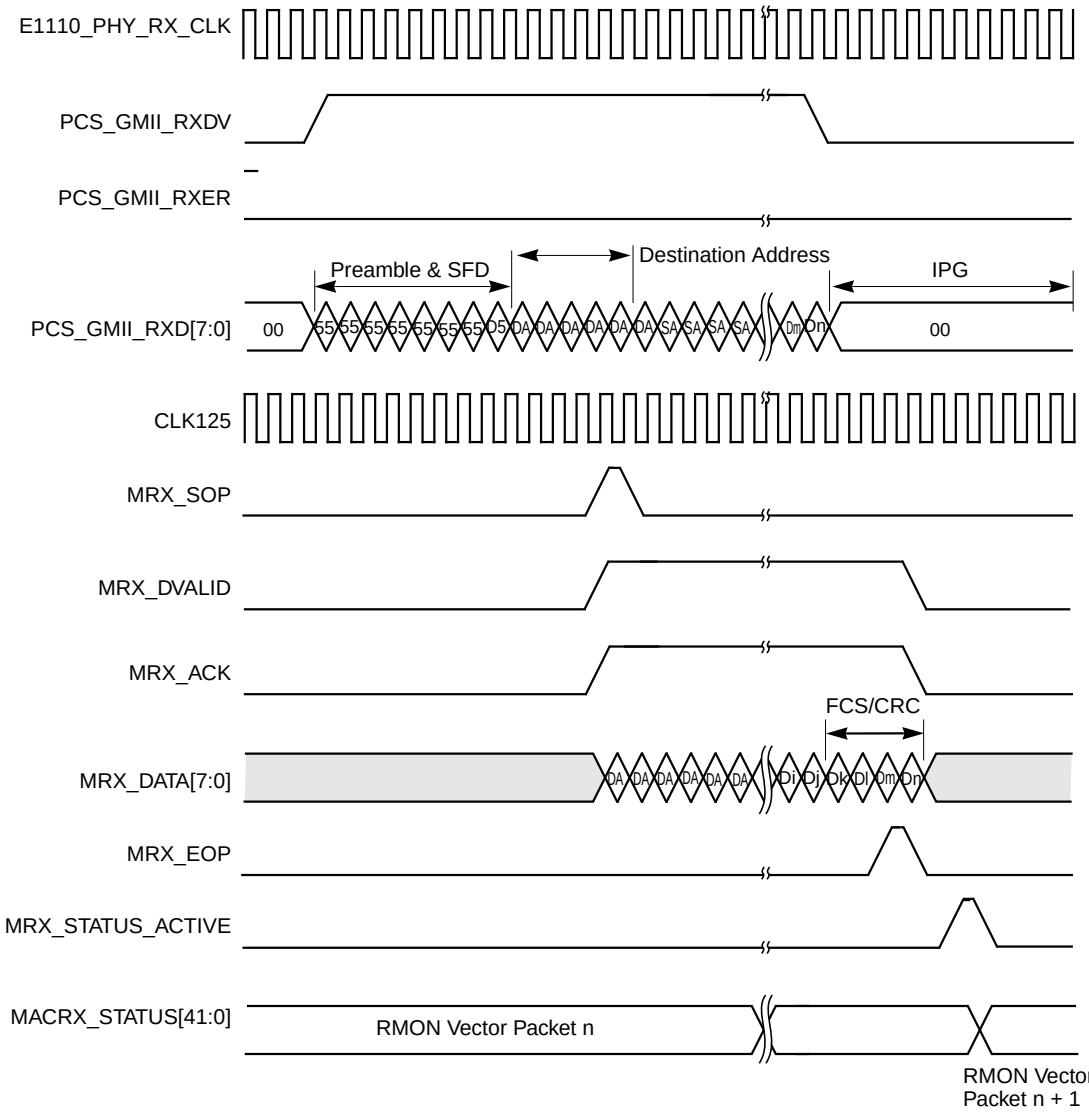
The host asserts MTX_SOP, MTX_DVALID, and drives valid data on the the MTX_DATA[7:0] lines to the E-1110. If the transmit MAC is idle, the E-1110 asserts MTX_ACK on consecutive clocks to read two bytes from the host and fill up its internal buffers. At the same time, the E-1110 asserts E110_TPSF, which serves as a synchronized version of start of frame to the E-110. The E-110 then waits for the media to be free, then starts transmitting the preamble and SFD sequence. At this point, the E-110 is committed to the transfer. The E-1110 then asserts E110_TPUD when it is about to send the nibble over the MII interface. Thereafter, the E-110 transmits one byte every two E110_MTXC clocks (one nibble every clock, due to the 4-bit MII interface). The E-1110 interface logic generates MTX_ACK on alternate clocks after synchronizing to E110_TPUD. MTX_ACK is asserted for only one clock. This sequence continues until the host reaches the end of the packet. After the E-1110 samples MTX_EOP, it asserts E110_TPEF, which indicates the end of the transfer. The E-110 then deasserts E110_TPUD in response to the assertion of the E110_TPEF signal.

Next, the E-110 asserts E110_TPDN signal, indicating that the frame has been transmitted successfully. This signal is synchronized to CLK125 and output as the MTX_OK signal. The RMON status vector from the E-110 core is also synchronized, then regenerated into a common E-1110 format and output as MACTX_STATUS[40:0] and TX_STATUS_ACTIVE. After the host asserts MTX_EOP, it can assert MTX_SOP to start the new cycle as early as the next clock. However, owing to the half-duplex nature of the media, it is recommended that the next transfer be initiated only after sampling MTX_OK asserted.

4.3 1000 Mbits/s Receive Packet Transfer

Figure 4.3 shows the typical timing for a 1000 Mbits/s receive packet transfer.

Figure 4.3 Timing Diagram for 1000 Mbits/s Receive Packet Transfer



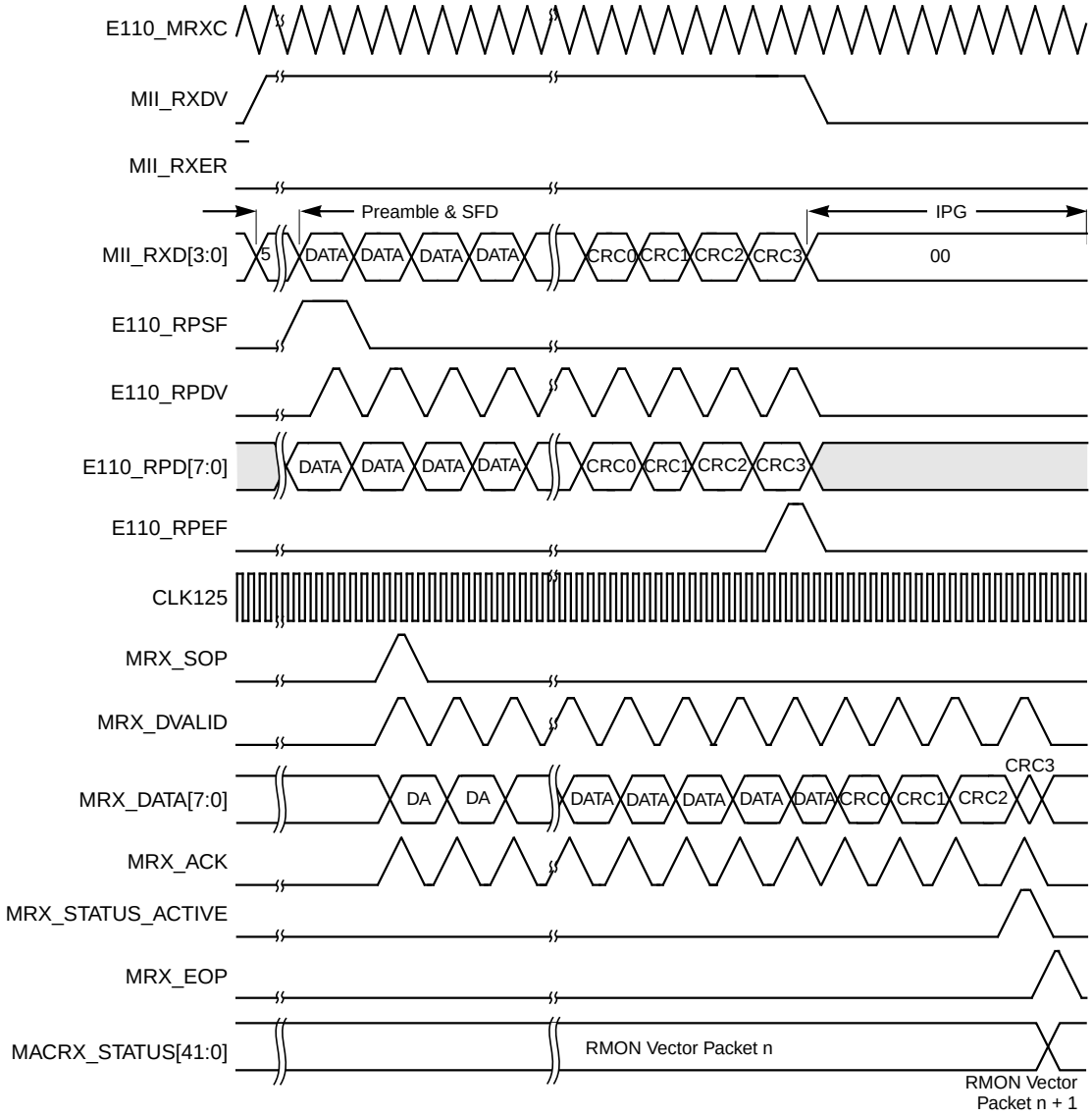
The GMII interface starts receiving the preamble, SFD, and packet data with the 125 MHz E1110_PHY_RX_CLK. The PCS_GMII_RXD[7:0] data (for TBI mode) or E1110_RXD[9:0] data (for GMII mode) is synchronous to this clock. The data and clock are then fed to an elasticity FIFO where the received GMII data is synchronized to the local 125 MHz clock on which the host interface and receive MAC engine operates. After the E-1110 detects the preamble and SFD, it asserts MRX_SOP and MRX_DVALID while driving the first octet (MRX_DATA[7:0]) of the packet onto the host receive interface bus. The data is then continuously output on every rising edge of CLK125. Any time the MRX_ACK signal is sampled deasserted, the E-1110 declares an underrun condition and aborts the receive operation on the next clock. The E-1110 indicates the aborted condition with the deassertion of MRX_DVALID. However, the E-1110 still asserts MRX_EOP to indicate the end of packet condition of the currently aborted packet.

The E-1110 asserts MRX_STATUS and drives the MACRX_STATUS[41:0] lines, which contain the new RMON vector. The RMON vector value is updated when MRX_STATUS is active; otherwise, the value remains unchanged. The host can sample the status vector to decide whether to drop or accept the packet. A number of configuration conditions have an influence over the status vector. If VLAN is enabled, the E-1110 detects the VLAN frame ID and outputs the VLAN_PKT signal. It also outputs the VLAN_ID, and VLAN_PRIORITY, and VLAN_CFI signals from the 16-bit VLAN tag. In VLAN mode, VLAN frames up to 1522 bytes are not declared as oversized. If the MAC receives a packet larger than the allowed maximum size, the frame is truncated and declared as a jabber frame. In such cases, the MRX_EOP signal is asserted with the last byte transferred to the host, even though technically it is not an end of frame.

4.4 10/100 Mbits/s Receive Packet Transfer

Figure 4.3 shows the typical timing for a 10/100 Mbits/s receive packet transfer.

Figure 4.4 Timing Diagram for 10/100 Mbits/s Receive Packet Transfer



Data received by the E-1110 over the PHY interface is passed on to the E-110 over the MII interface bus. The E-110 then extracts the received packet and sends it back to the E-1110 so it can be routed to the host through the E-110 host interface. The E-1110 samples the E110_RPSF, E110_RPDV, and E110_RPEF signals along with E110_RPD[7:0]. These signals are buffered and synchronized to the 125-MHz clock through through interface logic. The E-1110 then asserts MRX_SOP, MRX_DVALID, and drives the MRX_DATA[7:0] data lines after proper synchronization logic and passes the data received from the E-110 to the host. The E-1110 indicates the end of packet transfer with the assertion of MRX_EOP. The RMON vector is received from the E-110 over the E110_RSV[27:0] lines when E110_RSVP_L is valid. The vector is synchronized and regenerated into a common E-1110 format and output over MACRX_STATUS[41:0] when the RX_STATUS_ACTIVE signal is active. If the E-1110 is configured to strip off the FCS or CRC, the E-1110 terminates the receive packet transfer four octets before the end of the frame, effectively removing the FCS from the received packet.

Signals such as MRX_BYTE7, MRX_BCO, MRX_MCO, CRCG, and CRCO[8:0] are asserted after the E-1110 outputs the complete destination address. The E-1110 updates or changes the MRX_BCO, MRX_MCO, and CRCO[8:0] signals when the MRX_BYTE7 and CRCG signals are asserted. A number of configuration conditions have an influence over the status vector. If VLAN is enabled, the E-1110 detects the VLAN frame ID and outputs the VLAN_PKT signal. It also outputs the VLAN_ID, VLAN_PRIORITY, and VLAN_CFI signals from the 16-bit VLAN tag. In VLAN mode, VLAN frames up to 1522 bytes are not declared as oversized. If the MAC receives a packet larger than the allowed maximum size, the frame is truncated and declared as a jabber frame. In such cases, MRX_EOP is asserted with the last byte transferred to the host, even though technically it is not an end of frame.

Chapter 5
Specifications

This chapter provides specifications for the E-1110 core, including the AC timing, AC loading, and a pin summary.

This chapter has the following sections:

5.1 Derivation of AC Timing and Loading

Delay predictor software is included with every core LSI Logic delivers for incorporation into an ASIC. This software generates an input loading report so you can plan for buffer strengths that drive core inputs.

A ramp time violation report is generated when you integrate the core into the rest of logic and run simulations. The report indicates if a core output is heavily loaded. Adjust buffering, wire length, and other parameters to eliminate the violation.

There are no specific numbers in this chapter for AC timing and loading because these parameters depend upon the technology used and the design layout.

5.2 E-1110 Core Pin Summary

Table 5.1 summarizes the E-1110 core input and output signals and their associated clock domains. The table provides the signal names and types for both outputs and inputs.

Table 5.1 E-1110 Core Pin Summary

Signal Name	Description	Type	Active	Clock Domain
Receive Function Signals				
MRX_SOP	Receive packet Start of Packet	Output	High	Clk125
MRX_DVALID	Receive packet data valid on MRX_DATA bus.	Output	High	Clk125
MRX_DATA[7:0]	Receive packet data	Output	–	Clk125
MRX_EOP	Receive packet End of packet	Output	High	Clk125
MRX_ACK	Receive packet data acknowledge	Input	High	Clk125
MRX_ABORT	Receive Packet Abort	Input	High	Clk125
MRX_BYTE7	Byte 7 Valid Indicator	Output	High	Clk125
MRX_BCO	Broadcast Receive packet Indication	Output	High	Clk125
MRX_MCO	Multicast Receive packet Indication	Output	High	Clk125
CRCG	CRCO Output Good	Output	High	Clk125
CRCO[8:0]	CRCO output - contains the most significant 9 bits of the CRC of the destination address of the received packet.	Output	High	Clk125
ACCEPT_CRC	Accept packets with CRC errors	Input	High	Clk125
ACCEPT_RUNT	Accept short packets. (<64 bytes)	Input	High	Clk125
ACCEPT_LONG	Accept oversized packets. (>MAX_PKT_LEN or 1518/1522 bytes)	Input	High	Clk125
ACCEPT_CTRL	Accept MAC control packets.	Input	High	Clk125
RX_STRIP_CRC	Strip CRC from the received packet.	Input	High	Clk125

Table 5.1 E-1110 Core Pin Summary (Cont.)

Signal Name	Description	Type	Active	Clock Domain
Transmit Function Signals				
MTX_SOP	MAC Transmit Start of Packet	Input	High	Clk125
MTX_DVALID	Transmit packet data valid	Input	High	Clk125
MTX_DATA[7:0]	Transmit Data	Input	–	Clk125
MTX_EOP	MAC Transmit End of Packet	Input	High	Clk125
MTX_APPEND_CRC	Append CRC to the transmit packet	Input	High	Clk125
MTX_HIGH_PRIORITY	Transmit packet with high priority (override the pause state of MAC).	Input	High	Clk125
MTX_ACK	Transmit Data Acknowledge	Output	High	Clk125
MTX_OK	Transmit packet successful/OK	Output	High	Clk125
MTX_RETRY	Transmit packet retry (due to collisions)	Output	High	Clk125
MTX_ABORT	Transmit packet abort (excess collisions/late collisions/transmit underrun)	Output	High	Clk125
MTX_PAUSED	Transmit MAC in the paused state	Output	High	Clk125
E110_BACKPRESS	E-110 Backpressure Flow control from host	Input	High	Clk125
E110_FULL_DUPLEX	10/100 MAC in full-duplex operation	Input	High	Clk125
HUGE_PKT_EN	Huge Packet Enable (enables significance of value programmed in MAX_PKT_LEN)	Input	High	Clk125
MAX_PKT_LEN[15:0]	Maximum Packet Length (maximum value of 9,000 can be programmed).	Input	–	Clk125
MTX_NOPRE	Transmit packet with no preamble and SFD	Input	High	Clk125
AUTOPAD_ENABLE	Transmit packet autopadding enable	Input	High	Clk125
E1000_IFG_OFFSET[1:0]	Gigabit MAC Inter Frame Gap	Input	–	Clk125
FLCTRL_CFG[1:0]	Flow Control Configuration.	Input	High	Clk125
FLOWCTRL_EN	Transmit MAC Flow Control Enable.	Input	High	Clk125

Table 5.1 E-1110 Core Pin Summary (Cont.)

Signal Name	Description	Type	Active	Clock Domain
PAUSE_TIME[15:0]	Pause Time in multiples of 512-bit times	Input	–	Clk125
MAC_ADDRESS[47:0]	MAC Port Destination Address	Input	–	Clk125
PREAMBLE_LENGTH[3:0]	Gigabit MAC Preamble Length excluding the SFD.	Input	–	Clk125
VLAN Signals				
VLAN_EN	VLAN packets reception Enable	Input	High	Clk125
VLAN_PKT	VLAN Packet Detected on Receive MAC	Output	High	Clk125
VLAN_RPVID[11:0]	Extracted VLAN Received packet ID	Output	–	Clk125
VLAN_PRIORITY[2:0]	Extracted VLAN packet priority	Output	–	Clk125
VLAN_CFI	Extracted VLAN packet CFI bit	Output	High	Clk125
Status and Configuration Signals				
MACTX_STATUS[40:0]	MAC Transmit Status Vector	Output	–	Clk125
TX_STATUS_ACTIVE	Transmit Status Vector Updated	Output	High	Clk125
MACRX_STATUS[41:0]	MAC Receive Status Vector	Output	–	Clk125
RX_STATUS_ACTIVE	Receive Status Vector Updated	Output	High	Clk125
MAC_SPEED_MODE	MAC Speed Mode configuration.	Input	–	Clk125
MAC_PHY_MODE	MAC PHY Mode Selection	Input	–	Clk125
DA_MATCH	MAC Control Frame Destination Address Match for reserved multicast address or input unicast MAC address.	Output	High	Clk125
HOST_HWD[10:0]	Host Write Data used for E-110 core random number/delay generation in half duplex mode.	Input	–	Clk125
HOST_LRNG	Load Random Number Generator	Input	High	Clk125
Clock and Reset Signals				
CLK125	125MHz MAC & Host packet interface clock (also Scan Mode Clock Input)	Input	–	SCAN

Table 5.1 E-1110 Core Pin Summary (Cont.)

Signal Name	Description	Type	Active	Clock Domain
HARDRESET	Hardware System Reset. This is an asynchronous reset signal to the entire MAC and associated logic. It must be asserted for a minimum of 5000 ns.	Input	High	Asynchronous
E110_MTXC	E-110 transmit clock (also Scan Mode Clock Input)	Input	–	SCAN
E110_MRXC	E-110 receive clock (also Scan Mode Clock Input)	Input	–	SCAN
Scan Signals				
TEST_MODE	Test Mode Enable	Input	High	SCAN
TEST_SE	Test Scan Enable	Input	High	SCAN
TEST_SO	Test Scan Output	Output	High	SCAN
TEST_SI	Test Scan Input	Input	High	SCAN
Gigabit PCS Interface Signals				
PCS_GMII_TCLK	PCS GMII Interface TX Clock 125 MHz	Output	–	-
PCS_GMII_TXEN	PCS GMII Interface TX_EN	Output	High	PCS_GMII_ TCLK
PCS_GMII_TXER	PCS GMII Interface TX_ER	Output	High	PCS_GMII_ TCLK
PCS_GMII_TXD[7:0]	PCS GMII Interface TX Data	Output	–	PCS_GMII_ TCLK
PCS_GMII_COL	PCS GMII Interface COL (collision)	Input	High	
PCS_GMII_CRS	PCS GMII Interface CRS (carrier sense)	Input	High	
PCS_GMII_RCLK	PCS GMII Interface Receive Clock 125 MHz	Input	High	PCS_GMII_ RCLK
PCS_GMII_RXDV	PCS GMII Interface RX_DV	Input	High	PCS_GMII_ RCLK
PCS_GMII_RXER	PCS GMII Interface RX_ER	Input	High	PCS_GMII_ RCLK
PCS_GMII_RXD[7:0]	PCS GMII Interface RX Data	Input	–	PCS_GMII_ RCLK

Table 5.1 E-1110 Core Pin Summary (Cont.)

Signal Name	Description	Type	Active	Clock Domain
PCS_TBI_RCLK	PCS TBI interface RCLK (this clock is also driven out from E1110_TBI_RCLK as Scan clock in the scan mode)	Output	–	SCAN
PCS_TBI_RCLKN	PCS TBI interface RCLKN (this clock is also driven out from E1110_TBI_RCLKN as Scan clock in the scan mode)	Output	–	SCAN
PCS_TBI_RXD[9:0]	PCS TBI interface RXDATA	Output	–	PCS_TBI_ RCLK/CLKN
PCS_TBI_TXD[9:0]	PCS TBI interface TXDATA	Input	–	PCS_TBI_ TCLK
PCS_TBI_TCLK	PCS TBI interface TCLK	Input	–	–
E-110 Core Interface Signals				
MII_COL	MII interface COL (collision detect) signal	Output	High	ASYNC
MII_CRS	MII interface Carrier sense Signal (CRS)	Output	High	MII_RCLK
MII_RCLK	MII interface Receive Clock (this clock is driven out from E1110_PHY_RX_CLK in the Scan Mode for E-110 testing)	Output	–	- SCAN
MII_RXDV	MII interface RX_DV or RX data valid signal	Output	High	MII_RCLK
MII_RXER	MII Interface RX Error Signal	Output	High	MII_RCLK
MII_RXD[3:0]	MII RX Data from the PHY	Output	–	MII_RCLK
MII_TCLK	MII interface Transmit Clock (this clock is driven out from E1110_MII_TCLK in the Scan Mode for E-110 testing)	Output	–	SCAN
MII_TXEN	MII Interface TX_EN signal	Input	High	MII_TCLK
MII_TXER	MII Interface TX_ER signal	Input	High	MII_TCLK
MII_TXD[3:0]	MII Interface TX Data	Input	–	MII_TCLK
E110_TPUR	E-110 Transmit data underrun error	Output	High	E110_MTXC
E110_HRST_L	Asynchronous active-LOW system Reset.	Output	Low	ASYNC
E110_TPSF	E-110 Transmit packet start of frame	Output	High	E110_MTXC

Table 5.1 E-1110 Core Pin Summary (Cont.)

Signal Name	Description	Type	Active	Clock Domain
E110_TPEF	E-110 Transmit packet End of frame	Output	High	E110_MTXC
E110_TPUD	E-110 Transmit packet Data Used	Input	High	E110_MTXC
E110_AUTOPAD_ENABLE	E-110 Auto padding enable (synchronized)	Output	High	E110_MTXC
E110_TPD[7:0]	E-110 Transmit Data from host	Output	High	E110_MTXC
E110_RPSF	E-110 Receive start of frame	Input	High	E110_MRXC
E110_RPEF	E-110 receive end of frame	Input	High	E110_MRXC
E110_RPDV	E-110 receive data valid for host bus interface	Input	High	E110_MRXC
E110_CRCG	E-110 CRCG Output	Input	High	E110_MRXC
E110_CRCO[9:1]	E-110 CRCO[9:1] Output	Input	–	E110_MRXC
E110_FC_FLS_CRS	E-110 False carrier sense input from the flow control module	Output	High	E110_MTXC
E110_TPRT	E-110 transmit retry due to collision/error	Input	High	E110_MTXC
E110_VLAN_PKT	E-110 VLAN Packet Detect	Input	High	E110_MRXC
E110_VLAN_RPVID[11:0]	E-110 VLAN Packet ID	Input	High	E110_MRXC
E110_VLAN_PRIORITY[2:0]	E-110 VLAN Packet PRIORITY	Input	High	E110_MRXC
E110_VLAN_CFI	E-110 VLAN Packet CFI Bit	Input	High	E110_MRXC
E110_TPAB	E-110 transmit abort due to excess collision, deferring, and so on	Input	High	E110_MTXC
E110_TPDN	E-110 transmit done	Input	High	E110_MTXC
E110_TRST_L	E-110 active-LOW transmit interface reset synchronized to E-110 TX clock	Input	Low	E110_MTXC
E110_RRST_L	E-110 active-LOW receive interface reset synchronized to E-110 RX clock	Input	Low	E110_MRXC
E110_LRNG	Host Latch Random Number Generator (synchronized)	Output	High	E110_MTXC
E110_HWD[10:0]	Host Random Number Generator value (latched)	Output	High	E110_MTXC

Table 5.1 E-1110 Core Pin Summary (Cont.)

Signal Name	Description	Type	Active	Clock Domain
E110_CRCEN	E-110 CRC Append Enable	Output	High	E110_MTXC
E110_TSVP_L	E-110 transmit status active-LOW pulse	Input	Low	E110_MTXC
E110_RSVP_L	E-110 receive status active-LOW pulse	Input	Low	E110_MRXC
E110_TSV[30:0]	E-110 transmit status vector	Input	–	E110_MTXC
E110_RSV[27:0]	E-110 receive status vector	Input	–	E110_MRXC
E110_RPD[7:0]	E-110 receive data to host	Input	–	E110_MRXC
PHY Interface Signals				
E1110_PHY_TCLK	Transmit Clock to the PHY in GMII/TBI Mode	Output	–	–
E1110_TXD[7:0]	Transmit Data in MII/GMII/TBI Mode to the PHY	Output	–	E1110_PHY_TCLK/E1110_MII_TCLK
E1110_TXD[8]/ E1110_TX_EN	Transmit Data[8] in TBI Mode/ Transmit Enable in MII/GMII Mode.	Output	–	E1110_PHY_TCLK/E1110_MII_TCLK
E1110_TXD[9]/ E1110_TX_ER	Transmit Data[9] in TBI Mode/ Transmit Error in MII/GMII Mode.	Output	–	E1110_PHY_TCLK/E1110_MII_TCLK
E1110_COL	Collision Detect (MII/GMII Mode)	Input	–	ASYNC
E1110_CRS	Carrier Sense (MII/GMII Mode)	Input	–	E1110_PHY_RCLK
E1110_PHY_RCLK	E1110 PHY receive clock (also Scan Mode Clock Input)	Input	–	SCAN
E1110_MII_TCLK	E1110 MII Interface transmit clock (also Scan Mode Clock Input)	Input	–	SCAN

Table 5.1 E-1110 Core Pin Summary (Cont.)

Signal Name	Description	Type	Active	Clock Domain
E1110_TBI_RCLK	E1110 TBI interface Receive clock. (RBC0) (also Scan Mode Clock Input if PCS is used)	Input	–	SCAN
E1110_TBI_RCLKN	E1110 TBI interface Receive clock. (RBC1) (also Scan Mode Clock Input if PCS is used)	Input	–	SCAN
E1110_RXD[7:0]	MII/GMII/TBI receive data	Input	–	E1110_PHY_RX_CLK/ E1110_TBI_RX_CLK/CLKN
E1110_RXD[8]/ E1110_RX_DV	Receive Data[8] in TBI Mode/ Receive data valid in MII/GMII Mode.	Input	High	E1110_PHY_RX_CLK/ E1110_TBI_RX_CLK/CLKN
E1110_RXD[9]/ E1110_RX_ER	Receive Data[9] in TBI Mode/ Receive data Error in MII/GMII Mode.	Input	High	E1110_PHY_RX_CLK/ E1110_TBI_RX_CLK/ CLKN
SIGNAL_DETECT	Signal Detect for GMII/TBI	Input	HIGH	ASYNC

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