SONY **CXB1134Q**

22, 15, 7 Stage Descrambler

Advanced Information

Description

CXB1134Q is an Ultra high speed bipolar monolithic descrambler IC, which operates in 22, 15, 7-bit length mode.

This IC is used with the CXB1133Q scramblar/maximal code sequence generator.

Features

- Ultra high speed operation by high-speed bipolar process. fclk=1.6GHz (Typ.)
- Variable bit length : 22, 15, 7-bit
- I/O levels and supply voltage are ECL 100K compatible.
- Open input pins are pulled down to Low level.
- Output pins are open emitter type.

Function

- 22, 15, 7-bit length descramblar

Structure

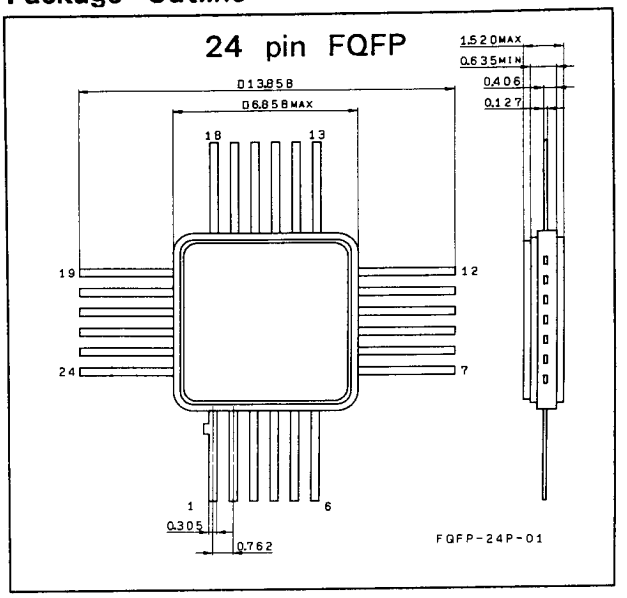
Bipolar silicon monolithic IC

Applications

- High speed optical communication systems and other high speed digital signal processing systems.

Package Outline

Unit : mm



Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{EE}	−7.0 to +0.5	V
• Input voltage	V_{IN}	V_{EE} to +0.5	V
• Output current	Io	−50 to 0	mA
• Junction temperature	Tj	150	°C
• Storage temperature	Tstg	−55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{EE}	−4.5±0.3	V
• Operating temperature	Topr	−20 to +75	°C

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Electrical Characteristics

Transfer characteristics

V_{EE} = −4.5V, V_{TT} = −2.0V, Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input voltage	V_{IH}		−1165		−880	mV
	V_{IL}		−1810		−1475	mV
Output voltage	V_{OH}	R_L = 50 Ω to V_{TT}	−1035			mV
	V_{OL}				−1610	mV
Input current	I_{IH}	V_{IN} = V_{IH} (Max.)			110	μA

DC characteristics

V_{EE} = −4.5V, V_{TT} = −2.0V, Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}			−118		mA
Reference voltage	V_{BB}			−1.32		V

AC characteristics

V_{EE} = −4.5V, V_{TT} = −2.0V, Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Max. operating frequency	fmax	R_L = 50 Ω to V_{TT}		1.6		GHz

Pin Description

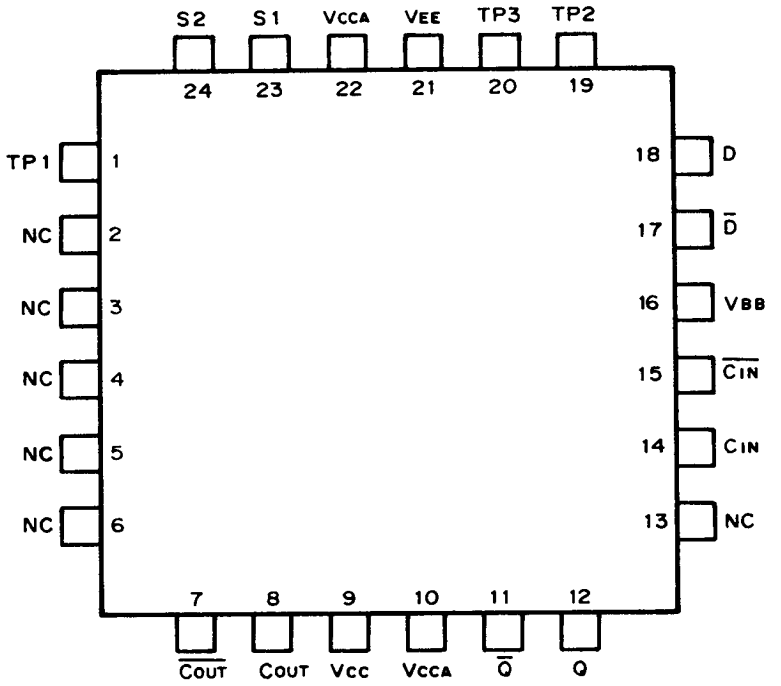
No.	Symbol	I/O	Description
1	TP1	I	(Test point) *1
2	NC	—	Non connection
3	NC	—	Non connection
4	NC	—	Non connection
5	NC	—	Non connection
6	NC	—	Non connection
7	$\overline{C_{OUT}}$	O	Complementary clock output
8	C_{OUT}	O	Clock output
9	V_{CC}	—	Positive power supply (GND)
10	V_{CCA}	—	Output devices positive power supply (GND)
11	$\overline{Q}$	O	Complementary data output
12	Q	O	Data output
13	NC	—	Non connection
14	C_{IN}	I	Clock input
15	$\overline{C_{IN}}$	I	Inverting clock input
16	V_{BB}	O	Reference bias supply voltage (−1.32V)
17	$\overline{D}$	I	Inverting data input
18	D	I	Data input
19	TP2	O	(Test point) *1
20	TP3	O	(Test point) *1
21	V_{EE}	—	Negative power supply (−4.5V)
22	V_{CCA}	—	Output devices positive power supply (GND)
23	S1	I	Bit length select input
24	S2	I	Bit length select input

*1 : Test point pin must be left open.

Stage Select

S1	S2	Operation
L	L	22 Stage
L	H	15 Stage
H	L	7 Stage
H	H	

Pin Configuration (Top View)



Block Diagram