NEC

User's Manual

AS17707

DEVICE FILE
PC-9800 Series (MS-DOS™) Base
IBM PC/AT™ (PC DOS™) Base

Target Device

μPD17704
μPD17705
μPD17707
μPD17708
μPD17709
μPD17717
μPD17718
μPD17719

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Major Revisions in This Version

Page	Contents
Throughout	The following products have been added as target devices. • μPD17704 • μPD17705 • μPD17717 • μPD17718 • μPD17719
Throughout	The following tools have been developed. • RA17K Assembler Package • *emIC-17K*
p. 31	Description on **CHAPTER 4 LOAD MODULE FILE FORMAT** has been changed

The mark ★ shows major revised points.

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INTRODUCTION

Device files are files that store unique data (device data) dependent upon the 17K Series devices. This information is required when using the following 17K Series software development tools.

★ • RA17K assembler package
• *SIMPLEHOST*™
★ • *emIC-17K*™

The following files are contained in AS17707.

Device File	File Name	Target Device
AS17707	D17704.DEV	μPD17704
	D17705.DEV	μPD17705
	D17707.DEV	μPD17707
	D17708.DEV	μPD17708
	D17709.DEV	μPD17709
	D17717.DEV	μPD17717
	D17718.DEV	μPD17718
	D17719.DEV	μPD17719

For details of the RA17K assembler package and the use of device files contained in the μPD17704, 17705, 17707, 17708, 17709, 17717, 17718 and 17719, refer to the **RA17K Assembler Package User's Manual (U10305E)**.

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CHAPTER 1 DEVICE DATA

During assembly, the device files provide the following data related to the device.

(1) Program memory (ROM) capacity

μPD17704

- Segment 0 : 8192 × 16 bits (0000H to 1FFFH)

total 8192 × 16 bits

μPD17705, 17707 and 17717

- Segment 0 : 8192 × 16 bits (0000H to 1FFFH)
- Segment 1 : 4096 × 16 bits (2000H to 2FFFH)

total 12288 × 16 bits

μPD17708, 17718

- Segment 0 : 8192 × 16 bits (0000H to 1FFFH)
- Segment 1 : 8192 × 16 bits (2000H to 3FFFH)

total 16384 × 16 bits

μPD17709, 17719

- Segment 0 : 8192 × 16 bits (0000H to 1FFFH)
- Segment 1 : 8192 × 16 bits (2000H to 3FFFH)

total 16384 × 16 bits

(2) Data memory (RAM) capacity

μPD17704, 17705 : 672 × 4 bits (BANK0 to BANK5)
μPD17707, 17708, 17717, 17718: 1120 × 4 bits (BANK0 to BANK9)
μPD17709, 17719 : 1776 × 4 bits (BANK0 to BANK15)

(3) Usable instructions

See **CHAPTER 2 INSTRUCTION SET.**

(4) Register file, port register, and peripheral register read and write data

See **CHAPTER 3 RESERVED SYMBOLS.**

(5) Reserved symbols

See **CHAPTER 3 RESERVED SYMBOLS.**

(6) Device files, device numbers, and SE board numbers

Device files register a device number for each device and a SE board number to indicate the best SE board for developing various products. These device files are also included in ICE files and PRO files output by the RA17K assembler package. These device files are used when the in-circuit emulator checks the development environment and during mask order checking.

Table 1-1. Relations among Device Files, Device Numbers, and SE Board Numbers

Device File	Device Name	Device Number	SE Board Number	SE Board
AS17707	μPD17704	5F	55	SE-17709
	μPD17705	5E		
	μPD17707	57		
	μPD17708	56		
	μPD17709	55		
	μPD17717	5D		
	μPD17718	5C		
	μPD17719	5B		

CHAPTER 2 INSTRUCTION SET

2.1 Instruction Set Summary

b_{14} - b_{11} \ b_{15}		0		1	
BIN	HEX				
0000	0	ADD	r, m	ADD	m, #n4
0001	1	SUB	r, m	SUB	m, #n4
0010	2	ADDC	r, m	ADDC	m, #n4
0011	3	SUBC	r, m	SUBC	m, #n4
0100	4	AND	r, m	AND	m, #n4
0101	5	XOR	r, m	XOR	m, #n4
0110	6	OR	r, m	OR	m, #n4
0111	7	INC INC RORC MOVT PUSH POP GET PUT PEEK POKE BR CALL SYSCAL[Note] RET RETSK RETI EI DI STOP HALT NOP	AR IX r DBF, @AR AR AR DBF, p p, DBF WR, rf rf, WR @AR @AR entry s h 		
1000	8	LD	r,m	ST	m, r
1001	9	SKE	m, #n4	SKGE	m, #n4
1010	A	MOV	@r,m	MOV	m, @r
1011	B	SKNE	m, #n4	SKLT	m, #n4
1100	C	BR	addr (page 0)	CALL	addr (page 0)
1101	D	BR	addr (page 1)	MOV	m, #n4
1110	E	BR	addr (page 2)	SKT	m, #n
1111	F	BR	addr (page 3)	SKF	m, #n

★ **Note** SYSCAL cannot be used because there is no segment 1 area in the μPD17704.

2.2 Legend

AR : Address register
ASR : Address stack register indicated by stack pointers
addr : Program memory address (lower 11 bits)
BANK : Bank register
CMP : Compare flag
CY : Carry flag
DBF : Data buffer
entry : Program memory address (bit 10 to bit 8, bit 3 to bit 0)
$entry_H$: Program memory address (bit 10 to bit 8)
$entry_L$: Program memory address (bit 3 to bit 0)
h : Halt release conditions
INTEF : Interrupt enable flag
INTR : Register that is automatically saved to a stack when an interrupt occurs
INTSK : Interrupt stack register
IX : Index register
MP : Data memory low address pointer
MPE : Memory pointer enable flag
m : Data memory address indicated by m_R and mc
m_R : Data memory row address (high)
mc : Data memory column address (low)
n : Bit position (4 bits)
n4 : Immediate data (4 bits)
PAGE : Page (Bit 12, 11 of program counter)
PC : Program counter
p : Peripheral address
p_H : Peripheral address (higher 3 bits)
p_L : Peripheral address (lower 4 bits)
r : General register column address
rf : Register file address
rf_R : Register file low address (higher 3 bits)
rfc : Register file column address (lower 4 bits)
SGR : Segment register (bit 13 of program counter)
SP : Stack pointer
s : Stop release conditions
WR : Window register
(×) : × indicates addressed contents

2.3 Instruction List

Instruction Set	Mnemonic	Operand	Operation	Instruction Code			
				Op Code	Operand		
Addition	ADD	r, m	(r) ← (r) + (m)	00000	m_R	mc	r
		m, #n4	(m) ← (m) + n4	10000	m_R	mc	n4
	ADDC	r, m	(r) ← (r) + (m) + CY	00010	m_R	mc	r
		m, #n4	(m) ← (m) + n4 + CY	10010	m_R	mc	n4
	INC	AR	AR ← AR + 1	00111	000	1001	0000
		IX	IX ← IX + 1	00111	000	1000	0000
Subtraction	SUB	r, m	(r) ← (r) − (m)	00001	m_R	mc	r
		m, #n4	(m) ← (m) − n4	10001	m_R	mc	n4
	SUBC	r, m	(r) ← (r) − (m) − CY	00011	m_R	mc	r
		m, #n4	(m) ← (m) − n4 − CY	10011	m_R	mc	n4
Logical operation	OR	r, m	(r) ← (r) ∨ (m)	00110	m_R	mc	r
		m, #n4	(m) ← (m) ∨ n4	10110	m_R	mc	n4
	AND	r, m	(r) ← (r) ∧ (m)	00100	m_R	mc	r
		m, #n4	(m) ← (m) ∧ n4	10100	m_R	mc	n4
	XOR	r, m	(r) ← (r) ∀ (m)	00101	m_R	mc	r
		m, #n4	(m) ← (m) ∀ n4	10101	m_R	mc	n4
Decision	SKT	m, #n	CMP ← 0, if (m) ∧ n = n, then skip	11110	m_R	mc	n
	SKF	m, #n	CMP ← 0, if (m) ∧ n = 0, then skip	11111	m_R	mc	n
Comparison	SKE	m, #n4	(m) − n4, skip if zero	01001	m_R	mc	n4
	SKNE	m, #n4	(m) − n4, skip if not zero	01011	m_R	mc	n4
	SKGE	m, #n4	(m) − n4, skip if not borrow	11001	m_R	mc	n4
	SKLT	m, #n4	(m) − n4, skip if borrow	11011	m_R	mc	n4
Rotation	RORC	r	→ CY → (r) $_{b3}$ → (r) $_{b2}$ → (r) $_{b1}$ → (r) $_{b0}$ →	00111	000	0111	r
Transfer	LD	r, m	(r) ← (m)	01000	m_R	mc	r
	ST	m, r	(m) ← (r)	11000	m_R	mc	r
	MOV	@r, m	if MPE = 1 : (MP, (r)) ← (m) if MPE = 0 : (BANK, m_R, (r)) ← (m)	01010	m_R	mc	r
		m, @r	if MPE = 1 : (m) ← (MP, (r)) if MPE = 0 : (m) ← (BANK, m_R, (r))	11010	m_R	mc	r
		m, #n4	(m) ← n4	11101	m_R	mc	n4
	MOVT	DBF, @AR	SP ← SP−1, ASR ← PC, PC ← AR, DBF ← (PC), PC ← ASR, SP ← SP + 1	00111	000	0001	0000
	PUSH	AR	SP ← SP −1, ASR ← AR	00111	000	1101	0000
	POP	AR	AR ← ASR, SP ← SP + 1	00111	000	1100	0000
	GET	DBF, p	DBF ← (p)	00111	p_H	1011	p_L
	PUT	p, DBF	(p) ← DBF	00111	p_H	1010	p_L
	PEEK	WR, rf	WR ← (rf)	00111	rf_R	0011	rfc
	POKE	rf, WR	(rf) ← WR	00111	rf_R	0010	rfc

Instruction Set	Mnemonic	Operand	Operation	Instruction Code			
				Op Code	Operand		
Branch	BR	addr	$PC_{10-0} \leftarrow$ addr, PAGE $\leftarrow$ 0	01100	addr		
			$PC_{10-0} \leftarrow$ addr, PAGE $\leftarrow$ 1	01101			
			$PC_{10-0} \leftarrow$ addr, PAGE $\leftarrow$ 2	01110			
			$PC_{10-0} \leftarrow$ addr, PAGE $\leftarrow$ 3	01111			
		@AR	PC $\leftarrow$ AR	00111	000	0100	0000
Subroutine	CALL	addr	SP $\leftarrow$ SP – 1, ASR $\leftarrow$ PC $PC_{11} \leftarrow$ 0, $PC_{10-0} \leftarrow$ addr	11100	addr		
		@AR	SP $\leftarrow$ SP – 1, ASR $\leftarrow$ PC PC $\leftarrow$ AR	00111	000	0101	0000
	SYSCAL[Note]	entry	SP $\leftarrow$ SP – 1, ASR $\leftarrow$ PC, SGR $\leftarrow$ 1 $PC_{12,11} \leftarrow$ 0, $PC_{10-8} \leftarrow$ $entry_H$, $PC_{7-4} \leftarrow$ 0, $PC_{3-0} \leftarrow$ $entry_L$	00111	$entry_H$	0010	$entry_L$
	RET		PC $\leftarrow$ ASR, SP $\leftarrow$ SP + 1	00111	000	1110	0000
	RETSK		PC $\leftarrow$ ASR, SP $\leftarrow$ SP + 1 and skip	00111	001	1110	0000
	RETI		PC $\leftarrow$ ASR, INTR $\leftarrow$ INTSK, SP $\leftarrow$ SP + 1	00111	010	1110	0000
Interrupt	EI		INTEF $\leftarrow$ 1	00111	000	1111	0000
	DI		INTEF $\leftarrow$ 0	00111	001	1111	0000
Others	STOP	s	STOP	00111	010	1111	s
	HALT	h	HALT	00111	011	1111	h
	NOP		No operation	00111	100	1111	0000

★ **Note** SYSCAL cannot be used because there is no segment 1 area in the μPD17704.

2.4 Macro Instructions Bundled with Assembler (RA17K)

Legend

flag n : FLG-type symbol

n : Bit No.

< > : Contents between < > symbols can be omitted.

	Mnemonic	Operand	Operation	n
Bundled macros	SKTn	flag 1, ··· flag n	if (flag 1) to (flag n) = all "1", then skip	1 ≤ n ≤ 4
	SKFn	flag 1, ··· flag n	if (flag 1) to (flag n) = all "0", then skip	1 ≤ n ≤ 4
	SETn	flag 1, ··· flag n	(flag 1) to (flag n) ← 1	1 ≤ n ≤ 4
	CLRn	flag 1, ··· flag n	(flag 1) to (flag n) ← 0	1 ≤ n ≤ 4
	NOTn	flag 1, ··· flag n	if (flag n) = "0", then (flag n) ← 1 if (flag n) = "1", then (flag n) ← 0	1 ≤ n ≤ 4
	INITFLG	<NOT> flag 1, ··· <<NOT> flag n>	if description = NOT flag n, then (flag n) ← 0 if description = flag n, then (flag n) ← 1	1 ≤ n ≤ 4
	BANKn		(BANK) ← n	**Note 1**
Extended instruction	BRX	Label	Jump Label	–
	CALLX	function-name	CALL sub-routine	–
	SYSCALX[Note 2]	function-name or expression	CALL system sub-routine	–
	INITFLGX	<NOT/INV> flag 1, ··· <NOT/INV> flag n	if description = NOT (or INV) flag, (flag) ← 0 if description = flag, (flag) ← 1	n ≤ 4

★ **Notes 1.** 0 ≤ n ≤ 6 : μPD17704, 17705

0 ≤ n ≤ 10 : μPD17707, 17708, 17717, 17718

0 ≤ n ≤ 15 : μPD17709, 17719

★ **2.** SYSCALX cannot be used there is no segment 1 area in the μPD17704.

[MEMO]

CHAPTER 3 RESERVED SYMBOLS

The symbols defined for the μPD17704, 17705, 17707, 17708, 17709, 17717, 17718 and 17719 are described on the following pages.

These symbols are listed below.

- Data buffer (DBF)
- System register (SYSREG)
- Port register
- Register file (Control register)
- Peripheral hardware register
- Others

3.1 Data Buffer (DBF)

Symbol Name	Attribute	Value	R/W	Description
DBF3	MEM	0.0CH	R/W	DBF bits 15 to 12
DBF2	MEM	0.0DH	R/W	DBF bits 11 to 8
DBF1	MEM	0.0EH	R/W	DBF bits 7 to 4
DBF0	MEM	0.0FH	R/W	DBF bits 3 to 0

3.2 System Register (SYSREG)

Symbol Name	Attribute	Value	R/W	Description
AR3[Note]	MEM	0.74H	R/W	Address register bits 15 to 12
AR2	MEM	0.75H	R/W	Address register bits 11 to 8
AR1	MEM	0.76H	R/W	Address register bits 7 to 4
AR0	MEM	0.77H	R/W	Address register bits 3 to 0
WR	MEM	0.78H	R/W	Window register
BANK	MEM	0.79H	R/W	Bank register
IXH	MEM	0.7AH	R/W	Index register bits 10 to 8
MPH	MEM	0.7AH	R/W	Memory pointer bits 6 to 4
MPE	FLG	0.7AH.3	R/W	Memory pointer enable flag
IXM	MEM	0.7BH	R/W	Index register bits 7 to 4
MPL	MEM	0.7BH	R/W	Memory pointer bits 3 to 0
IXL	MEM	0.7CH	R/W	Index register bits 3 to 0
RPH	MEM	0.7DH	R/W	General register pointer bits 6 to 3
RPL	MEM	0.7EH	R/W	General register pointer bits 2 to 0
BCD	FLG	0.7EH.0	R/W	BCD operation flag
PSW	MEM	0.7FH	R/W	Program status word
CMP	FLG	0.7FH.3	R/W	Compare flag
CY	FLG	0.7FH.2	R/W	Carry flag
Z	FLG	0.7FH.1	R/W	Zero flag
IXE	FLG	0.7FH.0	R/W	Index enable flag

★ **Note** AR3 is fixed to 0 in the μPD17704.

3.3 Port Register

Symbol Name	Attribute	Value	R/W	Description
P0A3	FLG	0.70H.3	R/W	Port 0A bit 3
P0A2	FLG	0.70H.2	R/W	Port 0A bit 2
P0A1	FLG	0.70H.1	R/W	Port 0A bit 1
P0A0	FLG	0.70H.0	R/W	Port 0A bit 0
P0B3	FLG	0.71H.3	R/W	Port 0B bit 3
P0B2	FLG	0.71H.2	R/W	Port 0B bit 2
P0B1	FLG	0.71H.1	R/W	Port 0B bit 1
P0B0	FLG	0.71H.0	R/W	Port 0B bit 0
P0C3	FLG	0.72H.3	R/W	Port 0C bit 3
P0C2	FLG	0.72H.2	R/W	Port 0C bit 2
P0C1	FLG	0.72H.1	R/W	Port 0C bit 1
P0C0	FLG	0.72H.0	R/W	Port 0C bit 0
P0D3	FLG	0.73H.3	R Note	Port 0D bit 3
P0D2	FLG	0.73H.2	R Note	Port 0D bit 2
P0D1	FLG	0.73H.1	R Note	Port 0D bit 1
P0D0	FLG	0.73H.0	R Note	Port 0D bit 0
P1A3	FLG	1.70H.3	R Note	Port 1A bit 3
P1A2	FLG	1.70H.2	R Note	Port 1A bit 2
P1A1	FLG	1.70H.1	R Note	Port 1A bit 1
P1A0	FLG	1.70H.0	R Note	Port 1A bit 0
P1B3	FLG	1.71H.3	R/W	Port 1B bit 3
P1B2	FLG	1.71H.2	R/W	Port 1B bit 2
P1B1	FLG	1.71H.1	R/W	Port 1B bit 1
P1B0	FLG	1.71H.0	R/W	Port 1B bit 0
P1C3	FLG	1.72H.3	R Note	Port 1C bit 3
P1C2	FLG	1.72H.2	R Note	Port 1C bit 2
P1C1	FLG	1.72H.1	R Note	Port 1C bit 1
P1C0	FLG	1.72H.0	R/W	Port 1C bit 0

Note These ports are input-only ports. The assembler and in-circuit emulator will not output error messages even if an instruction to output from these ports is written. Also, if the instruction is actually executed on a device, the operation will have no change.

Symbol Name	Attribute	Value	R/W	Description
P1D3	FLG	1.73H.3	R/W	Port 1D bit 3
P1D2	FLG	1.73H.2	R/W	Port 1D bit 2
P1D1	FLG	1.73H.1	R/W	Port 1D bit 1
P1D0	FLG	1.73H.0	R/W	Port 1D bit 0
P2A2	FLG	2.70H.2	R/W	Port 2A bit 2
P2A1	FLG	2.70H.1	R/W	Port 2A bit 1
P2A0	FLG	2.70H.0	R/W	Port 2A bit 0
P2B3	FLG	2.71H.3	R/W	Port 2B bit 3
P2B2	FLG	2.71H.2	R/W	Port 2B bit 2
P2B1	FLG	2.71H.1	R/W	Port 2B bit 1
P2B0	FLG	2.71H.0	R/W	Port 2B bit 0
P2C3	FLG	2.72H.3	R/W	Port 2C bit 3
P2C2	FLG	2.72H.2	R/W	Port 2C bit 2
P2C1	FLG	2.72H.1	R/W	Port 2C bit 1
P2C0	FLG	2.72H.0	R/W	Port 2C bit 0
P2D2	FLG	2.73H.2	R/W	Port 2D bit 2
P2D1	FLG	2.73H.1	R/W	Port 2D bit 1
P2D0	FLG	2.73H.0	R/W	Port 2D bit 0
P3A3	FLG	3.70H.3	R/W	Port 3A bit 3
P3A2	FLG	3.70H.2	R/W	Port 3A bit 2
P3A1	FLG	3.70H.1	R/W	Port 3A bit 1
P3A0	FLG	3.70H.0	R/W	Port 3A bit 0
P3B3	FLG	3.71H.3	R/W	Port 3B bit 3
P3B2	FLG	3.71H.2	R/W	Port 3B bit 2
P3B1	FLG	3.71H.1	R/W	Port 3B bit 1
P3B0	FLG	3.71H.0	R/W	Port 3B bit 0
P3C3	FLG	3.72H.3	R/W	Port 3C bit 3
P3C2	FLG	3.72H.2	R/W	Port 3C bit 2
P3C1	FLG	3.72H.1	R/W	Port 3C bit 1
P3C0	FLG	3.72H.0	R/W	Port 3C bit 0
P3D3	FLG	3.73H.3	R/W	Port 3D bit 3
P3D2	FLG	3.73H.2	R/W	Port 3D bit 2
P3D1	FLG	3.73H.1	R/W	Port 3D bit 1
P3D0	FLG	3.73H.0	R/W	Port 3D bit 0

3.4 Register File (Control Registers)

(1) μPD17704, 17705, 17707, 17708 and 17709

Symbol Name	Attribute	Value	R/W	Description
SP	MEM	0.81H	R/W	Stack pointer
WDTCK	MEM	0.82H	R/W	Watchdog timer clock selection flag (can be set only once after power application)
WDTCK1	FLG	0.82H.1	R/W	Watchdog timer clock selection flag (can be set only once after power application)
WDTCK0	FLG	0.82H.0	R/W	Watchdog timer clock selection flag (can be set only once after power application)
WDTRES	FLG	0.83H.3	R/W	Watchdog timer counter reset (when read: 0)
DBFSP	MEM	0.84H	R	DBF stack pointer
SPRSEL	MEM	0.85H	R/W	Stack overflow/underflow reset selection flag (can be set only once after power application)
ISPRES	FLG	0.85H.1	R/W	Stack overflow/underflow reset selection flag (can be set only once after power application)
ASPRES	FLG	0.85H.0	R/W	Stack overflow/underflow reset selection flag (can be set only once after power application)
CECNT3	FLG	0.86H.3	R/W	CE reset timer carry counter
CECNT2	FLG	0.86H.2	R/W	CE reset timer carry counter
CECNT1	FLG	0.86H.1	R/W	CE reset timer carry counter
CECNT0	FLG	0.86H.0	R/W	CE reset timer carry counter
MOVTSEL1	FLG	0.87H.1	R/W	MOVT bit selection flag
MOVTSEL0	FLG	0.87H.0	R/W	MOVT bit selection flag
SYSRSP	MEM	0.88H	R	System register stack pointer
SIO0WSTT	FLG	0.8AH.0	R	Serial interface 0 wait status judgement flag
SBMD	FLG	0.8BH.2	R/W	I^2C bus slave transmission operation mode selection flag
SIO0CK1	FLG	0.8BH.1	R/W	Serial interface 0 I/O clock selection flag
SIO0CK0	FLG	0.8BH.0	R/W	Serial interface 0 I/O clock selection flag
SIO0IMD3	FLG	0.8CH.3	R/W	Serial interface 0 interrupt mode selection flag (dummy)
SIO0IMD2	FLG	0.8CH.2	R/W	Serial interface 0 interrupt mode selection flag (dummy)
SIO0IMD1	FLG	0.8CH.1	R/W	Serial interface 0 interrupt mode selection flag
SIO0IMD0	FLG	0.8CH.0	R/W	Serial interface 0 interrupt mode selection flag
SIO0SF8	FLG	0.8DH.3	R	8-count detection flag of serial interface 0 clock counter
SIO0SF9	FLG	0.8DH.2	R	9-count detection flag of serial interface 0 clock counter
SBSTT	FLG	0.8DH.1	R	Serial interface 0 (I^2C mode) communication status detection flag (1: Start condition detected)
SBBSY	FLG	0.8DH.0	R	Serial interface 0 (I^2C mode) communication status detection flag (1: Start condition detected, 0: Stop condition detected)
SBACK	FLG	0.8EH.3	R/W	Serial interface 0 (I^2C mode) ACK signal setting/detection flag
SIO0NWT	FLG	0.8EH.2	R/W	Serial interface 0 wait status setting/detection flag (1: Wait status released (no wait))
SIO0WRQ1	FLG	0.8EH.1	R/W	Bit 1 of serial interface 0 wait condition setting flag
SIO0WRQ0	FLG	0.8EH.0	R/W	Bit 0 of serial interface 0 wait condition setting flag

Symbol Name	Attribute	Value	R/W	Description
SIO0CH	FLG	0.8FH.3	R/W	Serial interface 0 mode selection flag
SB	FLG	0.8FH.2	R/W	Serial interface 0 mode selection flag
SIO0MS	FLG	0.8FH.1	R/W	Serial interface 0 shift clock mode selection flag
SIO0TX	FLG	0.8FH.0	R/W	Serial interface 0 transmission (TX)/reception (RX) selection flag
PLLSCNF	FLG	0.90H.3	R/W	Swallow counter least significant bit setting flag
PLLMD1	FLG	0.90H.1	R/W	PLL mode selection flag
PLLMD0	FLG	0.90H.0	R/W	PLL mode selection flag
PLLRFCK3	FLG	0.91H.3	R/W	PLL reference frequency selection flag
PLLRFCK2	FLG	0.91H.2	R/W	PLL reference frequency selection flag
PLLRFCK1	FLG	0.91H.1	R/W	PLL reference frequency selection flag
PLLRFCK0	FLG	0.91H.0	R/W	PLL reference frequency selection flag
PLLUL	FLG	0.92H.0	R&Reset	PLL unlock FF flag
BEEP1SEL	FLG	0.93H.1	R/W	BEEP1/general-purpose port pin function selection flag
BEEP0SEL	FLG	0.93H.0	R/W	BEEP0/general-purpose port pin function selection flag
BEEP1CK1	FLG	0.94H.3	R/W	BEEP1 clock selection flag
BEEP1CK0	FLG	0.94H.2	R/W	BEEP1 clock selection flag
BEEP0CK1	FLG	0.94H.1	R/W	BEEP0 clock selection flag
BEEP0CK0	FLG	0.94H.0	R/W	BEEP0 clock selection flag
WDTCY	FLG	0.96H.0	R	Watchdog timer/stack pointer reset status detection flag
BTM0CY	FLG	0.97H.0	R	Basic timer 0 carry flag
BTM0CK1	FLG	0.98H.1	R/W	Basic timer 0 clock selection flag
BTM0CK0	FLG	0.98H.0	R/W	Basic timer 0 clock selection flag
SIO1TS	FLG	0.9DH.3	R/W	Serial interface 1 transmission/reception start flag
SIO1HIZ	FLG	0.9DH.2	R/W	Serial interface 1/general-purpose port selection flag
SIO1CK1	FLG	0.9DH.1	R/W	Serial interface 1 I/O clock selection flag
SIO1CK0	FLG	0.9DH.0	R/W	Serial interface 1 I/O clock selection flag
IEG4	FLG	0.9EH.3	R/W	Edge direction selection flag for INT4 pin interrupt request detection
INT4SEL	FLG	0.9EH.2	R/W	INT4 pin interrupt request flag setting disable
IEG3	FLG	0.9EH.1	R/W	Edge direction selection flag for INT3 pin interrupt request detection
INT3SEL	FLG	0.9EH.0	R/W	INT3 pin interrupt request flag setting disable
IEG2	FLG	0.9FH.2	R/W	Edge direction selection flag for INT2 pin interrupt request detection
IEG1	FLG	0.9FH.1	R/W	Edge direction selection flag for INT1 pin interrupt request detection
IEG0	FLG	0.9FH.0	R/W	Edge direction selection flag for INT0 pin interrupt request detection
FCGCH1	FLG	0.0A0H.1	R/W	FCG channel selection flag
FCGCH0	FLG	0.0A0H.0	R/W	FCG channel selection flag
IFCGOSTT	FLG	0.0A1H.0	R	IF counter gate status detection flag (1: Open, 0: Closed)

Symbol Name	Attribute	Value	R/W	Description
IFCMD1	FLG	0.0A2H.3	R/W	IF counter mode selection flag (10: AMIF, 11: FCG)
IFCMD0	FLG	0.0A2H.2	R/W	IF counter mode selection flag (00: CGP, 11: FMIF)
IFCCK1	FLG	0.0A2H.1	R/W	IF counter clock selection flag
IFCCK0	FLG	0.0A2H.0	R/W	IF counter clock selection flag
IFCSTRT	FLG	0.0A3H.1	W	IF counter count start flag
IFCRES	FLG	0.0A3H.0	W	IF counter reset flag
ADCCH3	FLG	0.0A4H.3	R/W	A/D converter channel selection flag (dummy)
ADCCH2	FLG	0.0A4H.2	R/W	A/D converter channel selection flag
ADCCH1	FLG	0.0A4H.1	R/W	A/D converter channel selection flag
ADCCH0	FLG	0.0A4H.0	R/W	A/D converter channel selection flag
ADCMD	FLG	0.0A5H.2	R/W	A/D converter compare mode selection flag
ADCSTT	FLG	0.0A5H.1	R	A/D converter operation status detection flag (0: End of conversion, 1: Conversion in progress)
ADCCMP	FLG	0.0A5H.0	R	A/D converter compare result detection flag
PWMBIT	FLG	0.0A6H.2	R/W	PWM counter bit selection flag (0: 8 bits, 1: 9 bits)
PWMCK	FLG	0.0A6H.0	R/W	PWM timer output clock selection flag
PWM2SEL	FLG	0.0A7H.2	R/W	PWM2/general-purpose port pin function selection flag
PWM1SEL	FLG	0.0A7H.1	R/W	PWM1/general-purpose port pin function selection flag
PWM0SEL	FLG	0.0A7H.0	R/W	PWM0/general-purpose port pin function selection flag
TM3SEL	FLG	0.0A8H.3	R/W	PWM/modulo timer 3 selection flag
TM3EN	FLG	0.0A8H.1	R/W	Modulo timer 3 count start flag
TM3RES	FLG	0.0A8H.0	R/W	Modulo timer 3 reset flag (when read: 0)
TM2EN	FLG	0.0A9H.3	R/W	Modulo timer 2 count start flag
TM2RES	FLG	0.0A9H.2	R/W	Modulo timer 2 reset flag (when read: 0)
TM2CK1	FLG	0.0A9H.1	R/W	Modulo timer 2 clock selection flag
TM2CK0	FLG	0.0A9H.0	R/W	Modulo timer 2 clock selection flag
TM1EN	FLG	0.0AAH.3	R/W	Modulo timer 1 count start flag
TM1RES	FLG	0.0AAH.2	R/W	Modulo timer 1 reset flag (when read: 0)
TM1CK1	FLG	0.0AAH.1	R/W	Modulo timer 1 clock selection flag
TM1CK0	FLG	0.0AAH.0	R/W	Modulo timer 1 clock selection flag
TM0EN	FLG	0.0ABH.3	R/W	Modulo timer 0 count start flag
TM0RES	FLG	0.0ABH.2	R/W	Modulo timer 0 reset flag (when read: 0)
TM0CK1	FLG	0.0ABH.1	R/W	Modulo timer 0 clock selection flag
TM0CK0	FLG	0.0ABH.0	R/W	Modulo timer 0 clock selection flag
TM0OVF	FLG	0.0ACH.3	R	Modulo timer 0 overflow detection flag
TM0GCEG	FLG	0.0ACH.2	R/W	Modulo timer 0 gate close input signal edge selection flag
TM0GOEG	FLG	0.0ACH.1	R/W	Modulo timer 0 gate open input signal edge selection flag
TM0MD	FLG	0.0ACH.0	R/W	Modulo timer 0 modulo counter/gate counter selection flag

Symbol Name	Attribute	Value	R/W	Description
IPSIO1	FLG	0.0ADH.3	R/W	Serial interface 1 interrupt enable flag
IPSIO0	FLG	0.0ADH.2	R/W	Serial interface 0 interrupt enable flag
IPTM3	FLG	0.0ADH.1	R/W	PWM timer interrupt enable flag
IPTM2	FLG	0.0ADH.0	R/W	Modulo timer 2 interrupt enable flag
IPTM1	FLG	0.0AEH.3	R/W	Modulo timer 1 interrupt enable flag
IPTM0	FLG	0.0AEH.2	R/W	Modulo timer 0 interrupt enable flag
IP4	FLG	0.0AEH.1	R/W	INT4 pin interrupt enable flag
IP3	FLG	0.0AEH.0	R/W	INT3 pin interrupt enable flag
IP2	FLG	0.0AFH.3	R/W	INT2 pin interrupt enable flag
IP1	FLG	0.0AFH.2	R/W	INT1 pin interrupt enable flag
IP0	FLG	0.0AFH.1	R/W	INT0 pin interrupt enable flag
IPCE	FLG	0.0AFH.0	R/W	CE pin interrupt enable flag
IRQSIO1	FLG	0.0B4H.0	R/W	Serial interface 1 interrupt request detection flag
IRQSIO0	FLG	0.0B5H.0	R/W	Serial interface 0 interrupt request detection flag
IRQTM3	FLG	0.0B6H.0	R/W	PWM timer interrupt request detection flag
IRQTM2	FLG	0.0B7H.0	R/W	Modulo timer 2 interrupt request detection flag
IRQTM1	FLG	0.0B8H.0	R/W	Modulo timer 1 interrupt request detection flag
IRQTM0	FLG	0.0B9H.0	R/W	Modulo timer 0 interrupt request detection flag
INT4	FLG	0.0BAH.3	R	INT4 pin status detection flag
IRQ4	FLG	0.0BAH.0	R/W	INT4 pin interrupt request detection flag
INT3	FLG	0.0BBH.3	R	INT3 pin status detection flag
IRQ3	FLG	0.0BBH.0	R/W	INT3 pin interrupt request detection flag
INT2	FLG	0.0BCH.3	R	INT2 pin status detection flag
IRQ2	FLG	0.0BCH.0	R/W	INT2 pin interrupt request detection flag
INT1	FLG	0.0BDH.3	R	INT1 pin status detection flag
IRQ1	FLG	0.0BDH.0	R/W	INT1 pin interrupt request detection flag
INT0	FLG	0.0BEH.3	R	INT0 pin status detection flag
IRQ0	FLG	0.0BEH.0	R/W	INT0 pin interrupt request detection flag
CE	FLG	0.0BFH.3	R	CE pin status detection flag
CECNTSTT	FLG	0.0BFH.1	R	CE reset counter status detection flag
IRQCE	FLG	0.0BFH.0	R/W	CE pin interrupt request detection flag
P0DPLD3	FLG	15.66H.3	R/W	P0D3 pin pull-down resistor selection flag
P0DPLD2	FLG	15.66H.2	R/W	P0D2 pin pull-down resistor selection flag
P0DPLD1	FLG	15.66H.1	R/W	P0D1 pin pull-down resistor selection flag
P0DPLD0	FLG	15.66H.0	R/W	P0D0 pin pull-down resistor selection flag

Symbol Name	Attribute	Value	R/W	Description
P3DGIO	FLG	15.67H.3	R/W	P3D input/output selection flag
P3CGIO	FLG	15.67H.2	R/W	P3C input/output selection flag
P3BGIO	FLG	15.67H.1	R/W	P3B input/output selection flag
P3AGIO	FLG	15.67H.0	R/W	P3A input/output selection flag
P2DBIO3	FLG	15.68H.3	R/W	P2D3 input/output selection flag (dummy)
P2DBIO2	FLG	15.68H.2	R/W	P2D2 input/output selection flag
P2DBIO1	FLG	15.68H.1	R/W	P2D1 input/output selection flag
P2DBIO0	FLG	15.68H.0	R/W	P2D0 input/output selection flag
P2CBIO3	FLG	15.69H.3	R/W	P2C3 input/output selection flag
P2CBIO2	FLG	15.69H.2	R/W	P2C2 input/output selection flag
P2CBIO1	FLG	15.69H.1	R/W	P2C1 input/output selection flag
P2CBIO0	FLG	15.69H.0	R/W	P2C0 input/output selection flag
P2BBIO3	FLG	15.6AH.3	R/W	P2B3 input/output selection flag
P2BBIO2	FLG	15.6AH.2	R/W	P2B2 input/output selection flag
P2BBIO1	FLG	15.6AH.1	R/W	P2B1 input/output selection flag
P2BBIO0	FLG	15.6AH.0	R/W	P2B0 input/output selection flag
P2ABIO3	FLG	15.6BH.3	R/W	P2A3 input/output selection flag (dummy)
P2ABIO2	FLG	15.6BH.2	R/W	P2A2 input/output selection flag
P2ABIO1	FLG	15.6BH.1	R/W	P2A1 input/output selection flag
P2ABIO0	FLG	15.6BH.0	R/W	P2A0 input/output selection flag
P1DBIO3	FLG	15.6CH.3	R/W	P1D3 input/output selection flag
P1DBIO2	FLG	15.6CH.2	R/W	P1D2 input/output selection flag
P1DBIO1	FLG	15.6CH.1	R/W	P1D1 input/output selection flag
P1DBIO0	FLG	15.6CH.0	R/W	P1D0 input/output selection flag
P0CBIO3	FLG	15.6DH.3	R/W	P0C3 input/output selection flag
P0CBIO2	FLG	15.6DH.2	R/W	P0C2 input/output selection flag
P0CBIO1	FLG	15.6DH.1	R/W	P0C1 input/output selection flag
P0CBIO0	FLG	15.6DH.0	R/W	P0C0 input/output selection flag
P0BBIO3	FLG	15.6EH.3	R/W	P0B3 input/output selection flag
P0BBIO2	FLG	15.6EH.2	R/W	P0B2 input/output selection flag
P0BBIO1	FLG	15.6EH.1	R/W	P0B1 input/output selection flag
P0BBIO0	FLG	15.6EH.0	R/W	P0B0 input/output selection flag
P0ABIO3	FLG	15.6FH.3	R/W	P0A3 input/output selection flag
P0ABIO2	FLG	15.6FH.2	R/W	P0A2 input/output selection flag
P0ABIO1	FLG	15.6FH.1	R/W	P0A1 input/output selection flag
P0ABIO0	FLG	15.6FH.0	R/W	P0A0 input/output selection flag

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Symbol Name	Attribute	Value	R/W	Description
SP	MEM	0.81H	R/W	Stack pointer
WDTCK	MEM	0.82H	R/W	Watchdog timer clock selection flag (can be set only once after power application)
WDTCK1	FLG	0.82H.1	R/W	Watchdog timer clock selection flag (can be set only once after power application)
WDTCK0	FLG	0.82H.0	R/W	Watchdog timer clock selection flag (can be set only once after power application)
WDTRES	FLG	0.83H.3	R/W	Watchdog timer counter reset (when read: 0)
DBFSP	MEM	0.84H	R	DBF stack pointer
SPRSEL	MEM	0.85H	R/W	Stack overflow/underflow reset selection flag (can be set only once after power application)
ISPRES	FLG	0.85H.1	R/W	Stack overflow/underflow reset selection flag (can be set only once after power application)
ASPRES	FLG	0.85H.0	R/W	Stack overflow/underflow reset selection flag (can be set only once after power application)
CECNT3	FLG	0.86H.3	R/W	CE reset timer carry counter
CECNT2	FLG	0.86H.2	R/W	CE reset timer carry counter
CECNT1	FLG	0.86H.1	R/W	CE reset timer carry counter
CECNT0	FLG	0.86H.0	R/W	CE reset timer carry counter
MOVTSEL1	FLG	0.87H.1	R/W	MOVT bit selection flag
MOVTSEL0	FLG	0.87H.0	R/W	MOVT bit selection flag
SYSRSP	MEM	0.88H	R	System register stack pointer
SIO2CLC	FLG	0.8AH.3	R	Serial interface 2 clock level control flag
SIO2WREL	FLG	0.8AH.2	R/W	Serial interface 2 wait release control flag
SIO2WAT1	FLG	0.8AH.1	R/W	Serial interface 2 interrupt generation timing/wait control flag
SIO2WAT0	FLG	0.8AH.0	R/W	Serial interface 2 interrupt generation timing/wait control flag
SIO2CLD	FLG	0.8BH.2	R/W	Serial interface 2 clock pin level detection flag
SIO2SIC	FLG	0.8BH.1	R/W	Serial interface 2 interrupt source selection flag
SIO2SVAM	FLG	0.8BH.0	R/W	Serial interface 2 address mask function specification flag
SIO2CMDD	FLG	0.8CH.3	R	Serial interface 2 command signal detection flag
SIO2RELD	FLG	0.8CH.2	R	Serial interface 2 bus release signal detection flag
SIO2CMDT	FLG	0.8CH.1	R/W	Serial interface 2 command signal trigger output control flag
SIO2RELT	FLG	0.8CH.0	R/W	Serial interface 2 bus release signal trigger output control flag
SIO2BSYE	FLG	0.8DH.3	R/W	Serial interface 2 synchronous busy signal enable flag
SIO2ACKD	FLG	0.8DH.2	R	Serial interface 2 acknowledge detection flag
SIO2ACKE	FLG	0.8DH.1	R/W	Serial interface 2 acknowledge enable flag
SIO2ACKT	FLG	0.8DH.0	R/W	Serial interface 2 acknowledge signal trigger output control flag
SIO2WUP	FLG	0.8EH.3	R/W	Serial interface 2 wake-up function specification flag
SIO2MD2	FLG	0.8EH.2	R/W	Serial interface 2 operation mode selection flag
SIO2MD1	FLG	0.8EH.1	R/W	Serial interface 2 operation mode selection flag
SIO2MD0	FLG	0.8EH.0	R/W	Serial interface 2 clock direction selection flag

Symbol Name	Attribute	Value	R/W	Description
SIO2CSIE	FLG	0.8FH.3	R/W	Serial interface 2 operation enable/disable flag
SIO2COI	FLG	0.8FH.2	R	Detection flag for match signal from serial interface 2 address comparator
SIO2TCL1	FLG	0.8FH.1	R/W	Serial interface 2 clock selection flag
SIO2TCL0	FLG	0.8FH.0	R/W	Serial interface 2 clock selection flag
PLLSCNF	FLG	0.90H.3	R/W	Swallow counter least significant bit setting flag
PLLMD1	FLG	0.90H.1	R/W	PLL mode selection flag
PLLMD0	FLG	0.90H.0	R/W	PLL mode selection flag
PLLRFCK3	FLG	0.91H.3	R/W	PLL reference frequency selection flag
PLLRFCK2	FLG	0.91H.2	R/W	PLL reference frequency selection flag
PLLRFCK1	FLG	0.91H.1	R/W	PLL reference frequency selection flag
PLLRFCK0	FLG	0.91H.0	R/W	PLL reference frequency selection flag
PLLUL	FLG	0.92H.0	R&Reset	PLL unlock FF flag
BEEP1SEL	FLG	0.93H.1	R/W	BEEP1/general-purpose port pin function selection flag
BEEP0SEL	FLG	0.93H.0	R/W	BEEP0/general-purpose port pin function selection flag
BEEP1CK1	FLG	0.94H.3	R/W	BEEP1 clock selection flag
BEEP1CK0	FLG	0.94H.2	R/W	BEEP1 clock selection flag
BEEP0CK1	FLG	0.94H.1	R/W	BEEP0 clock selection flag
BEEP0CK0	FLG	0.94H.0	R/W	BEEP0 clock selection flag
WDTCY	FLG	0.96H.0	R	Watchdog timer/stack pointer reset status detection flag
BTM0CY	FLG	0.97H.0	R	Basic timer 0 carry flag
BTM0CK1	FLG	0.98H.1	R/W	Basic timer 0 clock selection flag
BTM0CK0	FLG	0.98H.0	R/W	Basic timer 0 clock selection flag
SIO3CSIE	FLG	0.9AH.3	R/W	Serial interface 3 operation enable/disable flag
SIO3HIZ	FLG	0.9AH.2	R/W	Serial interface 3 SO3 pin status setting flag
SIO3TCL1	FLG	0/9AH.1	R/W	Serial interface 3 clock selection flag
SIO3TCL0	FLG	0.9AH.0	R/W	Serial interface 3 clock selection flag
SIO3PE	FLG	0.9BH.2	R	Serial interface 3 parity error flag
SIO3FE	FLG	0.9BH.1	R	Serial interface 3 framing error flag
SIO3OVE	FLG	0.9BH.0	R	Serial interface 3 overrun error flag
SIO3PS1	FLG	0.9CH.3	R/W	UART parity bit specification flag
SIO3PS0	FLG	0.9CH.2	R/W	UART parity bit specification flag
SIO3CL	FLG	0.9CH.1	R/W	UART character length specification flag
SIO3SL	FLG	0.9CH.0	R/W	Specification flag for stop bit number of UART transmission data
SIO3TXE	FLG	0.9DH.3	R/W	UART transmission mode enable flag
SIO3RXE	FLG	0.9DH.2	R/W	UART reception mode enable flag
SIO3ISRM	FLG	0.9DH.1	R/W	Reception completion interrupt enable flag when error occurs
IEG4	FLG	0.9EH.3	R/W	Edge direction selection flag for INT4 pin interrupt request detection
INT4SEL	FLG	0.9EH.2	R/W	INT4 pin interrupt request flag setting disable
IEG3	FLG	0.9EH.1	R/W	Edge direction selection flag for INT3 pin interrupt request detection
INT3SEL	FLG	0.9EH.0	R/W	INT3 pin interrupt request flag setting disable

Symbol Name	Attribute	Value	R/W	Description
IEG2	FLG	0.9FH.2	R/W	Edge direction selection flag for INT2 pin interrupt request detection
IEG1	FLG	0.9FH.1	R/W	Edge direction selection flag for INT1 pin interrupt request detection
IEG0	FLG	0.9FH.0	R/W	Edge direction selection flag for INT0 pin interrupt request detection
FCGCH1	FLG	0.0A0H.1	R/W	FCG channel selection flag
FCGCH0	FLG	0.0A0H.0	R/W	FCG channel selection flag
IFCGOSTT	FLG	0.0A1H.0	R	IF counter gate status detection flag (1: Open, 0: Closed)
IFCMD1	FLG	0.0A2H.3	R/W	IF counter mode selection flag (10: AMIF, 11: FCG)
IFCMD0	FLG	0.0A2H.2	R/W	IF counter mode selection flag (00: CGP, 11: FMIF)
IFCCK1	FLG	0.0A2H.1	R/W	IF counter clock selection flag
IFCCK0	FLG	0.0A2H.0	R/W	IF counter clock selection flag
IFCSTRT	FLG	0.0A3H.1	W	IF counter count start flag
IFCRES	FLG	0.0A3H.0	W	IF counter reset flag
ADCCH3	FLG	0.0A4H.3	R/W	A/D converter channel selection flag (dummy)
ADCCH2	FLG	0.0A4H.2	R/W	A/D converter channel selection flag
ADCCH1	FLG	0.0A4H.1	R/W	A/D converter channel selection flag
ADCCH0	FLG	0.0A4H.0	R/W	A/D converter channel selection flag
ADCMD	FLG	0.0A5H.2	R/W	A/D converter compare mode selection flag
ADCSTT	FLG	0.0A5H.1	R	A/D converter operation status detection flag (0: End of conversion, 1: Conversion in progress)
ADCCMP	FLG	0.0A5H.0	R	A/D converter compare result detection flag
PWMBIT	FLG	0.0A6H.2	R/W	PWM counter bit selection flag (0: 8 bits, 1: 9 bits)
PWMCK	FLG	0.0A6H.0	R/W	PWM timer output clock selection flag
PWM2SEL	FLG	0.0A7H.2	R/W	PWM2/general-purpose port pin function selection flag
PWM1SEL	FLG	0.0A7H.1	R/W	PWM1/general-purpose port pin function selection flag
PWM0SEL	FLG	0.0A7H.0	R/W	PWM0/general-purpose port pin function selection flag
TM3SEL	FLG	0.0A8H.3	R/W	PWM/modulo timer 3 selection flag
TM3EN	FLG	0.0A8H.1	R/W	Modulo timer 3 count start flag
TM3RES	FLG	0.0A8H.0	R/W	Modulo timer 3 reset flag (when read: 0)
TM2EN	FLG	0.0A9H.3	R/W	Modulo timer 2 count start flag
TM2RES	FLG	0.0A9H.2	R/W	Modulo timer 2 reset flag (when read: 0)
TM2CK1	FLG	0.0A9H.1	R/W	Modulo timer 2 clock selection flag
TM2CK0	FLG	0.0A9H.0	R/W	Modulo timer 2 clock selection flag
TM1EN	FLG	0.0AAH.3	R/W	Modulo timer 1 count start flag
TM1RES	FLG	0.0AAH.2	R/W	Modulo timer 1 reset flag (when read: 0)
TM1CK1	FLG	0.0AAH.1	R/W	Modulo timer 1 clock selection flag
TM1CK0	FLG	0.0AAH.0	R/W	Modulo timer 1 clock selection flag
TM0EN	FLG	0.0ABH.3	R/W	Modulo timer 0 count start flag
TM0RES	FLG	0.0ABH.2	R/W	Modulo timer 0 reset flag (when read: 0)
TM0CK1	FLG	0.0ABH.1	R/W	Modulo timer 0 clock selection flag
TM0CK0	FLG	0.0ABH.0	R/W	Modulo timer 0 clock selection flag

Symbol Name	Attribute	Value	R/W	Description
TM0OVF	FLG	0.0ACH.3	R	Modulo timer 0 overflow detection flag
TM0GCEG	FLG	0.0ACH.2	R/W	Modulo timer 0 gate close input signal edge selection flag
TM0GOEG	FLG	0.0ACH.1	R/W	Modulo timer 0 gate open input signal edge selection flag
TM0MD	FLG	0.0ACH.0	R/W	Modulo timer 0 modulo counter/gate counter selection flag
IPSIO3	FLG	0.0ADH.3	R/W	Serial interface 3 interrupt enable flag
IPSIO2	FLG	0.0ADH.2	R/W	Serial interface 2 interrupt enable flag
IPTM3	FLG	0.0ADH.1	R/W	PWM timer interrupt enable flag
IPTM2	FLG	0.0ADH.0	R/W	Modulo timer 2 interrupt enable flag
IPTM1	FLG	0.0AEH.3	R/W	Modulo timer 1 interrupt enable flag
IPTM0	FLG	0.0AEH.2	R/W	Modulo timer 0 interrupt enable flag
IP4	FLG	0.0AEH.1	R/W	INT4 pin interrupt enable flag
IP3	FLG	0.0AEH.0	R/W	INT3 pin interrupt enable flag
IP2	FLG	0.0AFH.3	R/W	INT2 pin interrupt enable flag
IP1	FLG	0.0AFH.2	R/W	INT1 pin interrupt enable flag
IP0	FLG	0.0AFH.1	R/W	INT0 pin interrupt enable flag
IPCE	FLG	0.0AFH.0	R/W	CE pin interrupt enable flag
IRQSIO3	FLG	0.0B4H.0	R/W	Serial interface 3 interrupt request detection flag
IRQSIO2	FLG	0.0B5H.0	R/W	Serial interface 2 interrupt request detection flag
IRQTM3	FLG	0.0B6H.0	R/W	PWM timer interrupt request detection flag
IRQTM2	FLG	0.0B7H.0	R/W	Modulo timer 2 interrupt request detection flag
IRQTM1	FLG	0.0B8H.0	R/W	Modulo timer 1 interrupt request detection flag
IRQTM0	FLG	0.0B9H.0	R/W	Modulo timer 0 interrupt request detection flag
INT4	FLG	0.0BAH.3	R	INT4 pin status detection flag
IRQ4	FLG	0.0BAH.0	R/W	INT4 pin interrupt request detection flag
INT3	FLG	0.0BBH.3	R	INT3 pin status detection flag
IRQ3	FLG	0.0BBH.0	R/W	INT3 pin interrupt request detection flag
INT2	FLG	0.0BCH.3	R	INT2 pin status detection flag
IRQ2	FLG	0.0BCH.0	R/W	INT2 pin interrupt request detection flag
INT1	FLG	0.0BDH.3	R	INT1 pin status detection flag
IRQ1	FLG	0.0BDH.0	R/W	INT1 pin interrupt request detection flag
INT0	FLG	0.0BEH.3	R	INT0 pin status detection flag
IRQ0	FLG	0.0BEH.0	R/W	INT0 pin interrupt request detection flag
CE	FLG	0.0BFH.3	R	CE pin status detection flag
CECNTSTT	FLG	0.0BFH.1	R	CE reset counter status detection flag
IRQCE	FLG	0.0BFH.0	R/W	CE pin interrupt request detection flag
P0DPLD3	FLG	15.66H.3	R/W	P0D3 pin pull-down resistor selection flag
P0DPLD2	FLG	15.66H.2	R/W	P0D2 pin pull-down resistor selection flag
P0DPLD1	FLG	15.66H.1	R/W	P0D1 pin pull-down resistor selection flag
P0DPLD0	FLG	15.66H.0	R/W	P0D0 pin pull-down resistor selection flag

Symbol Name	Attribute	Value	R/W	Description
P3DGIO	FLG	15.67H.3	R/W	P3D input/output selection flag
P3CGIO	FLG	15.67H.2	R/W	P3C input/output selection flag
P3BGIO	FLG	15.67H.1	R/W	P3B input/output selection flag
P3AGIO	FLG	15.67H.0	R/W	P3A input/output selection flag
P2DBIO3	FLG	15.68H.3	R/W	P2D3 input/output selection flag (dummy)
P2DBIO2	FLG	15.68H.2	R/W	P2D2 input/output selection flag
P2DBIO1	FLG	15.68H.1	R/W	P2D1 input/output selection flag
P2DBIO0	FLG	15.68H.0	R/W	P2D0 input/output selection flag
P2CBIO3	FLG	15.69H.3	R/W	P2C3 input/output selection flag
P2CBIO2	FLG	15.69H.2	R/W	P2C2 input/output selection flag
P2CBIO1	FLG	15.69H.1	R/W	P2C1 input/output selection flag
P2CBIO0	FLG	15.69H.0	R/W	P2C0 input/output selection flag
P2BBIO3	FLG	15.6AH.3	R/W	P2B3 input/output selection flag
P2BBIO2	FLG	15.6AH.2	R/W	P2B2 input/output selection flag
P2BBIO1	FLG	15.6AH.1	R/W	P2B1 input/output selection flag
P2BBIO0	FLG	15.6AH.0	R/W	P2B0 input/output selection flag
P2ABIO3	FLG	15.6BH.3	R/W	P2A3 input/output selection flag (dummy)
P2ABIO2	FLG	15.6BH.2	R/W	P2A2 input/output selection flag
P2ABIO1	FLG	15.6BH.1	R/W	P2A1 input/output selection flag
P2ABIO0	FLG	15.6BH.0	R/W	P2A0 input/output selection flag
P1DBIO3	FLG	15.6CH.3	R/W	P1D3 input/output selection flag
P1DBIO2	FLG	15.6CH.2	R/W	P1D2 input/output selection flag
P1DBIO1	FLG	15.6CH.1	R/W	P1D1 input/output selection flag
P1DBIO0	FLG	15.6CH.0	R/W	P1D0 input/output selection flag
P0CBIO3	FLG	15.6DH.3	R/W	P0C3 input/output selection flag
P0CBIO2	FLG	15.6DH.2	R/W	P0C2 input/output selection flag
P0CBIO1	FLG	15.6DH.1	R/W	P0C1 input/output selection flag
P0CBIO0	FLG	15.6DH.0	R/W	P0C0 input/output selection flag
P0BBIO3	FLG	15.6EH.3	R/W	P0B3 input/output selection flag
P0BBIO2	FLG	15.6EH.2	R/W	P0B2 input/output selection flag
P0BBIO1	FLG	15.6EH.1	R/W	P0B1 input/output selection flag
P0BBIO0	FLG	15.6EH.0	R/W	P0B0 input/output selection flag
P0ABIO3	FLG	15.6FH.3	R/W	P0A3 input/output selection flag
P0ABIO2	FLG	15.6FH.2	R/W	P0A2 input/output selection flag
P0ABIO1	FLG	15.6FH.1	R/W	P0A1 input/output selection flag
P0ABIO0	FLG	15.6FH.0	R/W	P0A0 input/output selection flag

3.5 Peripheral Hardware Register

(1) μPD17704, 17705, 17707, 17708 and 17709

Symbol Name	Attribute	Value	R/W	Description
ADCR	DAT	02H	R/W	A/D converter reference voltage set register
SIO0SFR	DAT	03H	R/W	Serial interface 0 presettable shift register
SIO1SFR	DAT	04H	R/W	Serial interface 1 presettable shift register
TM0M	DAT	1AH	R/W	Timer modulo 0 register
TM0C	DAT	1BH	R	Timer modulo 0 counter
TM1M	DAT	1CH	R/W	Timer modulo 1 register
TM1C	DAT	1DH	R	Timer modulo 1 counter
TM2M	DAT	1EH	R/W	Timer modulo 2 register
TM2C	DAT	1FH	R	Timer modulo 2 counter
AR	DAT	40H	R/W	Address register
DBFSTK	DAT	41H	R/W	DBF stack register
PLLR	DAT	42H	R/W	PLL data register
IFC	DAT	43H	R	IF counter data register
PWMR0	DAT	44H	R/W	PWM0 data register
PWMR1	DAT	45H	R/W	PWM1 data register
PWMR2	DAT	46H	R/W	PWM2 data register
TM3M	DAT	46H	R/W	Time modulo 3 register

★ (2) μPD17717, 17718 and 17719

Symbol Name	Attribute	Value	R/W	Description
ADCR	DAT	02H	R/W	A/D converter reference voltage set register
SIO2SFR	DAT	03H	R/W	Presettable shift register 2
SIO2SVA	DAT	04H	R/W	Serial interface 2 slave address register
SIO3TXS	DAT	05H	W	Serial interface 3 transmission register
SIO3RXB	DAT	05H	R	Serial interface 3 reception buffer register
TM0M	DAT	1AH	R/W	Timer modulo 0 register
TM0C	DAT	1BH	R	Timer modulo 0 counter
TM1M	DAT	1CH	R/W	Timer modulo 1 register
TM1C	DAT	1DH	R	Timer modulo 1 counter
TM2M	DAT	1EH	R/W	Timer modulo 2 register
TM2C	DAT	1FH	R	Timer modulo 2 counter
AR	DAT	40H	R/W	Address register
DBFSTK	DAT	41H	R/W	DBF stack register
PLLR	DAT	42H	R/W	PLL data register
IFC	DAT	43H	R	IF counter data register
PWMR0	DAT	44H	R/W	PWM0 data register
PWMR1	DAT	45H	R/W	PWM1 data register
PWMR2	DAT	46H	R/W	PWM2 data register
TM3M	DAT	46H	R/W	Timer modulo 3 register

3.6 Others

Symbol Name	Attribute	Value	Description
DBF	DAT	0FH	Operand (DBF) for GET/PUT/MOVT/MOVTH/MOVTL instruction
IX	DAT	01H	Operand (IX) for INC instruction
AR_EPA1	DAT	8040H	Operand (EPA bit ON) for CALL/BR/MOVT/MOVTH/MOVTL instruction
AR_EPA0	DAT	4040H	Operand (EPA bit OFF) for CALL/BR/MOVT/MOVTH/MOVTL instruction

3.7 List of Reserved Words (in Alphabetical Order)

3.7.1 Instructions and pseudo-instructions

ADD	ELSE	NIBBLE2	RORC
ADDC	END	NIBBLE2V	SBMAC
AND	ENDCASE	NIBBLE3	SET
BANK0	ENDIF	NIBBLE3V	SET1
BANK1	ENDIFC	NIBBLE4	SET2
BANK2	ENDIFNC	NIBBLE4V	SET3
BANK3	ENDM	NIBBLE5	SET4
BANK4	ENDP	NIBBLE5V	SFCOND
BANK5	ENDR	NIBBLE6	SKE
BANK6	EOF	NIBBLE6V	SKF
BANK7	EXIT	NIBBLE7	SKF1
BANK8	EXITR	NIBBLE7V	SKF2
BANK9	EXTRN	NIBBLE8	SKF3
BANK10	FLG	NIBBLE8V	SKF4
BANK11	GET	NOBMAC	SKGE
BANK12	GLOBAL	NOLIST	SKLT
BANK13	HALT	NOMAC	SKNE
BANK14	IF	NOP	SKT
BANK15	IFCHAR	NOT1	SKT1
BELOW	IFNCHAR	NOT2	SKT2
BR	INC	NOT3	SKT3
BRX	INCLUDE	NOT4	SKT4
C14344	INITFLG	OBMAC	SMAC
C4444	INITFLGX	OMAC	ST
CALL	IRP	OR	STOP
CALLX	LAB	ORG	SUB
CASE	LBMAC	OTHER	SUBC
CLR1	LD	PEEK	SUMMARY
CLR2	LFCOND	POKE	SYSCAL[Note]
CLR3	LIST	POP	SYSCALX[Note]
CLR4	LITERAL	PUBLIC	TAG
CSEG	LMAC	PURGE	TITLE
DAT	MACRO	PUSH	XOR
DB	MEM	PUT	ZZZERROR
DI	MOV	REPT	ZZZMCHK
DW	MOVT	RET	ZZZMSG
EI	NIBBLE	RETI	
EJECT	NIBBLE1	RETSK	

★ **Note** SYSCAL and SYSCALX cannot be used because there is no segment 1 area in the μPD17704.

3.7.2 Registers and flags

(1) μPD17704, 17705, 17707, 17708 and 17709

ADCCH0	DBF3	IRQ2	P0C2
ADCCH1	DBFSP	IRQ3	P0C3
ADCCH2	DBFSTK	IRQ4	P0CBIO0
ADCCH3	FCGCH0	IRQCE	P0CBIO1
ADCCMP	FCGCH1	IRQSIO0	P0CBIO2
ADCMD	IEG0	IRQSIO1	P0CBIO3
ADCR	IEG1	IRQTM0	P0D0
ADCSTT	IEG2	IRQTM1	P0D1
AR	IEG3	IRQTM2	P0D2
AR0	IEG4	IRQTM3	P0D3
AR1	IFC	ISPRES	P0DPLD0
AR2	IFCCK0	IX	P0DPLD1
AR3	IFCCK1	IXE	P0DPLD2
AR_EPA0	IFCGOSTT	IXH	P0DPLD3
AR_EPA1	IFCMD0	IXL	P1A0
ASPRES	IFCMD1	IXM	P1A1
BANK	IFCRES	MOVTSEL0	P1A2
BCD	IFCSTRT	MOVTSEL1	P1A3
BEEP0CK0	INT0	MPE	P1B0
BEEP0CK1	INT1	MPH	P1B1
BEEP0SEL	INT2	MPL	P1B2
BEEP1CK0	INT3	P0A0	P1B3
BEEP1CK1	INT3SEL	P0A1	P1C0
BEEP1SEL	INT4	P0A2	P1C1
BTM0CK0	INT4SEL	P0A3	P1C2
BTM0CK1	IP0	P0ABIO0	P1C3
BTM0CY	IP1	P0ABIO1	P1D0
CE	IP2	P0ABIO2	P1D1
CECNT0	IP3	P0ABIO3	P1D2
CECNT1	IP4	P0B0	P1D3
CECNT2	IPCE	P0B1	P1DBIO0
CECNT3	IPSIO0	P0B2	P1DBIO1
CECNTSTT	IPSIO1	P0B3	P1DBIO2
CMP	IPTM0	P0BBIO0	P1DBIO3
CY	IPTM1	P0BBIO1	P2A0
DBF	IPTM2	P0BBIO2	P2A1
DBF0	IPTM3	P0BBIO3	P2A2
DBF1	IRQ0	P0C0	P2ABIO0
DBF2	IRQ1	P0C1	P2ABIO1

P2ABIO2
P2ABIO3
P2B0
P2B1
P2B2
P2B3
P2BBIO0
P2BBIO1
P2BBIO2
P2BBIO3
P2C0
P2C1
P2C2
P2C3
P2CBIO0
P2CBIO1
P2CBIO2
P2CBIO3
P2D0
P2D1
P2D2
P2DBIO0
P2DBIO1
P2DBIO2
P2DBIO3
P3A0
P3A1
P3A2
P3A3
P3AGIO
P3B0
P3B1
P3B2
P3B3
P3BGIO
P3C0
P3C1
P3C2
P3C3
P3CGIO
P3D0
P3D1
P3D2
P3D3
P3DGIO
PLLMD0
PLLMD1
PLLR
PLLRFCK0
PLLRFCK1
PLLRFCK2
PLLRFCK3
PLLSCNF
PLLUL
PSW
PWM0SEL
PWM1SEL
PWM2SEL
PWMBIT
PWMCK
PWMR0
PWMR1
PWMR2
RPH
RPL
SB
SBACK
SBBSY
SBMD
SBSTT
SIO0CH
SIO0CK0
SIO0CK1
SIO0IMD0
SIO0IMD1
SIO0IMD2
SIO0IMD3
SIO0MS
SIO0NWT
SIO0SF8
SIO0SF9
SIO0SFR
SIO0TX
SIO0WRQ0
SIO0WRQ1
SIO0WSTT
SIO1CK0
SIO1CK1
SIO1HIZ
SIO1SFR
SIO1TS
SP
SPRSEL
SYSRSP
TM0C
TM0CK0
TM0CK1
TM0EN
TM0GCEG
TM0GOEG
TM0M
TM0MD
TM0OVF
TM0RES
TM1C
TM1CK0
TM1CK1
TM1EN
TM1M
TM1RES
TM2C
TM2CK0
TM2CK1
TM2EN
TM2M
TM2RES
TM3EN
TM3M
TM3RES
TM3SEL
WDTCK
WDTCK0
WDTCK1
WDTCY
WDTRES
WR
Z
ZZZ0
ZZZ1
ZZZ2
ZZZ3
ZZZ4
ZZZ5
ZZZ6
ZZZ7
ZZZ8
ZZZ9
ZZZALBMAC
ZZZALMAC
ZZZARGC
ZZZDEVID
ZZZEPA
ZZZLINE
ZZZLSARG
ZZZPRINT
ZZZSKIP
ZZZSYDOC

(2) μPD17717, 17718, and 17719

ADCCH0	DBF0	IRQ0	P0C1
ADCCH1	DBF1	IRQ1	P0C2
ADCCH2	DBF2	IRQ2	P0C3
ADCCH3	DBF3	IRQ3	P0CBIO0
ADCCMP	DBFSP	IRQ4	P0CBIO1
ADCMD	DBFSTK	IRQCE	P0CBIO2
ADCR	FCGCH0	IRQSIO2	P0CBIO3
ADCSTT	FCGCH1	IRQSIO3	P0D0
AR	IEG0	IRQTM0	P0D1
AR0	IEG1	IRQTM1	P0D2
AR1	IEG2	IRQTM2	P0D3
AR2	IEG3	IRQTM3	P0DPLD0
AR3	IEG4	ISPRES	P0DPLD1
AR_EPA0	IFC	IX	P0DPLD2
AR_EPA1	IFCCK0	IXE	P0DPLD3
ASPRES	IFCCK1	IXH	P1A0
BANK	IFCGOSTT	IXL	P1A1
BCD	IFCMD0	IXM	P1A2
BEEP0CK0	IFCMD1	MOVTSEL0	P1A3
BEEP0CK1	IFCRES	MOVTSEL1	P1B0
BEEP0SEL	IFCSTRT	MPE	P1B1
BEEP1CK0	INT0	MPH	P1B2
BEEP1CK1	INT1	MPL	P1B3
BEEP1SEL	INT2	P0A0	P1C0
BTM0CK0	INT3	P0A1	P1C1
BTM0CK1	INT3SEL	P0A2	P1C2
BTM0CY	INT4	P0A3	P1C3
CE	INT4SEL	P0ABIO0	P1D0
CECNT0	IP0	P0ABIO1	P1D1
CECNT1	IP1	P0ABIO2	P1D2
CECNT2	IP2	P0ABIO3	P1D3
CECNT3	IP3	P0B0	P1DBIO0
CECNTSTT	IP4	P0B1	P1DBIO1
CHECK0	IPCE	P0B2	P1DBIO2
CHECK1	IPSIO2	P0B3	P1DBIO3
CHECK2	IPSIO3	P0BBIO0	P2A0
CHECK3	IPTM0	P0BBIO1	P2A1
CMP	IPTM1	P0BBIO2	P2A2
CY	IPTM2	P0BBIO3	P2ABIO0
DBF	IPTM3	P0C0	P2ABIO1

P2ABIO2
P2ABIO3
P2B0
P2B1
P2B2
P2B3
P2BBIO0
P2BBIO1
P2BBIO2
P2BBIO3
P2C0
P2C1
P2C2
P2C3
P2CBIO0
P2CBIO1
P2CBIO2
P2CBIO3
P2D0
P2D1
P2D2
P2DBIO0
P2DBIO1
P2DBIO2
P2DBIO3
P3A0
P3A1
P3A2
P3A3
P3AGIO
P3B0
P3B1
P3B2
P3B3
P3BGIO
P3C0
P3C1
P3C2
P3C3
P3CGIO
P3D0
P3D1
P3D2
P3D3
P3DGIO
PLLMD0
PLLMD1
PLLR
PLLRFCK0
PLLRFCK1
PLLRFCK2
PLLRFCK3
PLLSCNF
PLLUL
PSW
PWM0SEL
PWM1SEL
PWM2SEL
PWMBIT
PWMCK
PWMR0
PWMR1
PWMR2
RPH
RPL
SIO2ACKD
SIO2ACKE
SIO2ACKT
SIO2BSYE
SIO2CLC
SIO2CLD
SIO2CMDD
SIO2CMDT
SIO2COI
SIO2CSIE
SIO2MD0
SIO2MD1
SIO2MD2
SIO2RELD
SIO2RELT
SIO2SFR
SIO2SIC
SIO2SVA
SIO2SVAM
SIO2TCL0
SIO2TCL1
SIO2WAT0
SIO2WAT1
SIO2WREL
SIO2WUP
SIO3CL
SIO3CSIE
SIO3FE
SIO3HIZ
SIO3ISRM
SIO3OVE
SIO3PE
SIO3PS0
SIO3PS1
SIO3RXB
SIO3RXE
SIO3SL
SIO3TCL0
SIO3TCL1
SIO3TXE
SIO3TXS
SP
SPRSEL
SYSRSP
TM0C
TM0CK0
TM0CK1
TM0EN
TM0GCEG
TM0GOEG
TM0M
TM0MD
TM0OVF
TM0RES
TM1C
TM1CK0
TM1CK1
TM1EN
TM1M
TM1RES
TM2C
TM2CK0
TM2CK1
TM2EN
TM2M
TM2RES
TM3EN
TM3M
TM3RES
TM3SEL
WDTCK
WDTCK0
WDTCK1
WDTCY
WDTRES
WR
Z
ZZZ0
ZZZ1
ZZZ2
ZZZ3
ZZZ4
ZZZ5
ZZZ6
ZZZ7
ZZZ8
ZZZ9
ZZZALBMAC
ZZZALMAC
ZZZARGC
ZZZDEVID
ZZZEPA
ZZZLINE
ZZZLSARG
ZZZPRINT
ZZZSKIP
ZZZSYDOC

[MEMO]

★

CHAPTER 4 LOAD MODULE FILE FORMAT

HEX-format load module files output by the RA17K assembler package have two types of output formats: ICE files and PRO files.

These two types of files must be used according to the target application. Besides having a user program area, they also have an assembly environment data area, an in-circuit emulator operating environment data area, and other areas.

(1) HEX-format load module file format

The data contained in HEX-format load module files output by the assembler is output in the following format.

[Example of HEX-format load module file format]

```
  :  10  0002  00  2B41000BFC80F ··· 3A20  EC
  |  |   |    |                    |       |
<1><2> <3>  <4>                  <5>      <6>

  :  00  0000  01  FF
  |  |   |    |   |
<1><2> <3>  <4> <6>
```

<1> Record mark

This indicates the start of a record.

<2> Code amount (2 digits)

This indicates the amount of code (byte data) stored in a record. This value is expressed as a hexadecimal number, with a maximum value of 10H (16 units). The value for the end record is 00H.

<3> Address (4 digits)

This indicates the start address of the code shown in a record. The value for the end record is 0000H, and has no relation to the address.

<4> Record type (2 digits)

A value of 00H indicates "data record" as the record type and a value of 01H indicates "end record."

<5> Code (up to 32 digits (16 bytes))

Code is output to this field one byte at a time, up to 16 bytes.

<6> Check sum (2 digits)

Each data from fields <2>, <3>, <4>, <5> and <6> is output to this field (with even parity) as byte data with an LSB value of 00H based on byte-unit sums.

(2) ICE files

ICE files are output as HEX-format files exclusive to the in-circuit emulator (IE-17K, IE-17K-ET, or EMU-17K [Note]) output by the RA17K assembler package. Figure 4-1 shows the output format assembled using the device files.

★ **Note** Manufactured by Naito Densei Machida Mfg. Co., Ltd.

Figure 4-1. ICE File Format (1/5)

(a) μPD17704

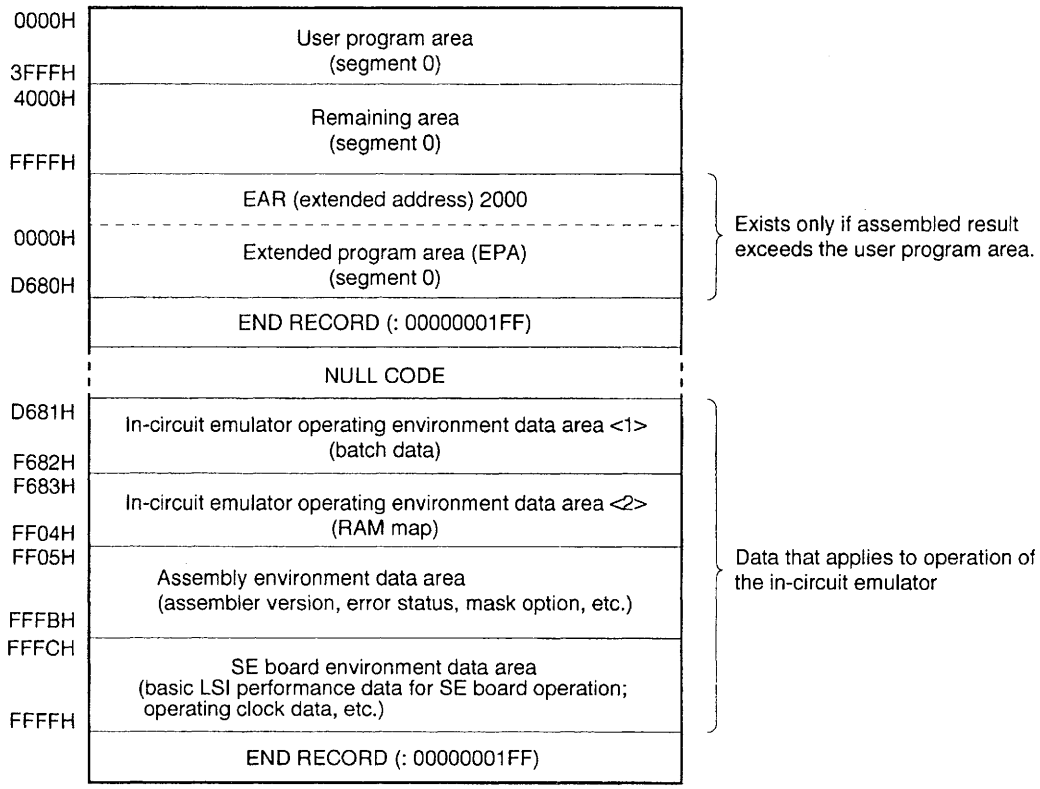


Figure 4-1. ICE File Format (2/5)

(b) μPD17705

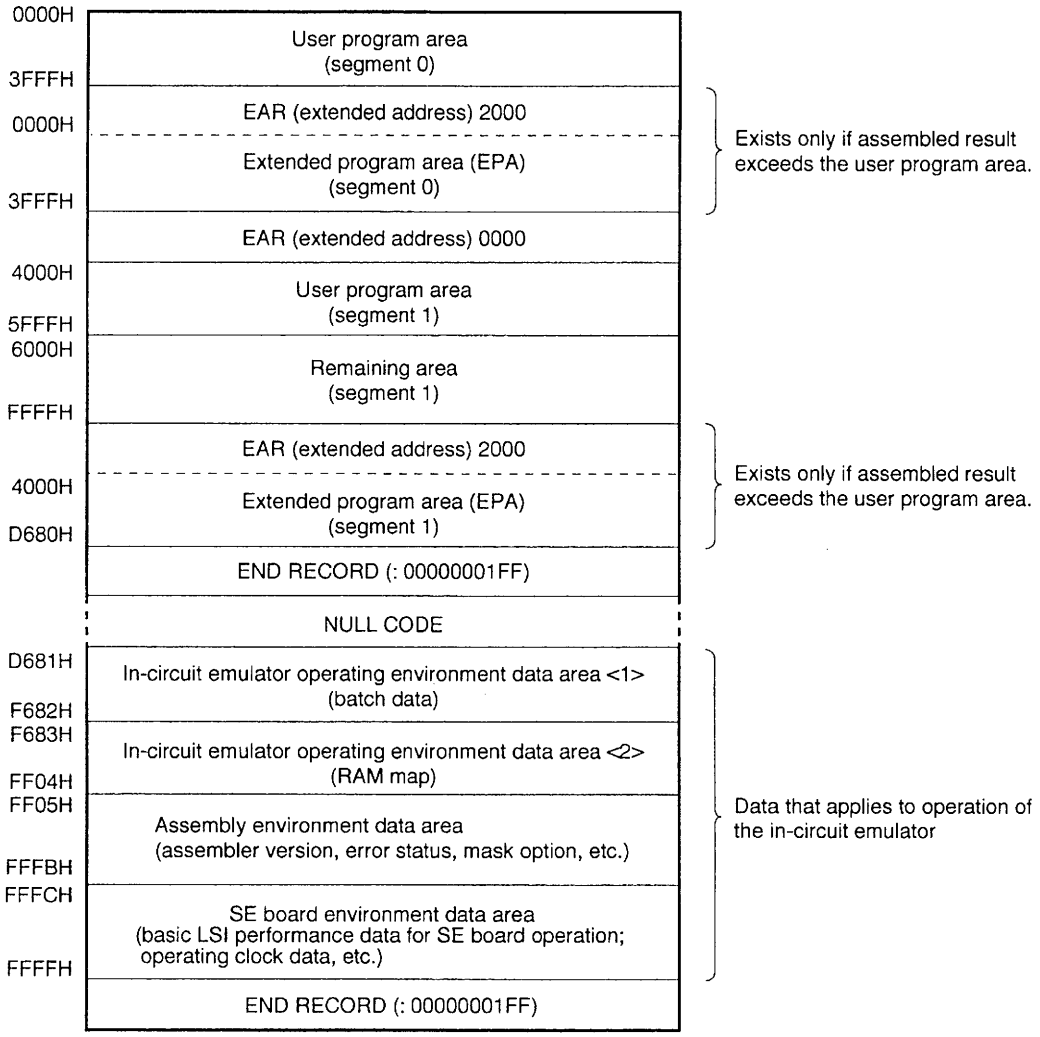


Figure 4-1. ICE File Format (3/5)

(c) μPD17707 and 17717

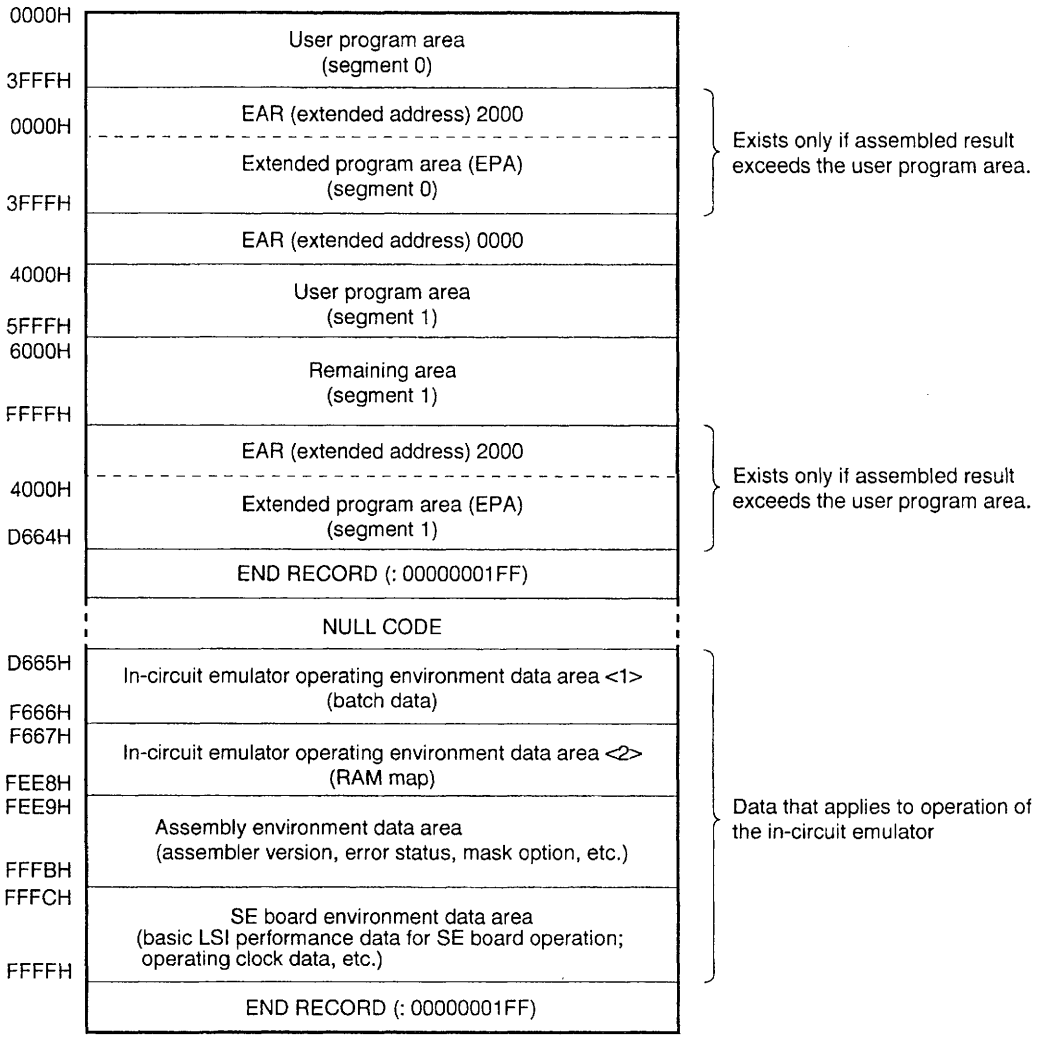


Figure 4-1. ICE File Format (4/5)

(d) μPD17708 and 17718

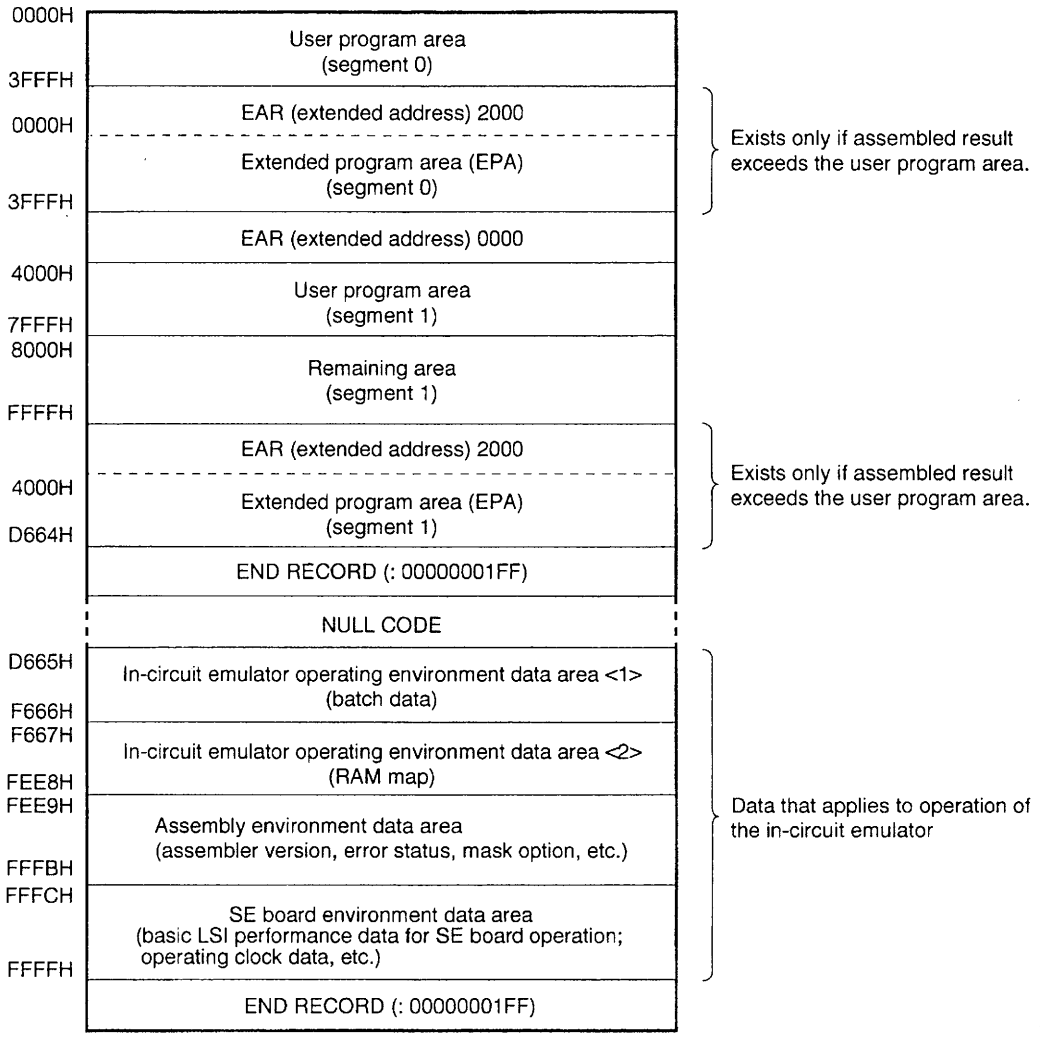
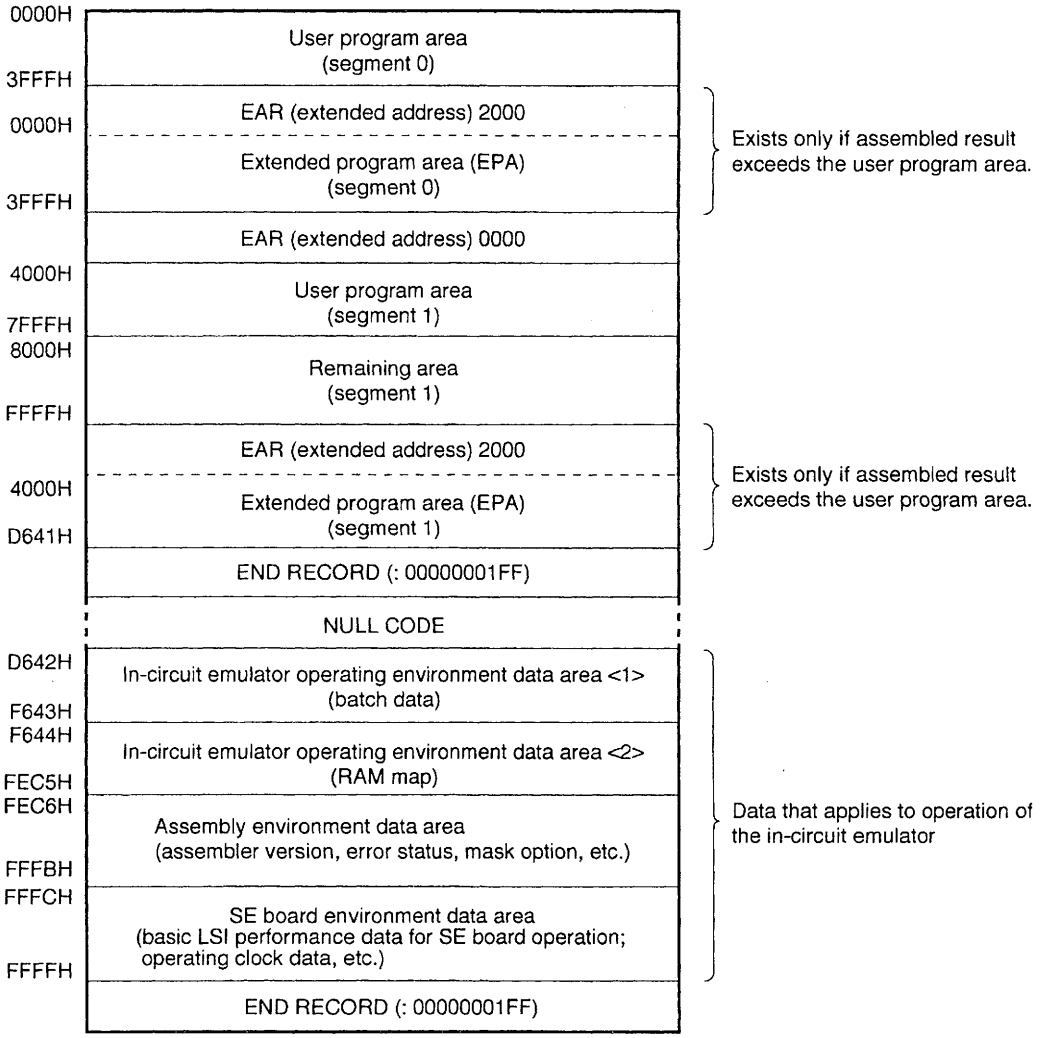


Figure 4-1. ICE File Format (5/5)

(e) μPD17709 and 17719



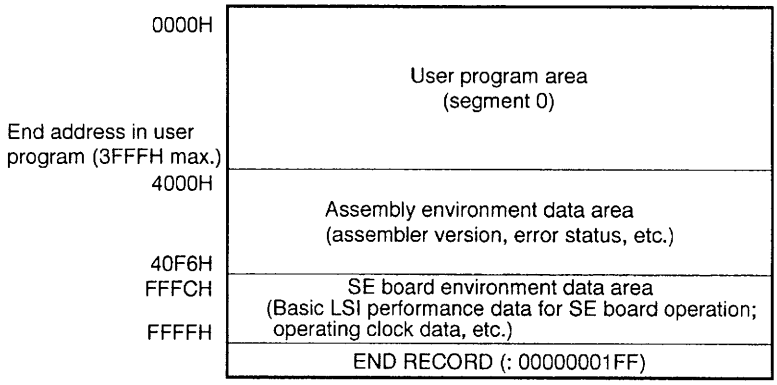
(3) PRO files

PRO files are output as HEX-format files exclusive to the PROM and one-time PROM products that are used for mask order and stand-alone SE board evaluations that are output by the RA17K assembler package. These are output when "/PRO" is specified as an assembly option during assembly.

Figure 4-2 shows the output format assembled using the device files.

Figure 4-2. PRO File Format (1/3)

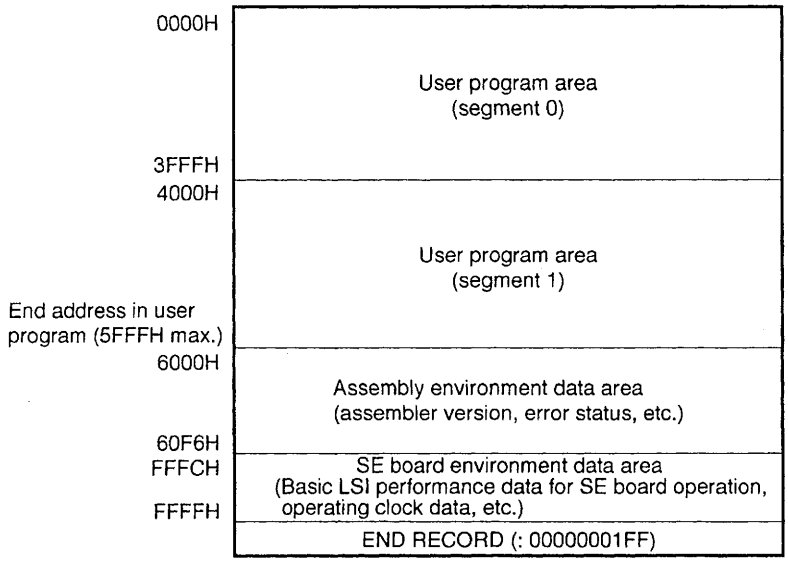
(a) μPD17704



Remark The range of 40F7H to FFFBH does not exist in PRO files.

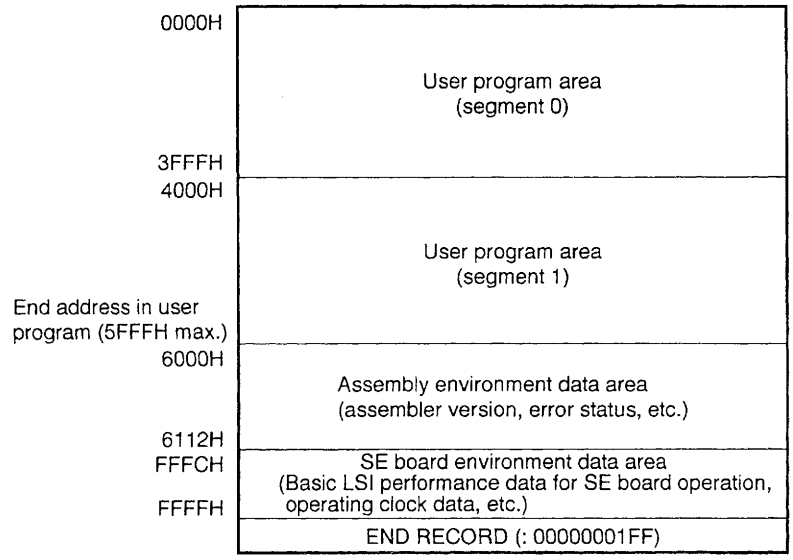
Figure 4-2. PRO File Format (2/3)

(b) μPD17705



Remark The range of 60F7H to FFFBH does not exist in PRO files.

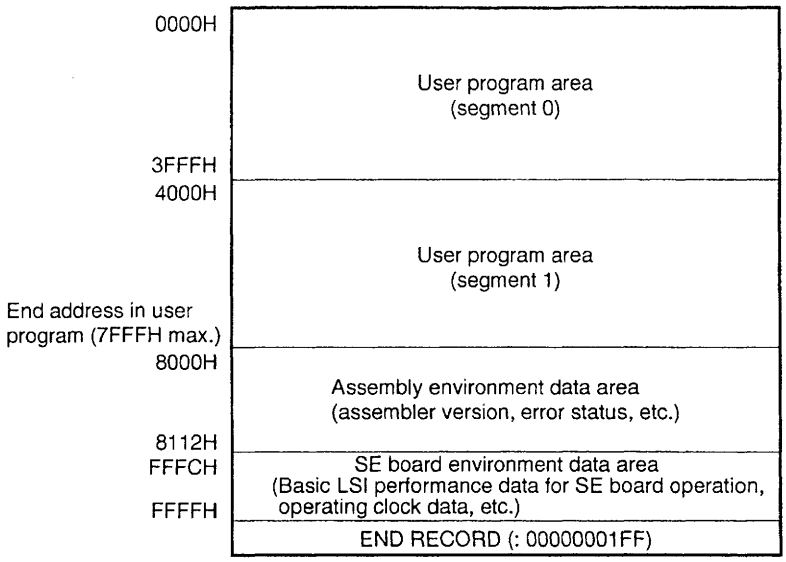
(c) μPD17707 and 17717



Remark The range of 6113H to FFFBH does not exist in PRO files.

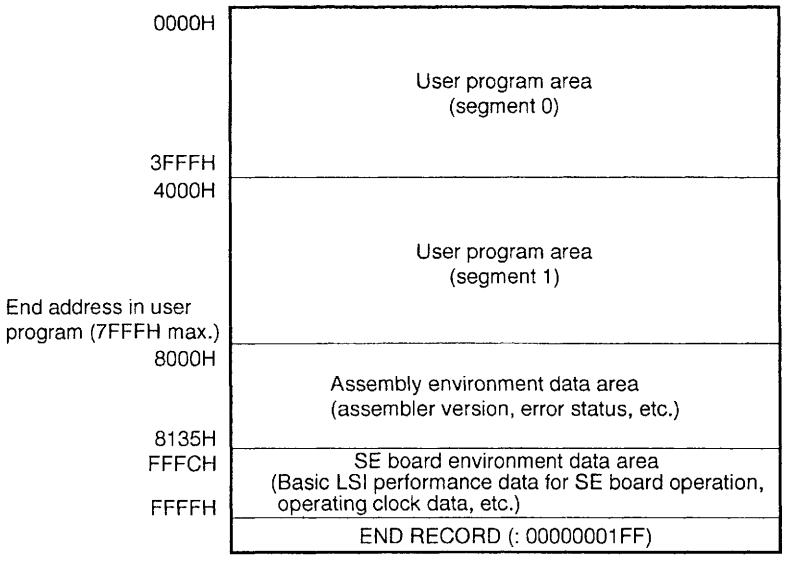
Figure 4-2. PRO File Format (3/3)

(d) μPD17708 and 17718



Remark The range of 8113H to FFFBH does not exist in PRO files.

(e) μPD17709 and 17719



Remark The range of 8136H to FFFBH does not exist in PRO files.

(4) File comparison of load module files

Even when there are no changes in the source file, changes may occur in the assembler output results (i.e., the assembly environment data area). This is because the data in the assembly environment data area includes items such as the source file creation date.

Table 4-1. Items whose Assembler Output Result May Change even when Source File Has No Change (1/5)

(a) μPD17704

Item	Address	
	ICE file	PRO file
Program name (character string of up to 32 bytes, specified by assembly option /' PROG=')	FF05H - FF24H	4000H - 401FH
SIMPLEHOST information	FFADH	40A8H
Error or warning status	FFB0H	40ABH
File creation date and time **Note**	FFBEH - FFC7H	40B9H - 40C2H
Device name	FFC8H - FFD7H	40C3H - 40D2H
Device file version	FFDDH	40D8H
Assembler version	FFE1H	40DCH

Note The creation date/time of the most recent source file or sequence file is written.

Caution Do not make changes to load module files only.
Change load module files by changing the source file and then reassembling. Revising load module files only may cause the histories of the other files to become mismatched, resulting in bugs.

Table 4-1. Items whose Assembler Output Result May Change even when Source File Has No Change (2/5)

(b) μPD17705

Item	Address	
	ICE file	PRO file
Program name (character string of up to 32 bytes, specified by assembly option /' PROG=')	FF05H - FF24H	6000H - 601FH
SIMPLEHOST information	FFADH	60A8H
Error or warning status	FFB0H	60ABH
File creation date and time Note	FFBEH - FFC7H	60B9H - 60C2H
Device name	FFC8H - FFD7H	60C3H - 60D2H
Device file version	FFDDH	60D8H
Assembler version	FFE1H	60DCH

Note The creation date/time of the most recent source file or sequence file is written.

Caution Do not make changes to load module files only.
Change load module files by changing the source file and then reassembling. Revising load module files only may cause the histories of the other files to become mismatched, resulting in bugs.

Table 4-1. Items whose Assembler Output Result May Change even when Source File Has No Change (3/5)

(c) μPD17707 and 17717

Item	Address	
	ICE file	PRO file
Program name (character string of up to 32 bytes, specified by assembly option /' PROG=')	FEE9H - FF08H	6000H - 601FH
SIMPLEHOST information	FFADH	60C4H
Error or warning status	FFB0H	60C7H
File creation date and time Note	FFBEH - FFC7H	60D5H - 60DEH
Device name	FFC8H - FFD7H	60DFH - 60EEH
Device file version	FFDDH	60F4H
Assembler version	FFE1H	60F8H

Note The creation date/time of the most recent source file or sequence file is written.

Caution Do not make changes to load module files only.
Change load module files by changing the source file and then reassembling. Revising load module files only may cause the histories of the other files to become mismatched, resulting in bugs.

Table 4-1. Items whose Assembler Output Result May Change even when Source File Has No Change (4/5)

(d) μPD17708 and 17718

Item	Address	
	ICE file	PRO file
Program name (character string of up to 32 bytes, specified by assembly option /' PROG=')	FEE9H - FF08H	8000H - 801FH
SIMPLEHOST information	FFADH	80C4H
Error or warning status	FFB0H	80C7H
File creation date and time Note	FFBEH - FFC7H	80D5H - 80DEH
Device name	FFC8H - FFD7H	80DFH - 80EEH
Device file version	FFDDH	80F4H
Assembler version	FFE1H	80F8H

Note The creation date/time of the most recent source file or sequence file is written.

Caution Do not make changes to load module files only.
Change load module files by changing the source file and then reassembling. Revising load module files only may cause the histories of the other files to become mismatched, resulting in bugs.

Table 4-1. Items whose Assembler Output Result May Change even when Source File Has No Change (5/5)

(e) μPD17709 and 17719

Item	Address	
	ICE file	PRO file
Program name (character string of up to 32 bytes, specified by assembly option /' PROG=')	FEC6H - FEE5H	8000H - 801FH
SIMPLEHOST information	FFADH	80E7H
Error or warning status	FFB0H	80EAH
File creation date and time Note	FFBEH - FFC7H	80F8H - 8101H
Device name	FFC8H - FFD7H	8102H - 8111H
Device file version	FFDDH	8117H
Assembler version	FFE1H	811BH

Note The creation date/time of the most recent source file or sequence file is written.

Caution Do not make changes to load module files only.
Change load module files by changing the source file and then reassembling. Revising load module files only may cause the histories of the other files to become mismatched, resulting in bugs.

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