



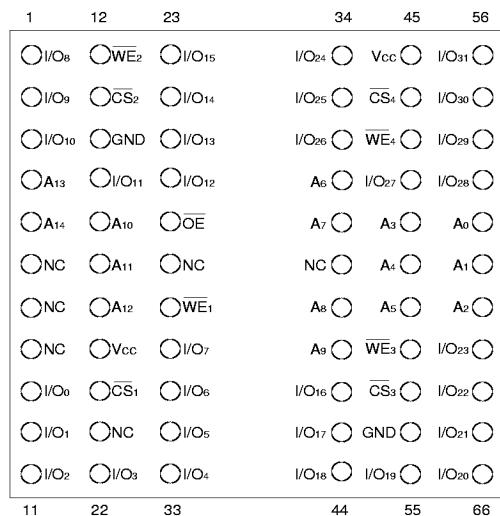
32Kx32 SRAM MODULE

FEATURES

- Access Times of 25, 35, 45, 55, 70, 85, 100, 120nS
- 66 pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400)
- Organized as 32Kx32; User Configurable as 64Kx16 or 128Kx8
- Battery Back-Up Operation
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power CMOS
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation

FIG. 1 PIN CONFIGURATION FOR WS32K32N-XH1X

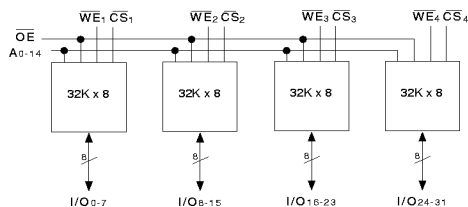
TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-14	Address Inputs
WE1-4	Write Enables
CS1-4	Chip Selects
OE	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C

TRUTH TABLE

CS	OE	WE	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

(T_A = 25°C)

Test	Symbol	Conditions	Max	Unit
OE capacitance	CoE	V _{IN} = 0 V, f = 1.0 MHz	50	pF
WE 1-4 capacitance	CwE	V _{IN} = 0 V, f = 1.0 MHz	20	pF
CS 1-4 capacitance	Ccs	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	CA _D	V _{IN} = 0 V, f = 1.0 MHz	50	pF

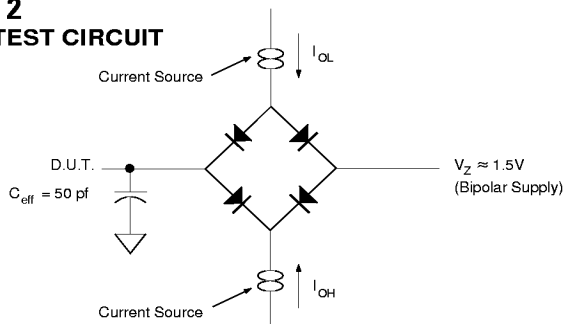
This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	-25		-35		-45		-55		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		15		15		15		15	μA
Output Leakage Current	I _{LO}	CS = V _{IH} , OE = V _{IH} , V _{OUT} = GND to V _{CC}		15		15		15		15	μA
Operating Supply Current x 32 Mode	I _{CC}	CS = V _{IL} , OE = V _{IH} , f = 5MHz		450		450		450		450	mA
Standby Current	I _{SB}	CS = V _{IH} , OE = V _{IH} , f = 5MHz		60		60		55		50	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA, V _{CC} = 4.5		0.4		0.4					V
Output High Voltage	V _{OH}	I _{OH} = 2.1mA, V _{CC} = 4.5						0.4		0.4	V
		I _{OH} = -4.0mA, V _{CC} = 4.5	2.4		2.4						V
Output High Voltage	V _{OH}	I _{OH} = -1.0mA, V _{CC} = 4.5					2.4		2.4		V

Parameter	Symbol	Conditions	-70		-85		-100		-120		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		15		15		15		15	μA
Output Leakage Current	I _{LO}	CS = V _{IH} , OE = V _{IH} , V _{OUT} = GND to V _{CC}		15		15		15		15	μA
Operating Supply Current x 32 Mode	I _{CC}	CS = V _{IL} , OE = V _{IH} , f = 5MHz	450		450		170		170		mA
Standby Current	I _{SB}	CS = V _{IH} , OE = V _{IH} , f = 5MHz	45		4		2.0		2.0		mA
Output Low Voltage	V _{OL}	I _{OL} = 2.1mA, V _{CC} = 4.5		0.4		0.4		0.4		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -1.0mA, V _{CC} = 4.5	2.4		2.4		2.4		2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3VFIG. 2
AC TEST CIRCUIT

AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.I_{OL} & I_{OH} programmable from 0 to 16mA.Tester Impedance Z₀ = 75 Ω.V_Z is typically the midpoint of V_{OH} and V_{OL}.I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.

ATE tester includes jig capacitance.

**DATA RETENTION CHARACTERISTICS**

(TA = -55°C to +125°C)

Parameter	Symbol	Conditions	-25			-35			-45			-55			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V _{DR}	CS ≥ V _{CC} - .2V	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I _{CCR1}	V _{CC} = 3V		.5	8.0		.5	8.0		.5	8.0		.03	3.2	mA
	I _{CCR2}	V _{CC} = 2V		.25	4.0		.25	4.0		.25	4.0		.02	2.1	mA

Parameter	Symbol	Conditions	-70			-85			-100			-120			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V _{DR}	CS ≥ V _{CC} - .2V	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I _{CCR1}	V _{CC} = 3V		30	1200		10	1600		10	750		10	750	μA
	I _{CCR2}	V _{CC} = 2V		20	900		7	1200		7	500		7	500	μA

AC CHARACTERISTICS(V_{CC} = 5.0V, V_{SS} = 0V, TA = -55°C to +125°C)

Parameter Read Cycle	Symbol	-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	25		35		45		55		nS
Address Access Time	t _{AA}		25		35		45		55	nS
Output Hold from Address Change	t _{OH}	5		5		5		5		nS
Chip Select Access	t _{ACS}		25		35		45		55	nS
Output Enable to Output Valid	t _{OE}		15		20		25		30	nS
Chip Select to Output in Low Z	t _{CLZ} ¹	5		5		5		5		nS
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		0		nS
Chip Disable to Output in High Z	t _{CHZ} ¹		12		15		20		25	nS
Output Disable to Output in High Z	t _{OHZ} ¹		12		15		20		25	nS

1. This parameter is guaranteed by design but not tested.

Parameter Read Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	70		85		100		120		nS
Address Access Time	t _{AA}		70		85		100		120	nS
Output Hold from Address Change	t _{OH}	5		5		5		5		nS
Chip Select Access	t _{ACS}		70		85		100		120	nS
Output Enable to Output Valid	t _{OE}		35		40		45		50	nS
Chip Select to Output in Low Z	t _{CLZ} ¹	5		5		5		5		nS
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		0		nS
Chip Disable to Output in High Z	t _{CHZ} ¹		30		35		40		50	nS
Output Disable to Output in High Z	t _{OHZ} ¹		30		35		40		50	nS

1. This parameter is guaranteed by design but not tested.



FIG. 3
TIMING WAVEFORM - READ CYCLE

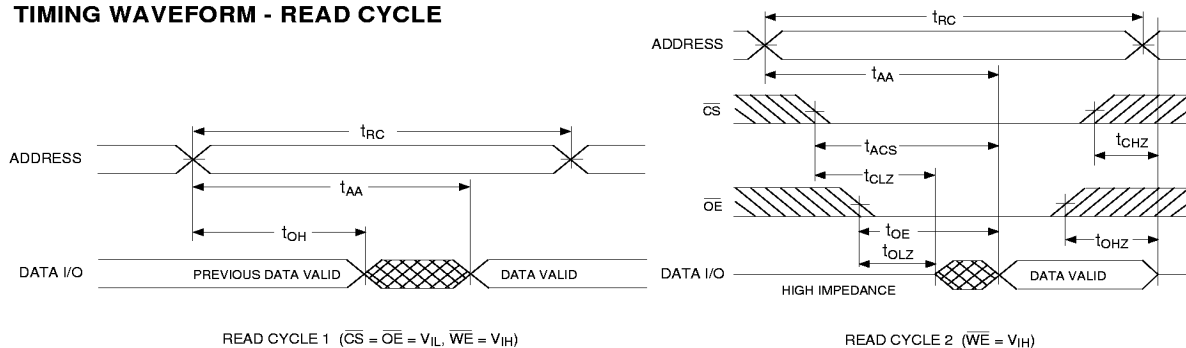


FIG. 4
WRITE CYCLE - $\overline{WE}$ CONTROLLED

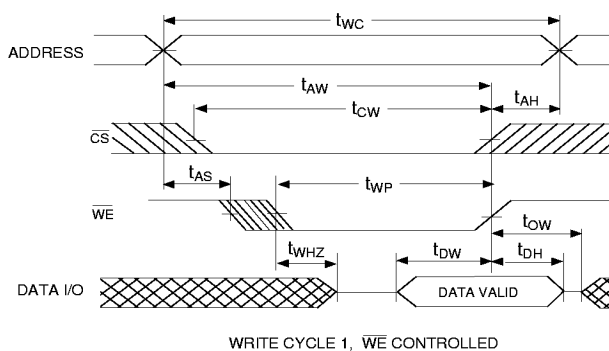
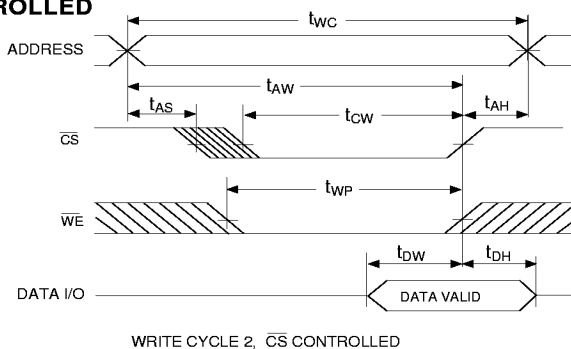


FIG. 5
WRITE CYCLE - $\overline{CS}$ CONTROLLED



**AC CHARACTERISTICS**(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

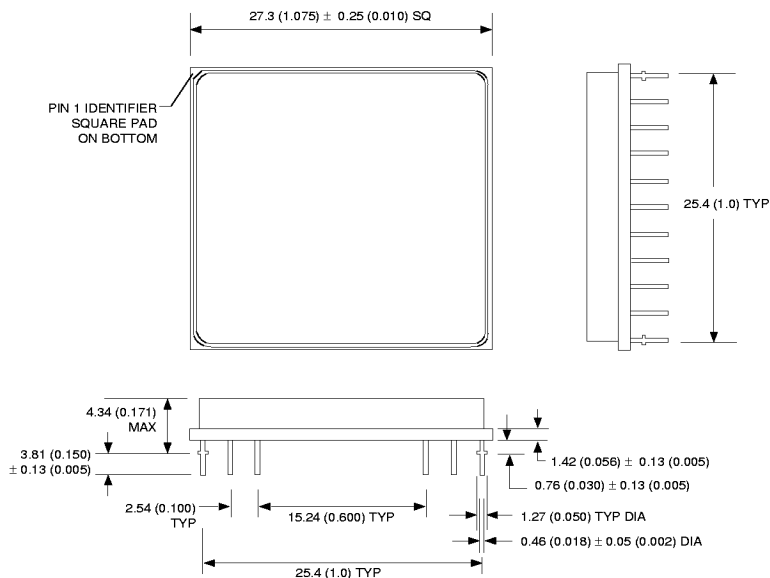
Parameter Write Cycle	Symbol	-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{wc}	25		35		45		55		nS
Chip Select to End of Write	t _{cw}	20		30		40		45		nS
Address Valid to End of Write	t _{aw}	20		30		40		45		nS
Data Valid to End of Write	t _{dw}	15		18		20		25		nS
Write Pulse Width	t _{wp}	20		25		35		40		nS
Address Setup Time	t _{as}	5		5		5		5		nS
Address Hold Time	t _{ah}	0		0		0		0		nS
Output Active from End of Write	t _{ow} ¹	5		5		5		5		nS
Write Enable to Output in High Z	t _{whz} ¹		10		15		15		20	nS
Data Hold Time	t _{dh}	3		3		3		5		nS

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter Write Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{wc}	70		85		100		120		nS
Chip Select to End of Write	t _{cw}	65		80		90		110		nS
Address Valid to End of Write	t _{aw}	65		80		90		110		nS
Data Valid to End of Write	t _{dw}	30		35		40		55		nS
Write Pulse Width	t _{wp}	45		50		55		65		nS
Address Setup Time	t _{as}	5		5		5		5		nS
Address Hold Time	t _{ah}	0		0		0		0		nS
Output Active from End of Write	t _{ow} ¹	5		5		5		5		nS
Write Enable to Output in High Z	t _{whz} ¹		30		35		40		50	nS
Data Hold Time	t _{dh}	5		5		5		5		nS

1. This parameter is guaranteed by design but not tested.

**PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)**

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION**W S 32K 32 N - XXX H1 X****DEVICE GRADE:**

M = Military Screened	-55°C to +125°C
I = Industrial	-40°C to +85°C
C = Commercial	0°C to +70°C

PACKAGE:

H1 = Ceramic Hex-In-Line Package, HIP (Package 400)

ACCESS TIME in nS**IMPROVEMENT MARK:**

N = No Connect at pin 6, 7, 8, 21, 28 and 39

ORGANIZATION, 32Kx32**SRAM****WHITE MICROELECTRONICS**