T-42-41

UCS51
ASIC FAMILY OF ENHANCED 8-BIT MICROCONTROLLERS WITH USER-SELECTABLE PERIPHERAL SET AND ROM/RAM CONFIGURATIONS

UCS51 16 MHz, V_{CC} = 5V ±10%, 0°C–70°C Case
12 MHz, V_{CC} = 5V ±10%, −55°C–+125°C Case

- **SFR Bus-Compatible Peripherals**
  - **A/D Converter**
  - **Bus Interface/Port**
  - **Baud-Rate Generator**
  - **UART**
  - **Timer Counter**
- **Customer-Designed SFR Peripherals**
  - **Extensive Cell Library Available**
- **Core Configurations**
  - **ROM, 0K-32K, 4K Increments**
  - **RAM 128 Bytes and 256 Bytes**
  - **5 and 10 Interrupts**
- **De-Multiplexed Ports**
  - **Ports and Databus can be used concurrently**
- **1.5 Micron CHMOS III**

The UCS51 microcontroller core cell allows customers to gain access to the internal peripheral bus (Special Function Register) SFR bus. This provides peripheral selection which exactly fits the customer's needs. When the supplied peripheral set is insufficient, an optimum peripheral can be designed by the customer.

The SFR bus supports direct addressing of peripherals, which allows for enhanced performance, more efficient code utilization, and increased bit-manipulation capability.

See the "ASIC Embedded Controller Handbook" for detailed information about the UCS51 product family.

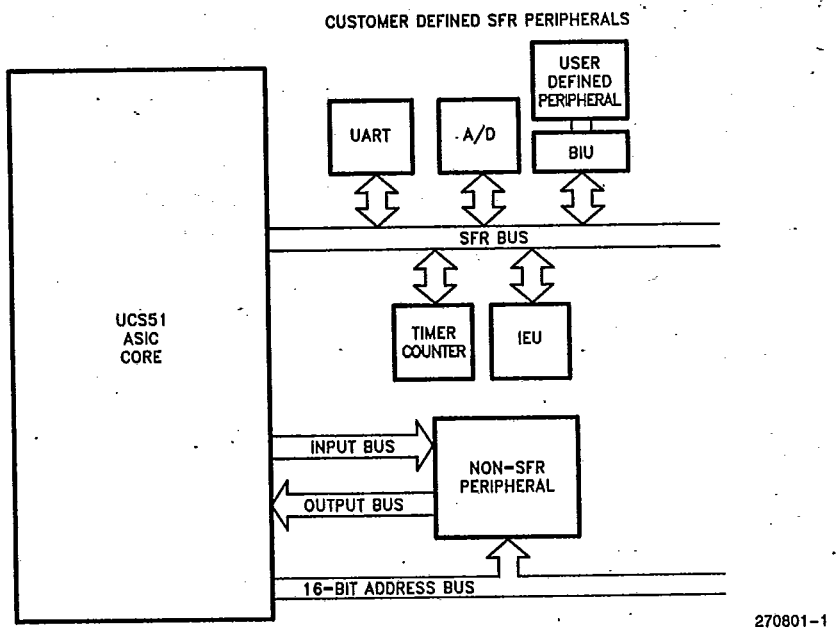

Figure 1. UCS51 Block Diagram

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Zycad is a trademark of Zyvision.

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Table 1

Operation	Case Temperature Range	Voltage Range
Commercial	0°C–70°C	5V ±10%
Industrial	−40°C–85°C	5V ±10%
Military	−55°C–125°C	5V ±10%

PIN DESCRIPTION

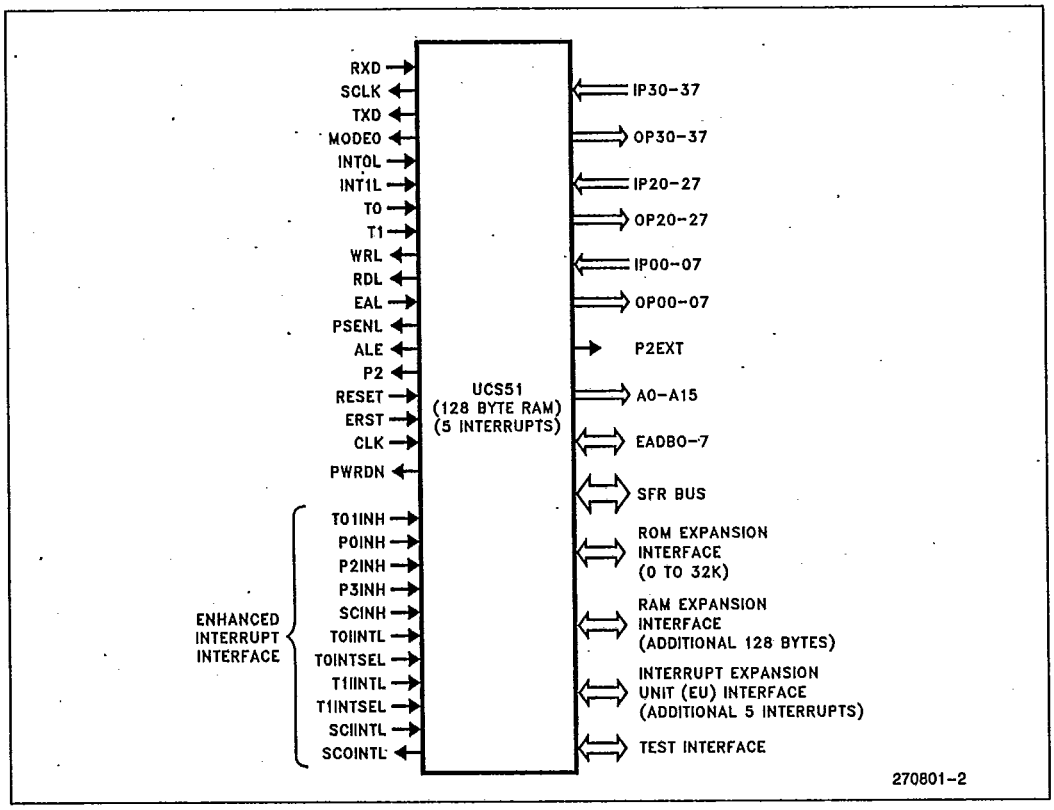

Figure 2. UCS51 Functional Diagram

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CLK: The Input Clock is the clock signal input to the UCS51 core during normal user operation. Connect to the output of either the POSC or PWOSC companion cell when using a crystal oscillator clock source.

TICLK: Tester Input Clock supplies the clock to the UCS51 core during test. MANDATORY PACKAGE PIN.

EAL: EAL is an input pin that specifies the location of program memory: 0 = external, 1 = internal. It is latched on the falling edge of ERST and RESET. For test purposes, EAL must be controllable from a package pin. EAL is not present on ROMless UCS51 cores.

ALE: Address Latch Enable is used for external program memory expansion in conjunction with PSENL. In conjunction with WRL and RDL, ALE is used for external data memory expansion. When ALE is a logic 1, the memory address is available on EADB0–7. The entire latched address is available on A0–A15.

PSENL: Program Strobe Enable is an active-low output that can be used to enable the output drivers of external program memory.

ERST: External Reset is an active-high input that provides an external (off-chip) reset for the entire chip during both normal user operation and testing. Do not use internal user logic to drive this input. MANDATORY PACKAGE PIN.

RESET: Internal Reset is an active-high input that enables on-chip user logic to reset the UCS51 core. Apply a logic 1 for at least 12 oscillator periods to reset the core.

INT0L: External Interrupt 0 is an active-low external interrupt input.

INT1L: External Interrupt 1 is an active-low external interrupt input.

SCIINTL: Serial Port Interrupt In is the active-low serial port interrupt input. This interrupt input may be reassigned to an external interrupt source.

SCOINTL: Serial Port Interrupt Out is an active-low output that indicates a serial port interrupt. A logical OR of the receive interrupt flag and the transmit interrupt flag in the SCON register generates SCOINTL.

T0IINTL: Timer 0 Interrupt In is the active-low Timer 0 interrupt input. This interrupt may be reassigned to an external interrupt source.

T1IINTL: Timer 1 Interrupt In is the active-low Timer 1 interrupt input. This interrupt may be reassigned to an external interrupt source.

EADB0–7: The External Address/Data Bus must be brought off-chip for testing and for off-chip program and data memory accesses. MANDATORY PACKAGE PINS.

A0–A15: A0–A15 is the 16-bit address bus for external program and data memory.

IP00–7: Input Port 0 is the demultiplexed, 8-bit Port 0 input bus (address = 80H).

OP00–7: Output Port 0 is the demultiplexed, 8-bit Port 0 output bus (address = 80H).

IP20–7: Input Port 2 is the demultiplexed, 8-bit Port 2 input bus (address = A0H).

OP20–7: Output Port 2 is the demultiplexed, 8-bit Port 2 output bus (address = A0H). Unlike Port 2 of the 80C51, OP20–7 is not used to output the high order address during fetches to internal program memory (see P2EXT).

IP30–7: Input Port 3 is the demultiplexed, 8-bit Port 3 input bus (address = B0H).

OP30–7: Output Port 3 is the demultiplexed, 8-bit Port 3 output bus (address = BOH).

P2: Phase 2 Clock is a UCS51 core output clock signal with a frequency equal to ½ of CLK/TICLK.

P2EXT: The Port 2/A8–15 Select is an active-high output signal that can be used to reconstruct the 80C51 Port 2 output function. While internal program memory is selected (i.e., EAL is high), P2EXT is active during the execution of a MOVX @DPTR instruction. While external program memory is selected (i.e., EAL is low or the addressing limit of the internal ROM is exceeded), P2EXT is always active except during a MOVX @R*i*.

T0: Timer/Counter 0 is the Timer 0 external input pin.

T1: Timer/Counter 1 is the Timer 1 external input pin.

WRL: The Write Strobe is an active-low strobe output for external data memory.

RDL: The Read Strobe is an active-low strobe output for external data memory.

RXD: RXD is the serial input port during all four serial port modes.

TXD: TXD is the serial output port during all four serial port modes.

SCLK: The Serial Port Shift Clock is equivalent to the Mode 0 TXD output on the the 80C51. SCLK is fixed at one-sixth of the input clock (CLK or TICLK). Output only during Serial Mode 0.

MODE0: Mode 0 Control is an active-high output that is active during Serial Port Mode 0 operation. MODE0 enables the designer to recombine Port 3 with RXD, TXD, and SCLK to create an 80C51-type Serial Mode 0.

PWRDN: Power Down is an active-high output signal that indicates that the core is in power-down mode. PWRDN goes active when bit 1 of the PCON register is set. Internal RAM is preserved during the power-down mode.

CORETEST: Core Test is an active-high output that signifies that the core is in test mode and is driving data onto the EADB bus. When active, all user logic must three-state the EADB bus.

TADBOE: The Test Address/Data Bus Output Enable Control controls the direction of the PADB companion cells that bring the EADB bus off-chip. A low level on TADBOE three-states the PADB cells. When user-logic connects to the EADB bus, combine TADBOE with the user-logic direction-control signal to control the PADB companion cells.

TITEST: The Test Mode Enable input enables the UCS51 core test mode during a reset (ERST or Reset high). TITEST is multiplexed with ALE during test mode. MANDATORY PACKAGE PIN.

TOPP1TO: Test Programmable Pin 1 Output Enable controls the direction of the TPP1 PRGUCS companion cell during test mode. TOPP1TO is low during normal user operation, which configures the TPRGIO pin as an output.

TOPP2TO: Test Programmable Pin 2 Output Enable controls the direction of the TPP2 PRGUCS companion cell during test mode. TOPP2TO is low during normal user operation, which configures TPRG2IO as an output.

TPPC: The Test Programmable Connector Control signal control both PRGUCS companion cells. When the PRGUCS companion cell is configured an output, TPPC is the multiplexer select signal that enables either the TPRGxIO signal or the user output signal (UOS). TPPC is a logic 1 during the test mode, which selects the test programmable pin outputs (TPRGxIO). TPPC remains low during normal user operation, which selects the user-output signals (UOS).

TADBC: The Test Address/Data Bus Control signal controls the PRGPIN companion cell. When the PRGPIN companion cell is configured as an output, TADBC is the multiplexer select signal that enables either the ALE signal or the user-output signal (UOS). TADBC is a logic 1 during test mode, which selects ALE.

During normal user operation TADBC is low, which selects the user-output signal (UOS).

TPRG1IO: Test Programmable Pin 1 Input/Output signal functions as the IO path during test mode. It is used in conjunction with the PRGUCS companion cell. MANDATORY PACKAGE PIN.

TPRG2IO: Test Programmable Pin 2 Input/Output signal functions as the IO path during test mode. It is used in conjunction with the PRGUCS companion cell. MANDATORY PACKAGE PIN.

SPH2: SFR Phase 2 Clock is a UCS51 Phase 2 clock output. It is **not** active during Idle mode.

SPH2S: SFR Phase 2 Sleep Clock is a UCS51 Phase 2 clock output. It remains active during Idle mode.

UCS51 DESCRIPTION

Many UCS Core Cells to Choose From

The UCS51 is a modified cell version of Intel's industry standard 80C51 Microcontroller. When used in conjunction with the Intel 1.5 Micron CHMOS III Cell Library, the UCS51 core enables a designer to implement a semi-custom integrated circuit that includes an 80C51 core, various peripherals that interface to the core, and design-specific support logic. This allows the designer to explore application areas previously reserved for custom design solutions.

The UCS51 core cell is available with 0 to 32 Kbytes of Read Only Memory (ROM) in 4K increments. The use of additional ROM expands the codespace capability of the UCS51 core beyond the 4 Kbytes available with the 80C51 standard product, in most cases alleviating the need for external program memory. The ROMless version of the UCS51 core cell provides an 80C31-compatible core.

In addition to configurable ROM selections, the UCS51 core is available with either 128 or 256 Bytes of Random Access Memory (RAM).

The UCS51 core contains three internal and two external interrupt sources. The addition of the interrupt expansion unit increases the number of external interrupts from two to seven. This allows for core configurations of either 5 or 10 interrupt sources.

80C51 I/O Demultiplexed

In transforming the 80C51 into an ASIC core cell, the standard product's I/O drivers and pin multiplexers were eliminated. As a result, all of the functional pins of the 80C51 are available to the UCS51 user, totaling 105 user-available signals. Intel has ensured compatibility with the cell library while maintaining code and functional compatibility with the standard product, but also allowing code optimization. Designers can take advantage of the UCS51's demultiplexed I/O ports to optimize their application code.

Special Function Register Bus Provides Direct Access to Peripherals

The most powerful feature of the UCS51 cell family is the ability to directly interface to the internal bus of the cores. This bus is called the Special Function Register (SFR) bus. The SFR bus is a synchronous 8-bit, multiplexed address/data bus which allows specially designed external peripheral blocks to be directly connected to the UCS51 core. In this manner, the registers in these peripherals become mapped to addresses in the core's special function register address space. These SFR peripheral registers are accessed by the UCS51 cores in the same manner as any internal special function register (e.g., the I/O ports, serial port, timers, etc.). The SFR bus, however can only be used for on-chip peripheral blocks and not for peripherals which lie off-chip.

A number of benefits result from direct peripheral connection to the SFR bus. First, peripheral registers residing in the SFR address space can take full advantage of the UCS51's rich set of direct addressing and bit operations. Second, the user interface logic required to connect a peripheral with a core is greatly simplified if not completely eliminated. Finally, code effectiveness and the consequential performance increase, as a result of being able to directly address the SFR bus, make the UCS suitable for applications that were not possible with the 80C51.

UCS51 PERIPHERAL CELLS

Intel offers a family of peripheral cells in the 1.5 micron CHMOS III Cell Library. These cells are designed for the efficient interfacing to the UCS51 cores through the SFR bus.

Cell Name	Cell Description
UCS51BIU	SFR Bus Interface Unit
UCS51AD	8-Bit Analog-to-Digital Converter
UCS51T2	16-Bit Timer
UCS51SIO	UART Serial Interface
UCS51BRG	Baud Rate Generator

UCS51BIU—Bus Interface Unit

The UCS51BIU is an 8-bit Bus Interface Unit with eight inputs and eight outputs. It is designed to provide an interface between on-chip, user-defined peripheral logic and the UCS51 core. Built-in handshaking circuitry aids in the transfer of data between the UCS51 core and a user-defined peripheral.

UCS51AD—Analog-to-Digital Converter Cell

The UCS51AD is an 8-bit, successive approximation type Analog-to-Digital Converter. It features eight user-selectable analog input channels, internal sample and hold, and user-selectable conversion speed control.

UCS51T2—Timer 2 Cell

The UCS51T2 is a 16-bit timer or up/down counter that is a functional super-set of the Timer 2 peripheral found in the 8052 standard product. The UCS51T2 peripheral can function as either a timer or an event counter, and it supports three operating modes: capture, auto-reload and baud-rate generator.

UCS51SIO—Serial I/O Interface Cell

The UCS51SIO is a programmable, full-duplex serial port with five operating modes. It is similar in function to the serial port on the UCS51 core, with the added capability of a fifth operating mode (Mode 4). Because the UCS51SIO is a full-duplex serial port it can transmit and receive simultaneously. It is also receive-buffered, which means that it can begin receiving a second byte before it reads the first byte.

UCS51BRG—Baud-Rate Generator

The UCS51 Baud Rate Generator contains a 14-bit counter register and a 14-bit reload register. By programming specific values into the registers, designers can use the UCS51BRG to generate the baud-rate clock for the UCS51SIO peripheral cell. When used in conjunction with the UCS51SIO, the UCS51BRG supports baud rates of 50 Hz to 19.2 KHz.

A secondary application for the UCS51BRG is as a general-purpose programmable clock divider that is capable of generating clocks ranging from 244 Hz to 4 MHz when using a 16 MHz system clock.

(Note that designers may also create their own peripheral macro-cells using the SSI and MSI Cells in the 1.5 micron library.)

Extended Temperature Operation

The Intel cell library supports three temperature ranges: commercial, industrial, and military. Intel guarantees the specified cell performance as long as the supply voltage and case temperature of the ASIC device remain within the ranges in Table 1.

UCS51 ASIC SUPPORT TOOLS

The Intel ASIC design environment provides customers with a full range of ASIC design tools and utilities for efficient capture, simulation, code development, emulation, and testing of a UCS51-based design.

Design Entry Tool (DET)

The UCS51 DET simplifies the process of designing an ASIC device, and automates the complex connections often involved in capturing a core-based design. DET allows the designer to specify the design from a menu interface, selecting port, timer interrupt options and peripheral addresses, etc. The tool then establishes the appropriate connections between the core, peripherals, and power and ground buses. The designer finally connects the remaining system logic and I/O pads with a schematic editor.

Mainframe Design Verification System (MDVS)

MDVS provides users with an integrated gate-level simulation environment using Intel's reference simulator. MDVS is based on a VAX™ mainframe computer utilizing a Zycad™ hardware accelerator, and offers full timing simulation checks including toggle and spike detection and reporting. MDVS is an extension of the workstation platforms and can be accessed from user sites and Intel Technology Centers.

Workstation Platform Support

Intel offers functional and timing simulation capabilities on Mentor workstations. This allows the designer to complete an entire design or any of the various design phases on an in-house engineering workstation.

Test Vector Generation

Intel tests vector for core-based ASIC's using the same test programs used for its standard products. ASIC designers need only to develop test vectors for their unique logic. Intel provides the ExtASM51 as an extension of Intel's ASM51, providing the system designer with the additional capability of generating vectors for a simulator and production tester.

Emulation Capability

The ICE-UCS51 emulator kit allows software development and system prototyping to occur in parallel with ASIC design. It is a complete development and debug system which allows the system designer to develop and test code for a UCS51-based ASIC product and to emulate ASIC product in the target system.

(For more details of the ASIC design tools see the "ASIC Embedded Controller Handbook".)