OnChip Systems

PT212AT 1200/300 bps Full Duplex Modem

T-75-33-05

Advanced Signal Processing Division **September 1989**

Description

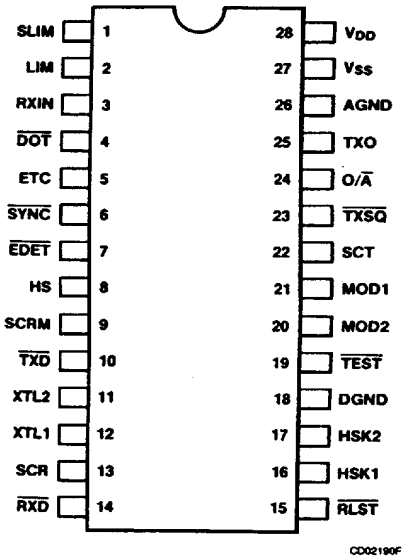
The PT212AT 1200 bps modem circuit is fabricated using an advanced Double-Poly Silicon-Gate CMOS process. The monolithic chip performs all signal processing functions required for a Bell 212A/103 compatible modem. Handshaking protocols, and mode control functions are provided by a general purpose single-chip μC. The PT212AT and μC, along with several components to handle the control and telephone line interfaces, provide a high performance, cost-effective solution for an intelligent Bell 212A-compatible modem design.

The modem chip performs the modulation, demodulation, filtering and certain control and self-test functions required for a Bell 212A-compatible modem, as well as additional functional enhancements. Switched capacitor filters provide channel isolation, spectral shaping and fixed compromise equalization for both high and low speed modes.

A novel switched-capacitor modulator and a digital coherent demodulator provide 1200 bps QPSK operation while a separate digital FSK modulator and demodulator handle the 0-300 bps requirement. The PT212AT includes an integral DTMF tone generator on-chip. The receive filter and energy detector may be configured for call progress tone detection (dialtone, busy, ringback, voice), providing the front end for a smart dialer.

- **Functions as 212A and 103 Compatible Modem**
- **Performs all Signal Processing Functions**
- **Interfaces to Single Chip μC Which Handles Handshaking Protocols and Mode Control Functions**
- **DTMF Tone Generation PT212AT**
- **Pin and Firmware Compatible with the PT212AT (Without integral DTMF) for Easy Upgrade**
- **Call Progress Tone Detection for Smart Dialer Applications**
- **On Chip Oscillator Uses Standard 3.6864 MHz Crystal**
- **Few External Components Required**
- **Industrial Temperature Range Option (−40°C to +85°C)**
- **Operates from +5 and −5 Volt Supplies**
- **Low Operating Power: 35 mW Typical**
- **28-Lead Ceramic DIP, 28-Lead Plastic DIP, and 28-Lead Surface Mount Packages**
- **A PT212AT Designer's Kit Is Available**

Connection Diagram
28-Lead Dip
(Top View)



28-Lead PLCC

(Pin numbers same as 28-Lead DIP. See page 12.)

Order Information

Type	Temperature Range	Package
1. PT212ATC	0 to +70°C	28-Lead Ceramic DIP
2. PT212ATP	0 to +70°C	28-Lead Molded DIP
3. PT212ATJ	0 to +70°C	28-Lead Molded Surface Mount

Absolute Maximum Ratings

V_{DD} to DGND or AGND	7.0 V
V_{SS} to DGND or AGND	−7.0 V
Voltage at any Input	V_{DD} + 0.3 to V_{SS} −0.3 V
Voltage at any Digital Output	V_{DD} + 0.3 V to DGND −0.3 V
Voltage at any Analog Output	V_{DD} + 0.3 V to V_{SS} −0.3 V
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 s)	300°C

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PT212AT

T-75-33-05

Pin No.	Pin Description	
1	SLIM	Soft Limiter Output. Connect external 0.033 μF capacitor here.
2	LIM	Comparator input. Connected external 0.033 μF capacitor here.
3	RXIN	Line signal to modem. From active or passive Hybrid output.
4	$\overline{DOT}$	If HS = 1, forces a 1200 bps dotting pattern on the transmit path, for use when programming the 212AT high speed self-test mode. Both RCV and XMIT paths are in $\overline{SYNC}$ mode during dotting transmission, overriding the setting of $\overline{SYNC}$, and of HSK1, HSK2. If HS = 0, $\overline{DOT}$ HSK1 and HSK2 pins select one of three test conditions, forces a 155 bps dotting pattern for use in lowspeed self-test mode. 1 = Normal Path, 0 = Dotting.
5	ETC	External Transmit Clock. 1200 Hz external clock providing XMTR timing in SYNC mode, selected by MOD1, MOD2 pins. $\overline{TXD}$ changes on negative edge, sampled on positive edge. Provided on SCT pin if selected.
6	$\overline{SYNC}$	Selects CHAR ASYNC or BIT SYNC mode. 1 = ASYNC mode: enables XMIT & RCV buffers, sets character length according to MOD1, MOD2 pins. 0 = SYNC mode: disables buffers, selects TX clock source according to MOD1, MOD2 pins. Active only if HS = 1.
7	$\overline{EDET}$	Energy Detect. In data mode, $\overline{EDET}$ = 0 if valid signal above threshold is present for 155 ± 50 ms, $\overline{EDET}$ = 1 if signal below threshold for > 17 ± 7 ms. In dialer mode, follows on/off variations of call-progress tones, when $\overline{TXSQ}$ = 0
8	HS[1]	Selects modem speed. 1 selects 1200 bps. 0 selects 300 bps. (Note)
9	SCRM	Scrambler. "0" disables scrambler and descrambler for testing purposes.
10	$\overline{TXD}$	XMIT Data. Serial data from host. Disconnected when in digital loop.
11 12	XTL2 XTL1	Frequency control. 3.6864 MHz XTAL oscillator, operating parallel mode. Provides timing, sampling and clocks.
13	SCR	Serial Clock Receive. In SYNC mode, 1200 Hz bit clock recovered from RCVD signal. May be pin-selected (MOD1, MOD2) as local transmit clock (SLAVE mode); provided on SCT pin if selected. $\overline{RXD}$ changes on negative edge, sampled on positive edge. Undefined in ASYNC mode.
14	$\overline{RXD}$	RCVD Data. Serial data to host, Internally clamped to mark (= 1) when modem is in digital loop or $\overline{EDET}$ is inactive (= 1).
15	$\overline{RLST}$	Remote Loop Status, used in RDL mode. Responding modem: sets $\overline{RLST}$ = 0 upon receipt of unscrambled mark for 154 – 231 ms. Initiating modem: asserts $\overline{RLST}$ = 0 upon receipt of scrambled mark for 231 – 308 ms. (See Table 3).
16 17 19	HSK1, HSK2 $\overline{TEST}$	When the $\overline{TEST}$ pin is inactive (high), HSK1 and HSK2 select one of four transmit conditions, for use when programming the Handshake sequences. (*See Table 1*). When $\overline{TEST}$ is active (low), the HSK1 and HSK2 pins select one of three test conditions, or, alternatively, the dialer mode used for call progress tone detection and DTMF tone generation.
18	DGND	Digital Ground
20 21	MOD2[1] MOD1[1]	Selects character length (ASYNC) or TX clock (SYNC). In ASYNC mode, selects 8, 9, 10 or 11 bit character length; in SYNC mode, selects internal, external or recovered RCV clock as XMTR data clock source. Active only if HS = 1. (*See Table 1*)

Notes:

1. For PT212AT in dialer mode, O/$\overline{A}$, HS, MOD1 and MOD2 select the DTMF to be generated (*see Table 2*).

2. The PT212AT is pin and function compatible with the PT212AT (without integral DTMF); in upgrade applications, insure proper state of TXSQ as indicated. See Technical Bulletin M-1.

Pin No.	Pin Description	
22	SCT	Serial Clock Transmit. 1200 Hz clock providing XMTR timing in SYNC mode. SCT source (INT., EXT., SLAVE) selected by MOD1, MOD2 pins. $\overline{TXD}$ changes on negative edge, sampled on positive edge. Internal clock provided in ASYNC mode.
23	$\overline{TXSQ}$[2]	Squelch XMTRS in data mode. 0 = Both XMTRS off; 1 = turns on XMTR selected by HS pin. In dialer mode, 0 = DTMF generator OFF/Call progress detection. 1 = DTMF generator ON.
24	O/$\overline{A}$[1]	Orig/Answer Mode Select. Assigns channels to XMTRS/RCVRS. 1 = Originate mode, 0 = Answer mode.
25	TXO	Line signal from modem. To active or passive Hybrid input. A coupling capacitor of at least 0.033 μf is recommended.
26	AGND	Analog Ground
27	V_{SS}	Negative power supply $V_{SS} = -5.0$ V
28	V_{DD}	Positive power supply $V_{DD} = +5.0$ V

Functional Description*

Refer to Figure 1.

Transmitter

The transmitter consists of high-speed and low-speed modulators, a transmit buffer and scrambler, and a transmit filter and line driver. In high-speed asynchronous mode, transmit data from the Data Terminal Equipment enters the transmit buffer, which synchronizes the data to the internal 1200 bps clock. Data which is underspeed relative to 1200 bps periodically has the last stop bit sampled twice resulting in an added stop bit. Similarly, overspeed input data periodically has unsampled — and therefore deleted — stop bits. The MOD1 and MOD2 pins choose 8, 9, 10 or 11 bit character lengths. In synchronous mode the transmit buffer is disabled. The transmitter clock source may be chosen by MOD1 and MOD2 internal, external or derived from the recovered received data. A scrambler precedes encoding to ensure that the line spectrum is sufficiently distributed to avoid interference with the in-band supervisory single-frequency signaling system employed in most Bell System toll trunks. The randomized spectrum also facilitates timing recovery in the receiver. The scrambler is characterized by the following recursive equation:

$$Y_i = X_i \oplus Y_{i-14} \oplus Y_{i-17}$$

where X_i is the scrambler input bit at time i. Y_i is the scrambler output bit at time i and $\oplus$ denotes the XOR operation.

212A-type modems achieve full-duplex 1200 bps operation by encoding transmitted data by bit-pairs (dibits), thereby halving the apparent data rate. The resultant reduced spectral width allows both frequency channels to coexist in a limited bandwidth telephone channel with practical levels of filtering. The four unique dibits thus obtained are gray-coded and differentially phase modulated onto a carrier at either 1200 Hz (originate mode) or 2400 Hz (answer mode). Each dibit is encoded as a phase change relative to the phase of the preceding signal dibit element:

Dibit	Phase Shift (deg)
00	+90
01	0
11	−90
10	180

At the receiver, the dibits are decoded and the bits are reassembled in the correct sequence. The left-hand digit of the dibit is the one occurring first in the data stream as it enters the modulator after the scrambler. The lowspeed transmitter generates phase-coherent FSK using one of two programmable tone generators. Answer mode mark (2225 Hz) is also utilized as answer tone in both low and high speed operation.

In Dialer mode, both tone generators are employed to generate DTMF tone pairs. The summed modulator outputs drive a lowpass filter which serves as a fixed compromise amplitude and delay equalizer for the phone line and reduces output harmonic energy well below maximum specified levels. The filter output drives an output buffer amplifier with low output impedance. At the TXO pin, the buffer provides 700 mVrms in data mode, for a nominal −9 dBm level at the line, assuming 2 dB loss in the data access arrangement.

DTMF Tone Generation

The PT212AT includes on-chip DTMF generation, using two programmable tone generators. Dialer mode must be selected ($\overline{TEST}$ = HSK1 = HSK2 = 0) for DTMF dialing. The O/$\overline{A}$, HS, MOD1 and MOD2 pins are used to select the required digit according to the encoding scheme *shown in*

*For additional information contact sales office for Applications Note ASP-1 "Theory of Operation–PT212AT" and Technical Bulletins M1, M3 & M4.

Table 2, and the tones are turned on and off by the logic level on $\overline{TXSQ}$. The generated tones meet the applicable CCITT and EIA requirement for tone dialing. DTMF output levels are 0.9 Vrms (low group) and 1.1 Vrms (high group).

Receiver

The received signal from the line-connection circuitry passes through a lowpass filter which performs anti-aliasing and compromise amplitude and delay equalization of the incoming signal. Depending upon mode selection (originate/answer) the following mixer either passes or down converts the signal to the 1200 Hz bandpass filter. In analog loopback mode, the receiver originate and answer mode assignments are inverted, which forces the receiver to operate in the transmitter frequency band. The 1200 Hz bandpass filter passes the desired received signal while attenuating the adjacent transmitted signal component reflected from the line (talker echo). The chosen passband shape converts the spectrum of the received high-speed signal to 100% raised cosine to minimize intersymbol interference in the recovered data. Following the filter is a soft limiter and a signal energy detector. An external capacitor is used to eliminate offset between the soft limiter output and the following limiter.

The energy detector provides a digital indication that energy is present within the filter passband at a level above a preset threshold. At least 2 dB of hysteresis is provided between on and off levels to stabilize the detector output. In dialer mode, the detector output is used to provide logic level indication of the presence of call progress tones.

The limiter output drives the QPSK demodulator and the carrier and clock recovery phase-locked loops. The low speed FSK demodulator shares part of the clock recovery loop. The QPSK demodulator and carrier loop form a digital coherent detector. This technique offers a 2 dB advantage in error performance compared to a differential demodulator. The demodulator output are in-phase (I) and quadrature (Q) binary signals which together represent the recovered dibit stream. The dibit decoder circuit utilizes the recovered clock signal to convert this dibit stream to serial data at 1200 bps.

The recovered bit stream is then descrambled, using the inverse of the transmit scrambler algorithm. In synchronous mode the descrambler output is identically the received data, while in asynchronous mode the descrambler output stream is selectively processed by the receive buffer. Underspeed data presented to the transmitting modem passes essentially unchanged through the receive buffer. Overspeed data, which had stop bits deleted at the transmitter, has those stop bits reinserted by the receive buffer. (Generally, stop bit lengths will be elastic). The receive buffer output is then presented to the receive data pin (RXD) at a nominal intracharacter rate of 1219.05 bps.

Master Clock/Oscillator/Divider Chain

The PT212AT may be controlled by either a quartz crystal operating in parallel mode or by an external signal source at 3.6864 MHz. The crystal should be connected between XTL1 and XTL2 pins, with a mica or high-Q ceramic 30 pF capacitor from each pin to digital ground *(see Figure 1)*. An external circuit may be driven from XTL2. In this case, AC coupling to a high impedance load should be used. Note that total capacitance to ground from XTL2, including such an external circuit, should be 30 pF. Crystal requirements; $R_S < 150$ ohms, $C_L = 18$ pF, parallel mode, tolerance (accuracy, temp, aging) less than ± 75 ppm. An external TTL drive may be applied to the XTL2 pin, with XTL1 grounded. Internal divider chains provide the timing signals required for modulation, demodulation, filtering, buffering, encoding/decoding, energy detection and remote digital loopback. Timing for line connect and disconnect sequences (handshaking) derives from the host controller, ensuring maximum applications flexibility.

Control Considerations

The host controller, whether a dedicated microcontroller or a digital interface, controls the PT212AT as well as the line connect circuit and other IC's. On-chip timing and logic circuitry has been specifically designed to simplify the development of control firmware.

Operating and Test Modes

Table 1 indicates the operating and test modes defined by the eight control pins. The PT212AT (together with the host controller) supports analog loopback, and local and remote digital loopback modes. Analog loopback forces the receiver to the transmitter channel. The controller forces the line control circuit on-hook but continues to monitor the ring indicator. This mode is available for lowspeed, highspeed synchronous and highspeed asynchronous operation. In local digital loop, the modem I.C. isolates the interface, slaves the transmit clock to SCR (high-speed mode), and loops received data back to the transmitter. In remote digital loop, local digital loop is initiated in the far-end modem by request of the near-end modem, if the far-end modem is so enabled. The PT212AT includes the handshake sequences required for this mode; the controller merely monitors $\overline{RLST}$ and controls remote loopback according to *Table 3*. Remote loop is only available in high-speed mode.

T-75-33-05

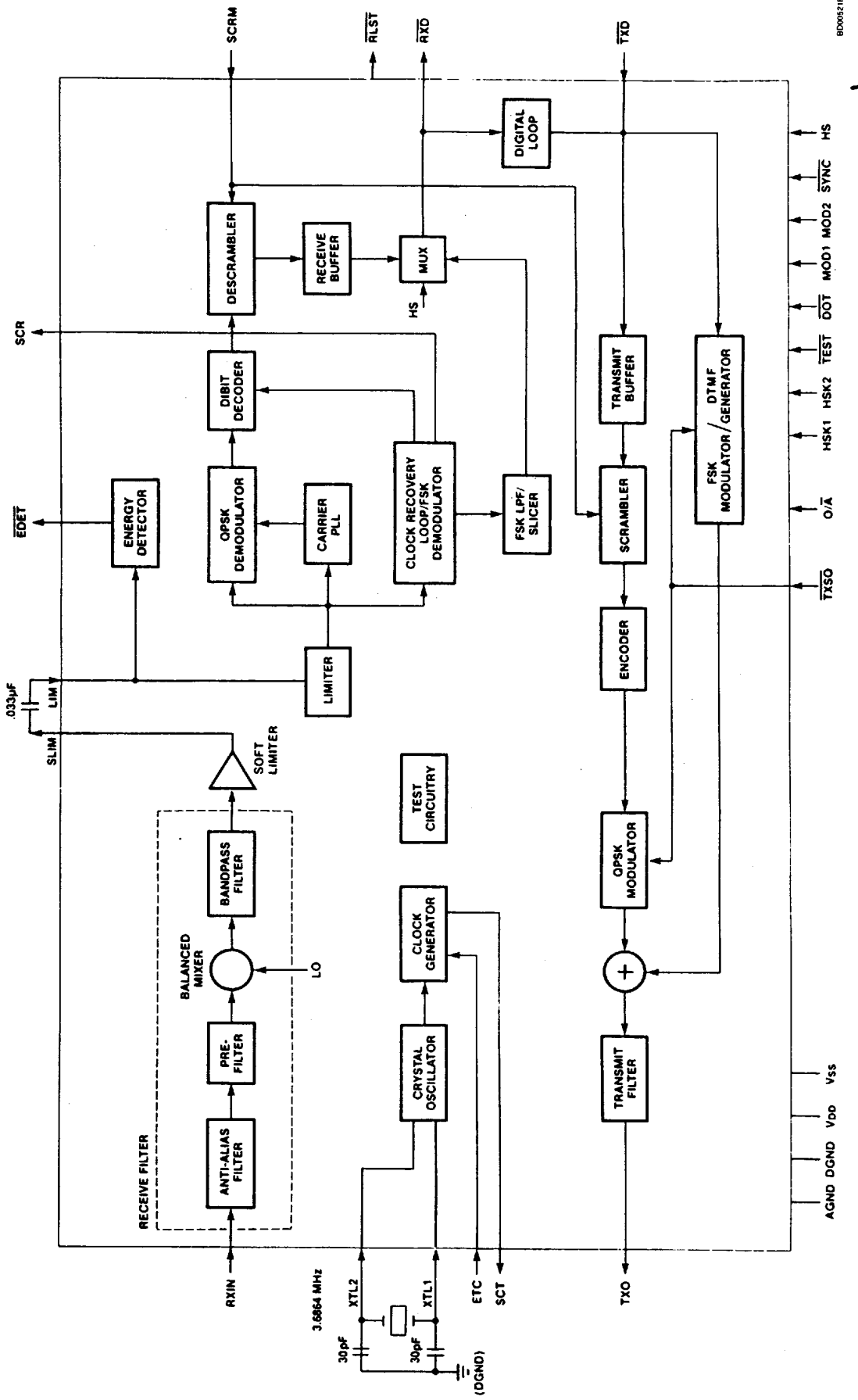


Figure 1 Block Diagram

Answer Tone In this mode, 2225 Hz answer tone is transmitted provided $\overline{TXSQ}$ is inactive high (= 1). Receive data rate is selected as normal with the HS pin. This permits the data rate of the originating modem to be determined while answer tone is continuously transmitted.

Force Continuous Mark Disconnects $\overline{TXD}$ pin from the transmitter and forces the signal internally to a mark (logic 1).

Force Continuous Space Disconnects $\overline{TXD}$ pin from the transmitter and forces the signal internally to a space (logic 0).

Analog Loop Receiver is forced to the transmitter channel. With modem on-hook (disconnected from line) signal from TXO is reflected through hybrid to RXIN.

Local Digital Loop Internally connects $\overline{RXD}$ to $\overline{TXD}$ and SCR to SCT. Transmitted data ($\overline{TXD}$) and clock (ETC) are ignored. SCR and SCT are provided. $\overline{RXD}$ is forced to 1.

Remote Digital Loop Initiating modem: If RDL is initiated ($\overline{TEST}$ = 0, HSK1 = 1, HSK2 = 0), $\overline{TXD}$ is isolated, $\overline{RXD}$ is clamped to a 1 and unscrambled mark is transmitted. When high speed scrambled dotting pattern is detected, scrambled mark is transmitted. At this point, upon receipt of scrambled mark, $\overline{RLST}$ is set to 0.

Responding modem: Upon receipt of unscrambled mark when in data mode ($\overline{TEST}$ = HSK1 = HSK2 = 1), $\overline{RLST}$ is set to 0. Upon detecting this the controller responds by setting $\overline{TEST}$ and HSK2 to 0, and the PT212AT isolates $\overline{TXD}$, clamps $\overline{RXD}$ to 1, and transmits a 1200 bps scrambled dotting pattern. At this point, upon receipt of a scrambled mark signal, the PT212AT internally loops RCVR data and clock to the XMTR, and resets $\overline{RLST}$ to 1. (*See Table 3*)

Dialer Mode The PT212AT provides DTMF tone generation and energy indication at $\overline{EDET}$ pin to identify call progress tones, i.e. dial, busy and ringback. The DTMF digit is selected by the levels on O/$\overline{A}$, HS. MOD1 and MOD2 according to Table 2. Tone generation is turned on and off by the level on $\overline{TXSQ}$. 1 = on, 0 = off.

Electrical Characteristics Unless otherwise noted: V_{DD} = 5.0 V ±5%, V_{SS} = −5.0 V ±5%, DGND = AGND = 0 V, T_A = 0°C to 70°C, typical characteristics specified at V_{DD} = 5.0 V, V_{SS} = −5.0 V, T_A = 25°C; all digital signals are referenced to DGND, all analog signals are referenced to AGND.

Table 1 Operating and Test Modes

$\overline{DOT}$	HS	$\overline{SYNC}$	MOD1	MOD2	$\overline{TEST}$	HSK1	HSK2	Description	SCT
0	–	X	X	X	1	1	1	Dotting Pattern (155 or 1200 bps)	INT
1	–	–	–	–	1	0	0	Answer Tone	X
1	–	–	–	–	1	0	1	Force Continuous Mark	X
1	–	–	–	–	1	1	0	Force Continuous Space	X
1	1	1	0	0	1	1	1	ASYNC, 8 Bit	INT
1	1	1	0	1	1	1	1	ASYNC, 9 Bit	INT
1	1	1	1	1	1	1	1	ASYNC, 10 Bit	INT
1	1	1	1	0	1	1	1	ASYNC, 11 Bit	INT
1	1	0	1	1	1	1	1	SYNC, Internal	INT
1	1	0	1	0	1	1	1	SYNC, Slave	SCR
1	1	0	0	1	1	1	1	SYNC, External	ETC
–	–	–	–	–	0	0	1	Analog Loop	ETC
1	–	X	X	X	0	1	1	Local Digital Loop	SCR
1	1	X	X	X	0	1	0	Response to Far End Request for RDL	SCR
1	0	X	X	X	–	–	–	Low Speed Mode	X
1	X	X	X	X	0	0	0	Dialer Mode[1]	X
1	1	–	–	–	0	1	0	Remote Digital Loop Initiate	X

Key:
SCT – TX Buffer and PSK Modulator Clock
SCR – Receive Clock
ETC – External Clock Input
INT – Internal 1200 Hz Clock
X – Don't Care
— – Set as appropriate for desired operating condition.

Table 2 DTMF Encoding[2]

O/$\overline{A}$	HS	MOD1	MOD2	DTMF Digit
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	*
1	0	1	1	#
1	1	0	0	A
1	1	0	1	B
1	1	1	0	C
1	1	1	1	D

Notes
1. DTMF digit is selected according to Table 2. $\overline{TXSQ}$ enables the tone generator: 1 = ON, 0 = OFF. $\overline{TXSQ}$ = 0 allows energy detection of call progress tones in both the PT212A and PT212AT.
2. For DTMF to operate dialer mode must be asserted ($\overline{TEST}$ = HSK1 = HSK2 = 0).

T-75-33-05

Table 3 Remote Digital Loopback (RDL) Command Sequences

Modem Action	Controller Action	$\overline{TEST}$	HSK1	HSK2	$\overline{RLST}$
Data Mode		1	1	1	1
Initiate RDL: Disable scrambler Disconnect $\overline{TXD}$ Force 1 on $\overline{RXD}$ Transmit unscrambled mark (U.M.) Recognize Dotting for 231 – 308 ms Enable scrambler Transmit scrambled mark (S.M.) Recognize S.M. for 231 – 308 ms Connect $\overline{TXD}$ Unclamp $\overline{RXD}$ "RDL ESTABLISHED"	"INITIATE RDL"	0 0	1 1	0 0	1 0
Response to far end request: U.M. recognized for 154 – 231 ms "RDL REQUESTED" Disconnect $\overline{TXD}$ Force 1 on $\overline{RXD}$ Force Sync Slave Mode Transmit Dotting S.M. recognized Internally loop Receiver to Transmitter "RDL ESTABLISHED"	"RDL RESPONSE OK"	1 0 0	1 1 1	1 0 0	0 0 1
Terminate RDL: Reset to Data Mode	$\overline{TXSQ}$ active 80 ms	1 1	1 1	1* 1	0 1

*$\overline{TEST}$ = HSK1 = HSK2 = 1 may be asserted at any time after "RDL ESTABLISHED" and before terminating.

Energy Detector

Symbol	Characteristic	Condition	Min	Typ	Max	Units
	Data mode					
V_{thon}	OFF/ON Threshold	Voltage Level at RXIN		6.5		mV_{rms}
V_{thoff}	ON/OFF Threshold	Pin In Data Mode		5.2		
t_{on}	Energy Detect Time	At $\overline{EDET}$ Pin	105	155	205	ms
t_{off}	Loss of Energy Detect Time		10	17	24	ms
	Dialer Mode					
V_{thon}	OFF/ON Threshold Dialtone	Voltage Level at RXIN		10		mV_{rms}
V_{thon}	OFF/ON Threshold Busy/Ringback	Pin in Dialer Mode		4.6		
t_{on}	Energy Detect in the Dialer Mode (Detecting Call Progress Tones)	At $\overline{EDET}$ Pin	25	30	35	ms
t_{off}	Energy Detect in the Dialer Mode (Detecting Call Progress Tones)		30	36	42	ms

PT212AT

T-75-33-05

Analog Line Interface

Symbol	Characteristic	Condition	Min	Typ	Max	Units
V_{line}	Output Level at TXO: Data Mode			0.7		V_{rms}
V_{tonh}	Output Level at TXO: DTMF HIGH Group			1.1		V_{rms}
V_{tonl}	Output Level at TXO: DTMF LOW Group			0.9		V_{rms}
$V_{\overline{TXSQ}}$	Output Level at TXO: $\overline{TXSQ}$ Active			0.3		mV_{rms}
P_{ext}	Extraneous frequency output relative to DTMF power.	Any DTMF digit			-20	dB
Z_{RXIN}	Input Impedance at RXIN			100		K
V_{oo}	Output Offset at TXO			5.0		mV

Masterclock Input

Symbol	Characteristic	Condition	Min	Typ	Max	Units
F_{clock}	Clock Frequency			3.6864		MHz
T_{clock}	Clock Frequency Tolerance		-.01		+.01	%
V_{exth}	External Clock Input HIGH	XTL2 driven and XTL1 grounded	4.5			V
V_{extl}	External Clock Input LOW	XTL2 driven and XTL1 grounded			0.5	V

Digital Interface

Symbol	Characteristic	Condition	Min	Typ	Max	Units
V_{IL}	Input Voltage LOW				0.6	V
V_{IH}	Input Voltage HIGH		2.2			V
V_{OL}	Output Voltage LOW	$I_L = 2.0$ mA			0.6	V
V_{OH}	Output Voltage HIGH	$I_L = -2.0$ mA	3.0			V
I_L	Input Current LOW	$DGND \leq V_{IN} \leq V_{IL}$, All Digital Inputs	-100			μA
I_{IH}	Input Current HIGH	$V_{IH} \leq V_{IN} \leq V_{DD}$	-50			μA
I_{DD}	Operating Current	$V_{DD} = 5.0$ V No Analog Signals		4.3	10	mA
I_{SS}	Operating Current	$V_{SS} = -5.0$ V No Analog Signals		-2.7	-5.0	mA

Transmit (Async/Sync) and Receive (Sync/Async) Buffers

Symbol	Characteristic	Condition	Min	Typ	Max	Units
L_{txchar}	Input Character Length	Start bit + data bits + stop bit	8		11	bits
R_{txchar}	Input Intracharacter Signaling Rate	At $\overline{TXD}$ pin	1170	1200	1212	bps
L_{break}	Input Break Sequence Length	At $\overline{TXD}$ pin	23			bits
R_{txchar}	Output Intracharacter Signaling Rate	At $\overline{RXD}$ pin		1219.05		bps
F_{cxr} (ORIG)	HS Cxr Freq. (Orig. Mode)	Unmodulated Carrier		1200		Hz
F_{cxr} (ANS)	HS Cxr Freq. (Ans. Mode)	Unmodulated Carrier		2400		Hz
Baud	Dibit Rate	High Speed Mode		600		Baud
F_{mark} (ORIG)	Mark Frequency Originate Mode (1270)	Low Speed Mode		1269.42		Hz
F_{space} (ORIG)	Space Frequency Originate Mode (1070)	Low Speed Mode		1066.67		Hz

T-75-33-05

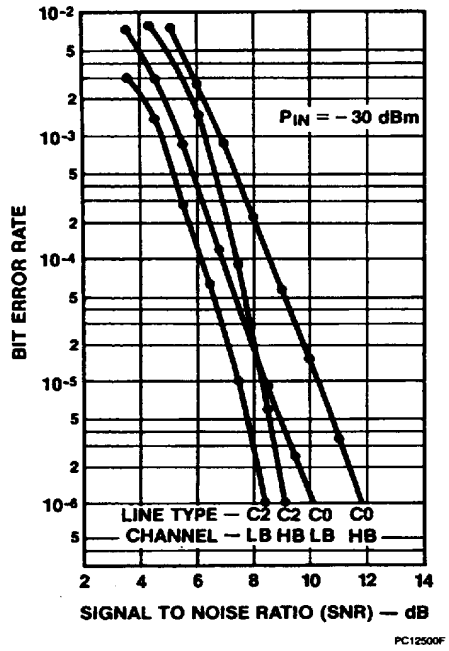
Transmit (Async/Sync) and Receive (Sync/Async) Buffers (Continued)

Symbol	Characteristic	Condition	Min	Typ	Max	Units
F_{mark} (ANS)	Mark Frequency Answer Mode/Answer Tone (2225)	Low Speed Mode		2226.09		Hz
F_{space} (ANS)	Space Frequency Answer Mode (2025)	Low Speed Mode		2021.05		Hz
F_{tonl}	DTMF Low Frequency Tone Group	Dialer Mode		698.2 771.9 853.3 942.3		Hz
F_{tonh}	DTMF High Frequency Tone Group	Dialer Mode		1209.4 1335.7 1476.9 1634.0		Hz
T_{ol}	Tolerance of all above Frequencies/Data Rates		−0.01		+0.01	%
bps	Data Rate	Low Speed Mode	0		300	bps

System Performance

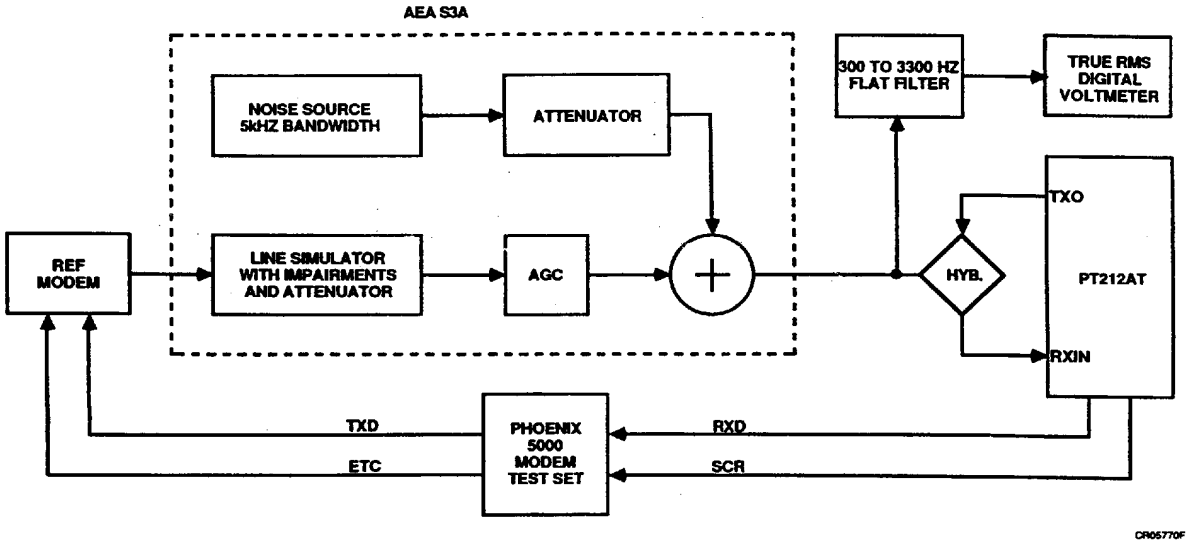
Symbol	Characteristic	Condition	Min	Typ	Max	Units
BER (High-Band Receive)	**Bit Error Rate:** SNR required for BER = 10^{-5} @ 1200 bps on a 3002-C0 line, with 5 kHz white noise referred to 3 KHz. Figures shown are for originate mode. (Note: P_{line} values assume 4 dB net gain from line to RXIN. Net gain varies with DAA type and design).	P_{line} = −34 dBm P_{line} = −48 dBm		10 11	dB dB	
	Telegraph Isochronous Distortion	Back-to-Back, 300 bps (Low Speed Mode)		10		% Peak

Figure 2 Bit Error Rate vs Signal-to-Noise Ratio



Note
BER measured in synchronous mode, using an AEA S3A channel simulator.

Figure 3 2-Wire Bit Error Test Setup



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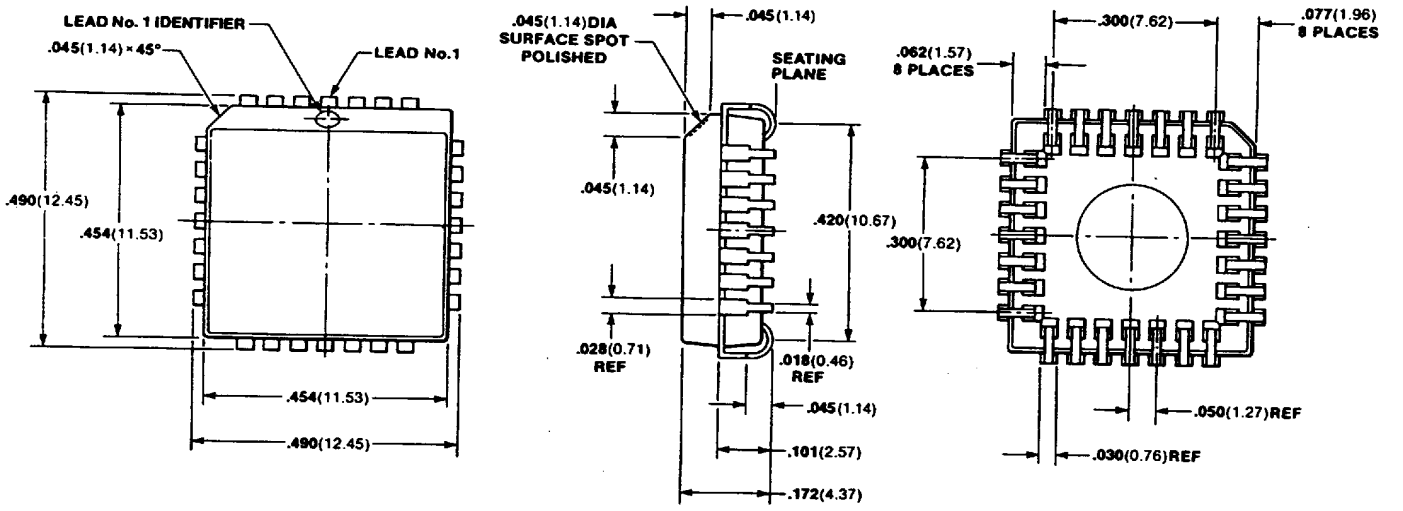
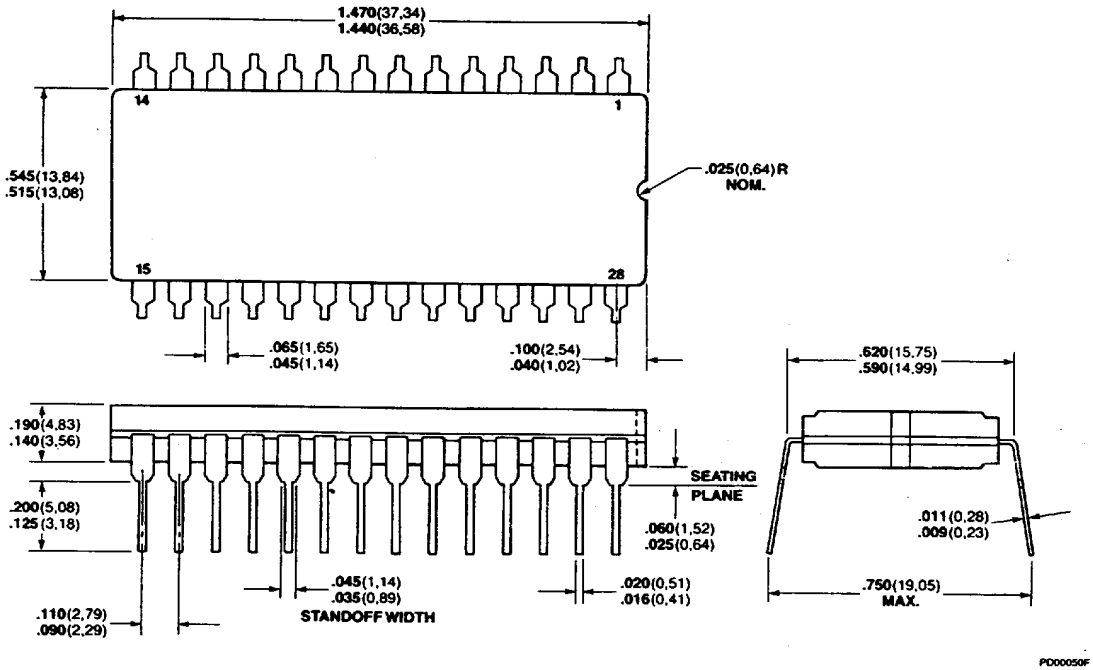
28-PLCC



28-Lead C-DIP



28-Lead P-DIP

*Consult Factory