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Status	Product Specification
Memory Products	

82S212
82S212A
2304-bit TTL bipolar RAM

DESCRIPTION

The organization of the 82S212 and 82S212A allow byte wide storage of data, including parity. Where parity is not required, the ninth bit can be used as a tag for each word stored. The 82S212 and 82S212A are ideal for scratch pads, push down stacks, buffer memories, and other internal memory applications in which space and performance requirements dictate a wide data path in favor of word depth.

Data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of Read/Write operations using a common bus.

Ordering information can be found on the following page.

The 82S212 and 82S212A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Handbook.

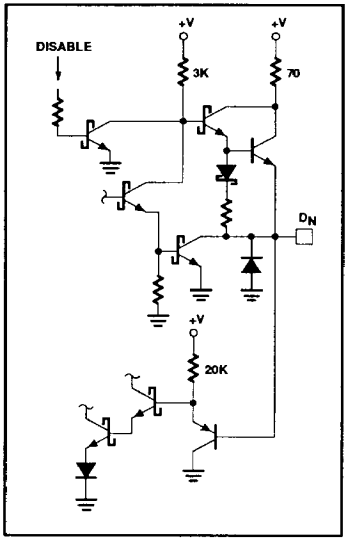
FEATURES

- Address access time:
  - N82S212: 45ns max
  - N82S212A: 35ns max
- Power dissipation: 0.3mW/bit typ
- Schottky clamped TTL
- One Chip Enable input
- Common I/O
  - Inputs: PNP Buffered
  - Outputs: 3-State

APPLICATIONS

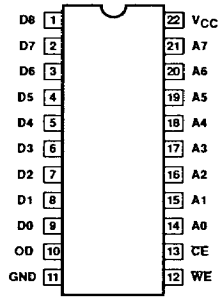
- Cache memory
- Buffer storage
- Writable control store

TYPICAL I/O STRUCTURE

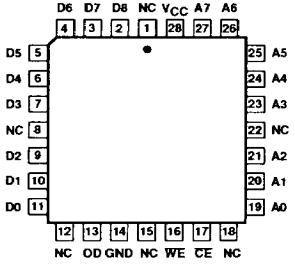


PIN CONFIGURATIONS

N Package



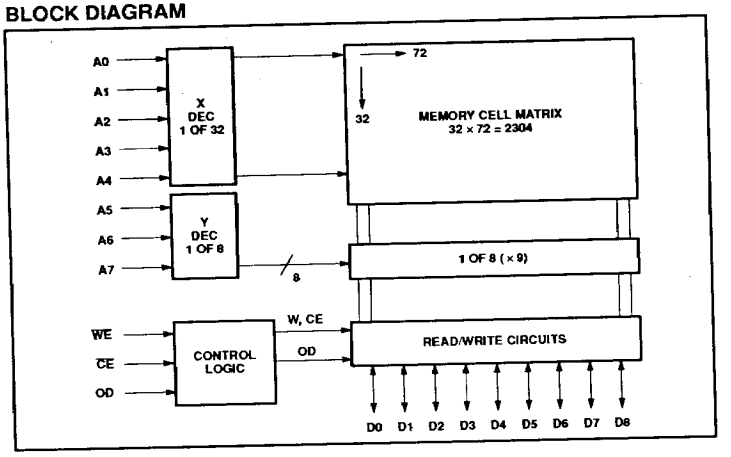
A Package



2304-bit TTL bipolar RAM (256 × 9)

82S212 / 82S212A

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
22-Pin Plastic Dual-In-Line 400mil-wide	N82S212 N, N82S212A N
28-Pin Plastic Leaded Chip Carrier 450mil-square	N82S212 A, N82S212A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH}	Output voltage High	+5.5	V_{DC}
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			V
V_{IC}	Clamp[3]	V_{CC} = 4.75V, I_{IN} = -12mA			-1.5	V
Output voltage[2]						
V_{OH}	High	I_{OL} = -2mA	2.4			V
V_{OL}	Low[3]	V_{CC} = 4.75V, I_{OL} = 8.0mA			0.5	V
Input current						
I_{IL}	Low	V_{IN} = 0.45V			-100	μA
I_{IH}	High	V_{IN} = 5.5V			25	μA
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}$ = High or OD = High, V_{OUT} = 5.5V			40	μA
		$\overline{CE}$ = High or OD = High, V_{OUT} = 0.5V			-100	μA
I_{OS}	Short circuit[3, 4]	$\overline{CE}$ = OD = Low, V_{OUT} = 0V	-15		-70	mA
Supply current[5]						
I_{CC}		V_{CC} = 5.25V		135	185	mA
Capacitance						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Measured on one pin at a time.
4. Duration of I_{OS} test should not exceed one second.
5. I_{CC} is measured with the Write Enable and Memory Enable inputs grounded, all other inputs at 0.45V, and the outputs open.

TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE}$	OD	D_N IN/OUT
Disable output	X	X	1	Hi-Z
Disable R/W	X	1	X	Hi-Z
Write	0	0	1	Data in
Read	1	0	0	Data out

X = Don't care

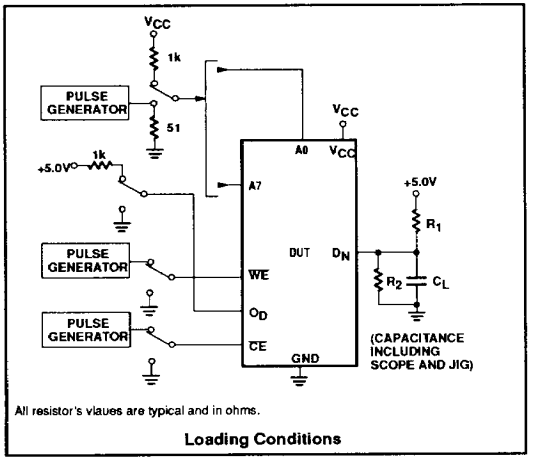
AC ELECTRICAL CHARACTERISTICS

$R_1 = 600\Omega$, $R_2 = 900\Omega$, $C_L = 30pF$, $0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER[1]	TO	FROM	N82S212			N82S212A			UNIT
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
Access time										
t_{AA}	Address	Output	Address			45			35	ns
Enable time										
t_{OD}	Output	Output	OD	5		25			25	ns
t_{CE}	Output	Output	Chip Enable			25			25	ns
Disable time[3]										
t_{OD}	Output	Output	OD			25			25	ns
t_{CD}	Output	Output	Chip Enable			25			25	ns
Pulse width										
t_{WP}[4]	Write			25			25			ns
Setup and hold time										
t_{WSC}	Setup time	Write	Chip Enable	5			5			ns
t_{WHC}	Hold time	Chip Enable	Write	5			5			ns
t_{WSD}	Setup time	Write	Data	25			25			ns
t_{WHD}	Hold time	Data	Write	5			5			ns
t_{WSA}[5]	Setup time	Write	Address	5			5			ns
t_{WHA}	Hold time	Address	Write	5			5			ns
t_{SO}	Setup time (from disabled state)	Chip Enable	OD	5			5			ns
t_{HO}	Hold time	OD	Chip Enable	5			5			ns

NOTES:
1. The operating ambient tempeature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warmup.
2. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
3. Measured at a delta of 0.5V from Logic level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
4. Measured with minimum t_{WSA}.
5. Measured with minimum t_{WP}.

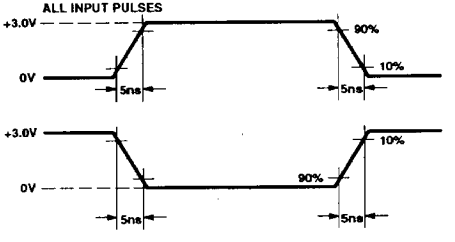
TEST LOAD CIRCUIT



All resistor's values are typical and in ohms.

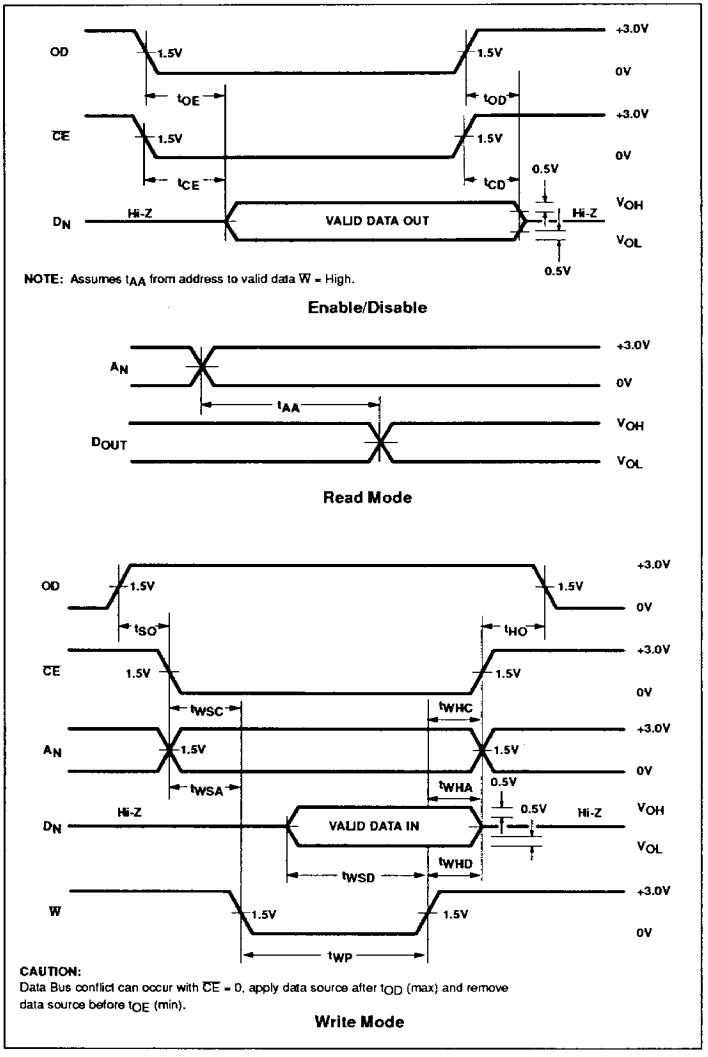
Loading Conditions

VOLTAGE WAVEFORMS



Input Pulses

TIMING DIAGRAMS



MEMORY TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{AA}	Delay between beginning of valid Address (with Chip Enable Low) and when Data Output becomes valid.
t_{OE}	Delay between beginning of Output Disable Low (with Address valid) and when Data Output becomes valid.
t_{CE}	Delay between beginning of Chip Enable Low (with Address valid) and when Data Output becomes valid.
t_{OD}	Delay between when Output Disable becomes High and Data Output is in Off-State.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in Off-State.
t_{WP}	Width of Write Enable pulse.
t_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
t_{WHD}	Required delay between end of Write Enable pulse and end of valid input data.
t_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
t_{WHD}	Required delay between end of Write Enable pulse and end of valid input data.
t_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
t_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.
t_{SO}	Set-up time between OD going High and $\overline{CE}$ going Low.
t_{HO}	Hold time for OD after $\overline{CE}$ goes High.