

DRAM MODULE

MT9LD272(X)
 MT18LD472(F)(X)
 MT36LD872(F)(X)

FEATURES

- JEDEC-standard ECC pinout in a 168-pin, dual-in-line memory module (DIMM)
- 16MB (2 Meg x 72), 32MB (4 Meg x 72), 64MB (8 Meg x 72)
- State-of-the-art, high-performance CMOS silicon-gate process
- Single +3.3V $\pm 0.3V$ power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE- RAS# (CBR) and HIDDEN
- All inputs are buffered except RAS#
- 2,048-cycle (11 row-, 11 column addresses) or 4,096-cycle (12 row-, 10 column addresses)
- FAST PAGE MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- 5V-tolerant inputs and I/Os (5.5V maximum V_{IH} level)

OPTIONS

- Refresh
2,048-cycle across 32ms
4,096-cycle across 64ms
(32MB and 64MB only)
- Packages
168-pin DIMM (gold)
- Timing
50ns access
60ns access
70ns access
- Access Cycle
FAST PAGE MODE
EDO PAGE MODE

** EDO versions only

MARKING

Blank
 F
 G
 -5**
 -6
 -7
 Blank
 X

KEY TIMING PARAMETERS

EDO Operating Mode

SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{CAS}
-5	84ns	50ns	20ns	30ns	18ns	8ns
-6	104ns	60ns	25ns	35ns	20ns	10ns
-7	124ns	70ns	30ns	40ns	25ns	12ns

FPM Operating Mode

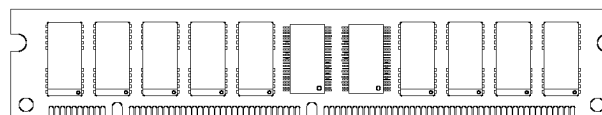
SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{RP}
-6	110ns	60ns	35ns	35ns	20ns	40ns
-7	130ns	70ns	40ns	40ns	25ns	50ns

PIN ASSIGNMENT (Front View)

168-Pin DIMM

(DE-8) 2 Meg x 72 (shown)

(DE-7) 4 Meg x 72, (DE-18) 8 Meg x 72



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	OE2#	86	DQ36	128	RFU
3	DQ1	45	RAS2#	87	DQ37	129	NC/RAS3#*
4	DQ2	46	CAS4#	88	DQ38	130	NC/CAS5#*
5	DQ3	47	RFU	89	DQ39	131	RFU
6	Vcc	48	WE2#	90	Vcc	132	PDE#
7	DQ4	49	Vcc	91	DQ40	133	Vcc
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	Vcc	101	DQ49	143	Vcc
18	Vcc	60	DQ24	102	Vcc	144	DQ60
19	DQ14	61	RFU	103	DQ50	145	RFU
20	DQ15	62	RFU	104	DQ51	146	RFU
21	DQ16	63	RFU	105	DQ52	147	RFU
22	DQ17	64	RFU	106	DQ53	148	RFU
23	Vss	65	DQ25	107	Vss	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	Vcc	68	Vss	110	Vcc	152	Vss
27	WE0#	69	DQ28	111	RFU	153	DQ64
28	CAS0#	70	DQ29	112	NC/CAS1#*	154	DQ65
29	RFU	71	DQ30	113	RFU	155	DQ66
30	RAS0#	72	DQ31	114	NC/RAS1#*	156	DQ67
31	OE0#	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ32	116	Vss	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	A11	164	PD4
39	NC (A12)	81	PD5	123	NC (A13)	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	Vcc	126	B0	168	Vcc

* 64MB version only

PART NUMBERS

EDO Operating Mode

PART NUMBER	CONFIGURATION	REFRESH
MT9LD272G-xx X	2 Meg x 72 ECC	2K refresh
MT18LD472G-xx X	4 Meg x 72 ECC	2K refresh
MT18LD472FG-xx X	4 Meg x 72 ECC	4K refresh
MT36LD872G-xx X	8 Meg x 72 ECC	2K refresh
MT36LD872FG-xx X	8 Meg x 72 ECC	4K refresh

xx = speed

FPM Operating Mode

PART NUMBER	CONFIGURATION	REFRESH
MT9LD272G-xx	2 Meg x 72 ECC	2K refresh
MT18LD472G-xx	4 Meg x 72 ECC	2K refresh
MT18LD472FG-xx	4 Meg x 72 ECC	4K refresh
MT36LD872G-xx	8 Meg x 72 ECC	2K refresh
MT36LD872FG-xx	8 Meg x 72 ECC	4K refresh

xx = speed

GENERAL DESCRIPTION

The MT9LD272(X), MT18LD472(F)(X) and MT36LD872(F)(X) are randomly accessed 16MB, 32MB and 64MB solid-state memories organized in a x72 configuration. It is specially processed to operate from 3.0V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the address bits. Two copies of address 0 (A0 and B0) are defined to allow maximum performance for 4-byte applications which interleave between two 4-byte banks. A0 is common to the DRAMs used for DQ0-DQ35, while B0 is common to the DRAMs used for DQ36-DQ71. RAS# is used to latch the first 11/12 bits and CAS# the latter 10/11 bits.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates READ mode while a logic LOW on WE# dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# was taken LOW. During EARLY WRITE cycles, the data-outputs (Q) will remain High-Z regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data-outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no write will occur, and the data-outputs will drive read data from the accessed location.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS# followed by a column address strobed-in by CAS#. CAS# may be toggled-in by holding RAS# LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST PAGE MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (^tCP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipeline READs.

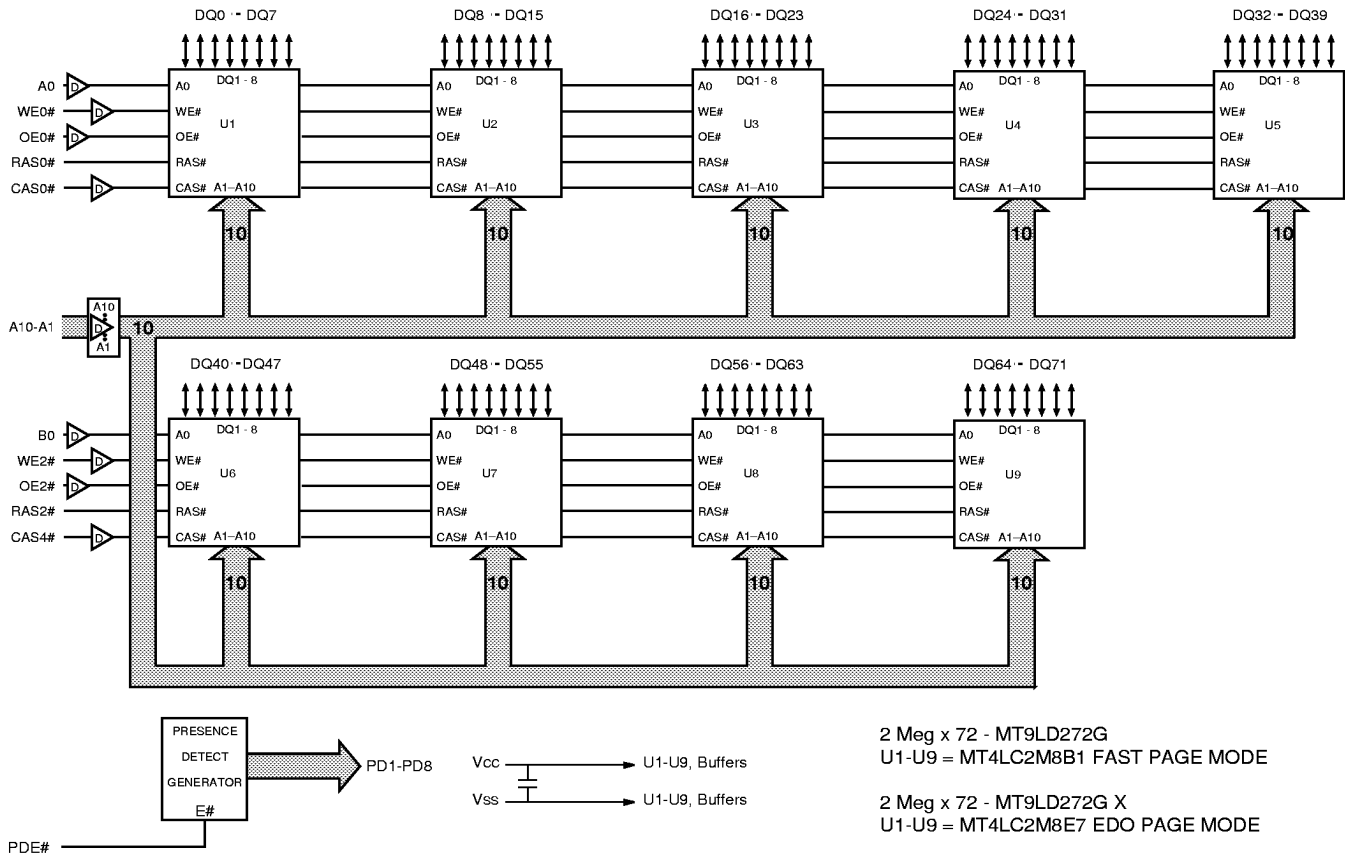
FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO-PAGE-MODE DRAMs operate similar to FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS# goes HIGH during READs, provided RAS# and OE# are held LOW. If OE# is pulsed while RAS# and CAS# are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE# is toggled or pulsed after CAS# goes HIGH while RAS# remains LOW, data will transition to and remain High-Z.

During an application, if the DQ outputs are wire OR'd, OE# must be used to disable idle banks of DRAMs. Alternatively, pulsing WE# to the idle banks during CAS# HIGH time will also High-Z the outputs. Independent of OE# control, the outputs will disable after ^tOFF, which is referenced from the rising edge of RAS# or CAS#, whichever occurs last (reference the MT4LC4M4E8 DRAM data sheet for additional information on EDO functionality).

REFRESH

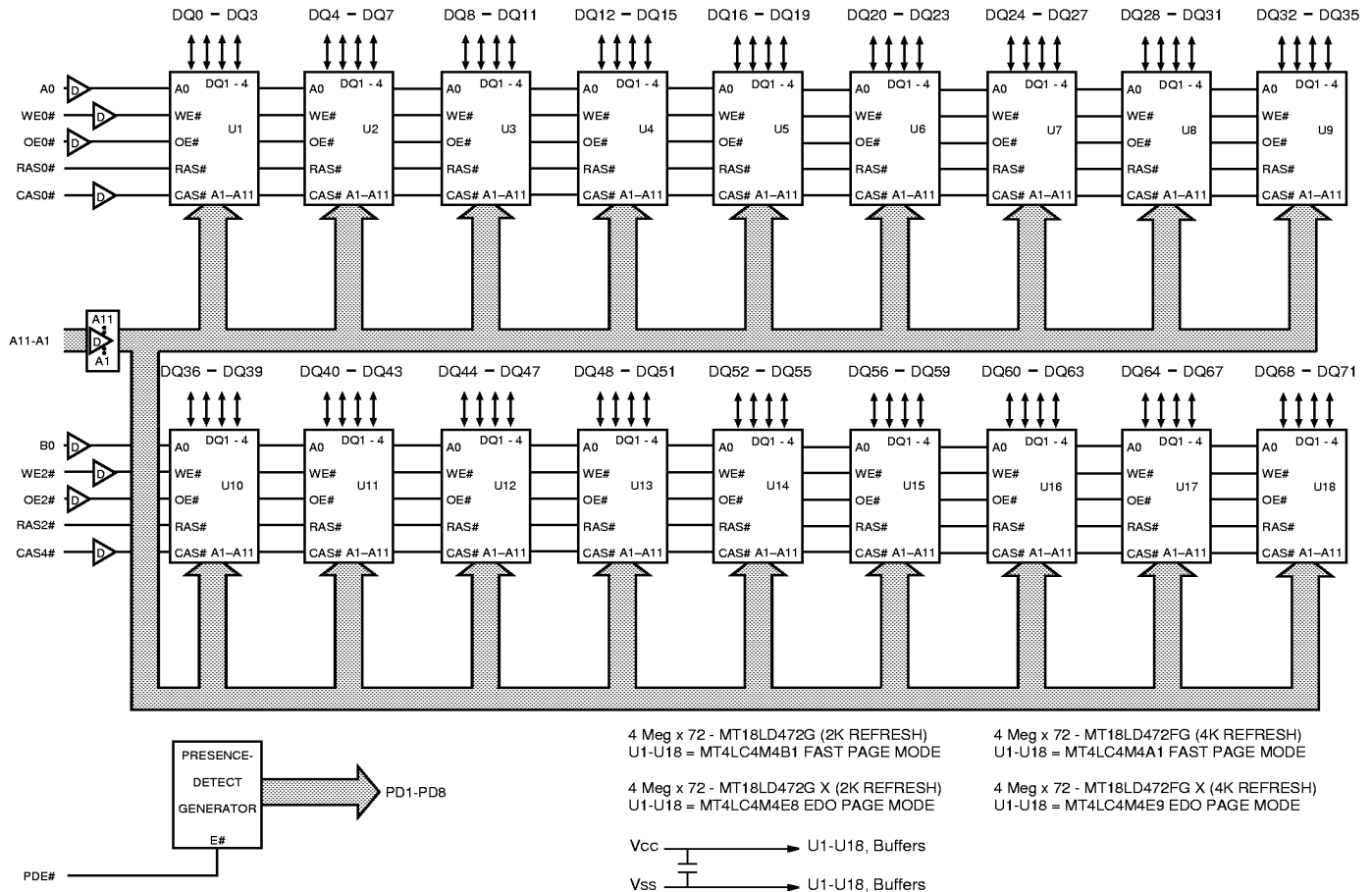
Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Correct memory cell data is preserved by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# refresh cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses are executed at least every ^tREF, regardless of sequence. The CBR Refresh cycle will invoke the internal refresh counter for automatic RAS# addressing.

**FUNCTIONAL BLOCK DIAGRAM
MT9LD272(X) (16MB)**



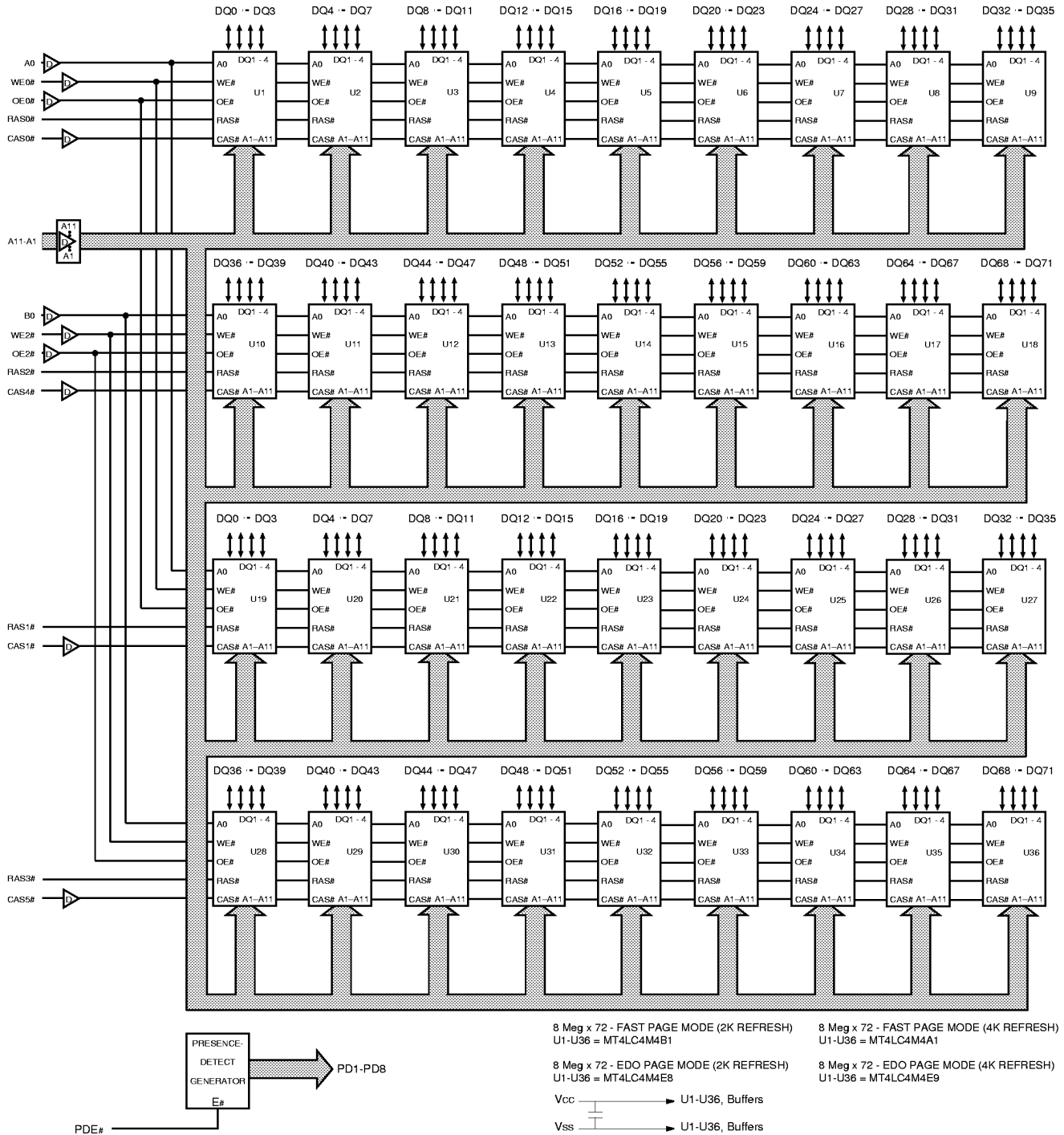
NOTE: 1. All inputs with the exception of RAS# are redriven.
2. D = line buffers.

**FUNCTIONAL BLOCK DIAGRAM
MT18LD472(F)(X) (32MB)**



NOTE: 1. All inputs with the exception of RAS# are redriven.
2. D = line buffers.

**FUNCTIONAL BLOCK DIAGRAM
MT36LD872(F)(X) (64MB)**



NOTE: 1. All inputs with the exception of RAS# are redriven.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45, 114, 129	RAS0#-RAS3#	Input	Row-Address Strobe: RAS# is used to clock-in the row-address bits. Two RAS# inputs allow for one x72 bank or two x36 banks.
28, 46, 112, 130	CAS0#, CAS1#, CAS4#, CAS5#	Buffered Input	Column-Address Strobe: CAS# is used to clock-in the column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles.
27, 48	WE0#, WE2#	Buffered Input	Write Enable: WE# is the READ/WRITE control for the DQ pins. WE0# controls DQ0-DQ35. WE2# controls DQ36-DQ71. If WE# is LOW prior to CAS# going LOW, the access is an EARLY WRITE cycle. If WE# is HIGH while CAS# is LOW, the access is a READ cycle, provided OE# is also LOW. If WE# goes LOW after CAS# goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	OE0#, OE2#	Buffered Input	Output Enable: OE# is the input/output control for the DQ pins. OE0# controls DQ0-DQ35. OE2# controls DQ36-DQ71. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-122, 126	A0-A11, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by RAS# and CAS#. A0 is common to the DRAMs used for DQ0-DQ35 while B0 is common to the DRAMs used for DQ36-DQ71.
2-5, 7-11, 13-17, 19-22, 52-53, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-106, 136-137, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ71	Input/Output	Data I/O: For WRITE cycles, DQ0-DQ71 act as inputs to the addressed DRAM location. For READ access cycles, DQ0-DQ71 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	Buffered Output	Presence-Detect: These pins are read by the host system and tell the system the DIMM's personality. They will be either no connect (1) or they will be driven to Vol (0).
29, 41-42, 47, 61-64, 111, 113, 115, 125, 128, 131, 145-148	RFU	—	RFU: These pins should be left unconnected (reserved for future use).
6, 18, 26, 40, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	Vcc	Supply	Power Supply: +3.3V $\pm$ 0.3V

PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152, 162	Vss	Supply	Ground
83, 167	ID0, ID1	Output	ID bits: ID0 = DIMM type. ID1 = Refresh Mode. These pins will be either left floating (NC) or they will be grounded (Vss).
132	PDE#	Input	Presence-Detect Enable: PDE# is the READ control for the buffered presence-detect pins.
24-25, 39, 50-51, 108-109, 112, 114, 122-123, 129, 130, 134-135, 150, 161	NC	—	No connect

TRUTH TABLE

FUNCTION		RAS#	CAS#	WE#	OE#	PDE#	ADDRESSES		DATA-IN/OUT
							tR	tC	DQ0-71
Standby		H	H→X	X	X	X	X	X	High-Z
READ		L	L	H	L	X	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	X	ROW	COL	Data-Out, Data-In
EDO/FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	X	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	X	n/a	COL	Data-Out
	Any Cycle (X version)	L	L→H	H	L	X	n/a	n/a	Data-Out
EDO/FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	X	n/a	COL	Data-In
EDO/FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	X	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	X	n/a	COL	Data-Out, Data-In
RAS#-ONLY REFRESH		H	X	X	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	X	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	X	High-Z
READ PRESENCE-DETECTS		X	X	X	X	L	X	X	Not Affected

PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	Module Configuration	Row/Column Addresses	ID0	ID1	1	2	3	4	5	6	7	8
0MB	No module installed	X			1	1	1	1				
8MB	1 Meg x 64/72	10/9			1	1	0	0				
8MB	1 Meg x 64/72	10/10			0	0	1	0				
16MB	2 Meg x 64/72	10/10			1	0	1	0				
• 16MB	2 Meg x 64/72	11/10			1	0	0	1				
32MB	4 Meg x 64/72	11/10			0	1	0	1				
• 32MB	4 Meg x 64/72	12*/11*			1	1	0	1				
• 64MB	8 Meg x 64/72	12*/11*			0	0	1	1				
Page Mode		Fast Page Mode							0			
		EDO Page Mode							1			
Access Timing		70ns								0	1	
		60ns								1	1	
		50ns								0	0	
Refresh Control		Standard		Vss								
Data Width		x64, No Parity	Vss									1
		x72, ECC	Vss									0

NOTE: Vss = ground; 0 = Vol; 1 = NC.

* This addressing includes a redundant address to allow mixing of 12/10 and 11/11 DRAMs with the same presence-detect setting.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to V_{SS} -1V to +4.6V
Voltage on Inputs or I/O Pins
Relative to V_{SS} -1V to +5.5V
Operating Temperature, T_A (ambient) 0°C to +70°C
Storage Temperature (plastic) -55°C to +125°C
Power Dissipation 9W
Short Circuit Output Current 50mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 5, 6) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYM	MIN	MAX	UNITS	NOTES
Supply Voltage		V _{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		V _{IH}	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs		V _{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V _{IN} ≤ 5.5V (All other pins not under test = 0V)	CAS0-1#, CAS4-5# A0-A11, B0, PDE# WE0,2#, OE0,2#	I _{I1}	-2	2	μA	
	RAS0#-RAS3#	I _{I2}	-18	18	μA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V _{OUT} ≤ 5.5V)	DQ0-DQ71, PD1-PD8	I _{OZ}	-10	10	μA	
OUTPUT LEVELS Output High Voltage (I _{OUT} = -2mA) Output Low Voltage (I _{OUT} = 2mA)		V _{OH}	2.4		V	
		V _{OL}		0.4	V	

2,048-CYCLE REFRESH I_{CC} OPERATING CONDITIONS AND MAXIMUM LIMITS

 (Notes: 1, 5, 6) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX			UNITS	NOTES
			-5*	-6	-7		
STANDBY CURRENT: (TTL) (RAS# = CAS# = V _{IH})	I _{CC1}	16MB	72	72	72	mA	
		32MB	90	90	90		
		64MB	132	132	132		
STANDBY CURRENT: (CMOS) (RAS# = CAS# = V _{CC} -0.2V)	I _{CC2}	16MB	4.5	4.5	4.5	mA	
		32MB	9	9	9		
		64MB	18	18	18		
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^t RC = ^t RC [MIN])	I _{CC3}	16MB	990	900	810	mA	3, 29
		32MB	1,980	1,800	1,620		
		64MB	2,070	1,890	1,710		
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V _{IL} , CAS#, address cycling: ^t PC = ^t PC [MIN])	I _{CC4}	16MB	-	720	630	mA	3, 29
		32MB	-	1,440	1,260		
		64MB	-	1,530	1,350		
OPERATING CURRENT: EDO PAGE MODE (X version only) Average power supply current (RAS# = V _{IL} , CAS#, address cycling: ^t PC = ^t PC [MIN])	I _{CC5} (X only)	16MB	990	900	810	mA	3, 29
		32MB	1,980	1,800	1,620		
		64MB	2,070	1,890	1,710		
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V _{IH} : ^t RC = ^t RC [MIN])	I _{CC6}	16MB	990	900	810	mA	3, 29
		32MB	1,980	1,800	1,620		
		64MB	2,070	1,890	1,710		
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^t RC = ^t RC [MIN])	I _{CC7}	16MB	990	900	810	mA	3, 4
		32MB	1,980	1,800	1,620		
		64MB	2,070	1,890	1,710		

* EDO versions only

4,096-CYCLE REFRESH I_{CC} OPERATING CONDITIONS AND MAXIMUM LIMITS

 (Notes: 1, 5, 6) ($V_{CC} = +3.3V \pm 0.3V$)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX			UNITS	NOTES
			-5*	-6	-7		
STANDBY CURRENT: (TTL) (RAS# = CAS# = V_{IH})	I_{CC1}	32MB	90	90	90	mA	
		64MB	132	132	132		
STANDBY CURRENT: (CMOS) (RAS# = CAS# = $V_{CC} - 0.2V$)	I_{CC2}	32MB	9	9	9	mA	
		64MB	18	18	18		
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: $t_{RC} = t_{RC} [MIN]$)	I_{CC3}	32MB	1,620	1,440	1,260	mA	3, 29
		64MB	1,710	1,530	1,350		
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V_{IL} , CAS#, address cycling: $t_{PC} = t_{PC} [MIN]$)	I_{CC4}	32MB	-	1,260	1,080	mA	3, 29
		64MB	-	1,350	1,170		
OPERATING CURRENT: EDO PAGE MODE (X version only) Average power supply current (RAS# = V_{IL} , CAS#, address cycling: $t_{PC} = t_{PC} [MIN]$)	I_{CC5} (X only)	32MB	1,800	1,620	1,440	mA	3, 29
		64MB	1,890	1,710	1,530		
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH} : $t_{RC} = t_{RC} [MIN]$)	I_{CC6}	32MB	1,620	1,440	1,260	mA	3, 29
		64MB	1,710	1,530	1,350		
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: $t_{RC} = t_{RC} [MIN]$)	I_{CC7}	32MB	1,620	1,440	1,260	mA	3, 4
		64MB	1,710	1,530	1,350		

* EDO versions only

CAPACITANCE

PARAMETER	SYM	MAX			UNITS	NOTES
		16MB	32MB	64MB		
Input Capacitance: A0-A11, B0, PDE#	C _{I1}	9	9	9	pF	2
Input Capacitance: WE0#, WE2#, OE0#, OE2#, CAS0#, CAS4#	C _{I2}	9	9	9	pF	2
Input Capacitance: RAS0#-RAS3#	C _{I3}	39	67	67	pF	2
Input/Output Capacitance: DQ0-DQ71	C _{IO}	10	10	18	pF	2
Output Capacitance: PD1-PD8	C _O	10	10	10	pF	2

FAST PAGE MODE

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 29) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX		
Access time from column-address	^t AA		35		40	ns	23
Column-address hold time (referenced to RAS#)	^t AR	48		53		ns	22
Column-address setup time	^t ASC	2		2		ns	21
Row-address setup time	^t ASR	5		5		ns	23
Column-address to WE# delay time	^t AWD	57		62		ns	21, 28
Access time from CAS#	^t CAC		20		25	ns	14, 23
Column-address hold time	^t CAH	15		20		ns	23
CAS# pulse width	^t CAS	15	10,000	20	10,000	ns	
CAS# hold time (CBR Refresh)	^t CHR	8		13		ns	4, 22
CAS# to output in Low-Z	^t CLZ	5		5		ns	21, 30
CAS# precharge time	^t CP	10		10		ns	15
Access time from CAS# precharge	^t CPA		40		45	ns	23
CAS# to RAS# precharge time	^t CRP	10		10		ns	23
CAS# hold time	^t CSH	58		68		ns	22
CAS# setup time (CBR Refresh)	^t CSR	7		7		ns	4, 21
CAS# to WE# delay time	^t CWD	42		47		ns	21, 28
Write command to CAS# lead time	^t CWL	15		20		ns	
Data-in hold time	^t DH	15		20		ns	23, 27
Data-in setup time	^t DS	-2		-2		ns	22, 27
Output disable	^t OD	3	15	3	20	ns	
Output enable	^t OE		15		20	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^t OEH	13		18		ns	22, 26
Output buffer turn-off delay	^t OFF	5	20	5	25	ns	19, 25, 33
OE# setup prior to RAS# during HIDDEN Refresh cycle	^t ORD	0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	35		40		ns	

FAST PAGE MODE

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 29) ($V_{CC} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
PDE# to valid presence-detect data	t^1PD		10		10	ns	32
PDE# inactive to presence-detects inactive	t^1PDOFF	2		2		ns	31
FAST-PAGE-MODE READ-WRITE cycle time	t^1PRWC	87		97		ns	21
Access time from RAS#	t^1RAC		60		70	ns	13
RAS# to column-address delay time	t^1RAD	13		13		ns	17, 24
Row-address hold time	t^1RAH	8		8		ns	22
RAS# pulse width	t^1RAS	60	10,000	70	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	t^1RASP	60	100,000	70	100,000	ns	
Random READ or WRITE cycle time	t^1RC	110		130		ns	
RAS# to CAS# delay time	t^1RCD	18		18		ns	16, 24
Read command hold time (referenced to CAS#)	t^1RCH	2		2		ns	18, 21
Read command setup time	t^1RCS	2		2		ns	21
Refresh period (2,048 cycles) (16MB)	t^1REF		32		32	ms	
Refresh period (4,096 cycles) (32MB and 64MB)	t^1REF		64		64	ms	
RAS# precharge time	t^1RP	40		50		ns	
RAS# to CAS# precharge time	t^1RPC	0		0		ns	
Read command hold time (referenced to RAS#)	t^1RRH	0		0		ns	18
RAS# hold time	t^1RSH	20		25		ns	23
READ WRITE cycle time	t^1RWC	155		185		ns	23
RAS# to WE# delay time	t^1RWD	87		97		ns	21, 28
Write command to RAS# lead time	t^1RWL	20		25		ns	23
Transition time (rise or fall)	t^1T	3	50	3	50	ns	
Write command hold time	t^1WCH	15		20		ns	23
Write command hold time (referenced to RAS#)	t^1WCR	43		53		ns	22
WE# command setup time	t^1WCS	2		2		ns	21, 28
Write command pulse width	t^1WP	10		15		ns	
WE# hold time (CBR Refresh)	t^1WRH	8		8		ns	22
WE# setup time (CBR Refresh)	t^1WRP	12		12		ns	21

EDO PAGE MODE
AC ELECTRICAL CHARACTERISTICS

 (Notes: 5, 6, 7, 8, 9, 12, 29) ($V_{CC} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-5		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	t_{AA}		30		35		40	ns	23
Column-address set-up to CAS# precharge	t_{ACH}	12		15		15		ns	
Column-address hold time (referenced to RAS#)	t_{AR}	36		43		48		ns	22
Column-address setup time	t_{ASC}	2		2		2		ns	21
Row-address setup time	t_{ASR}	5		5		5		ns	23
Column-address to WE# delay time	t_{AWD}	42		49		59		ns	21, 28
Access time from CAS#	t_{CAC}		18		20		25	ns	14, 23
Column-address hold time	t_{CAH}	13		15		17		ns	23
CAS# pulse width	t_{CAS}	8	10,000	10	10,000	12	10,000	ns	
CAS# hold time (CBR Refresh)	t_{CHR}	6		8		10		ns	4, 22
CAS# to output in Low-Z	t_{CLZ}	2		2		2		ns	21
Data output hold after next CAS# LOW	t_{COH}	5		5		5		ns	21
CAS# precharge time	t_{CP}	8		10		10		ns	15
Access time from CAS# precharge	t_{CPA}		33		40		45	ns	23
CAS# to RAS# precharge time	t_{CRP}	10		10		10		ns	23
CAS# hold time	t_{CSH}	36		43		48		ns	22
CAS# setup time (CBR Refresh)	t_{CSR}	7		7		7		ns	4, 21
CAS# to WE# delay time	t_{CWD}	30		37		42		ns	21, 28
Write command to CAS# lead time	t_{CWL}	8		10		15		ns	
Data-in hold time	t_{DH}	13		15		17		ns	23, 27
Data-in setup time	t_{DS}	-2		-2		-2		ns	22, 27
Output disable	t_{OD}	0	12	0	15	0	15	ns	
Output Enable	t_{OE}		12		15		20	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	t_{OEHL}	6		8		10		ns	22, 26
OE# HIGH hold from CAS# HIGH	t_{OEHC}	5		10		10		ns	26
OE# HIGH pulse width	t_{OEP}	5		5		5		ns	
OE# LOW to CAS# HIGH setup time	t_{OES}	4		5		5		ns	
Output buffer turn-off delay	t_{OFF}	2	17	2	20	2	20	ns	19, 25, 33

EDO PAGE MODE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 2, 3, 6, 9, 12, 29) ($V_{CC} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-5		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
OE# setup prior to RAS# during HIDDEN Refresh cycle	t_{ORD}	0		0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	t_{PC}	20		25		30		ns	
PDE# to valid presence-detect data	t_{PD}		10		10		10	ns	32
PDE# inactive to presence-detect inactive	t_{PDOFF}	2		2		2		ns	31
EDO-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	49		58		73		ns	21
Access time from RAS#	t_{RAC}		50		60		70	ns	13
RAS# to column-address delay time	t_{RAD}	7		10		10		ns	17, 22
Row-address hold time	t_{RAH}	7		8		8		ns	22
RAS# pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	t_{RASP}	50	125,000	60	125,000	70	125,000	ns	
Random READ or WRITE cycle time	t_{RC}	84		104		124		ns	
RAS# to CAS# delay time	t_{RCD}	9		12		12		ns	16, 24
Read command hold time (referenced to CAS#)	t_{RCH}	2		2		2		ns	18, 21
Read command setup time	t_{RCS}	2		2		2		ns	21
Refresh period (2,048 cycles) (16MB)	t_{REF}		32		32		32	ms	
Refresh period (4,096 cycles) (32MB and 64MB)	t_{REF}		64		64		64	ms	
RAS# precharge time	t_{RP}	30		40		50		ns	
RAS# to CAS# precharge time	t_{RPC}	5		5		5		ns	
Read command hold time (referenced to RAS#)	t_{RRH}	0		0		0		ns	18
RAS# hold time	t_{RSH}	18		20		20		ns	23
READ WRITE cycle time	t_{RWC}	121		145		175		ns	23
RAS# to WE# delay time	t_{RWD}	69		81		92		ns	21, 28
Write command to RAS# lead time	t_{RWL}	18		20		20		ns	23
Transition time (rise or fall)	t_T	2	50	2	50	2	50	ns	
Write command hold time	t_{WCH}	13		15		17		ns	23
Write command hold time (referenced to RAS#)	t_{WCR}	36		43		53		ns	22
WE# command setup time	t_{WCS}	2		2		2		ns	21, 28
Output disable delay from WE#	t_{WHZ}	2	17	2	20	2	20	ns	25
Write command pulse width	t_{WP}	5		5		5		ns	
WE# pulse to disable at CAS# HIGH	t_{WPZ}	10		10		12		ns	
WE# hold time (CBR Refresh)	t_{WRH}	6		8		8		ns	22
WE# setup time (CBR Refresh)	t_{WRP}	10		12		12		ns	21

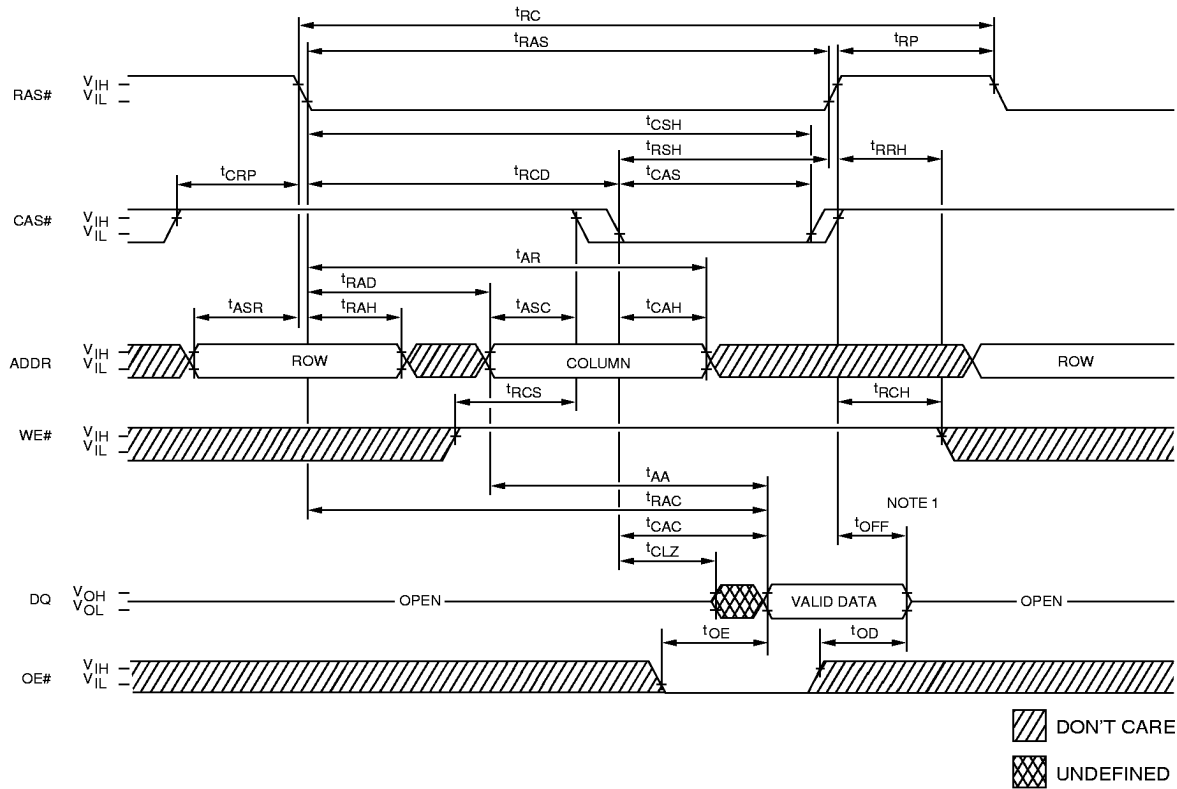
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.0V; f = 1 MHz.
3. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
6. An initial pause of 100μs is required after power-up followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH) before proper device operation is assured. The eight RAS# cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
7. AC characteristics assume t_T = 5ns for FPM and 2.5ns for EDO.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH}, data output is High-Z.
11. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
13. Requires that t_{AA} and t_{CAC} are not violated.
14. Requires that t_{AA} and t_{RAC} are not violated.
15. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for t_{CP}.
16. The t_{RCD} (MAX) limit is no longer specified. t_{RCD} (MAX) was specified as a reference point only. If t_{RCD} was greater than the specified t_{RCD} (MAX) limit, then access time was controlled exclusively by t_{CAC} (t_{RAC} [MIN] no longer applied). With or without the t_{RCD} (MAX) limit, t_{AA} and t_{CAC} must always be met.
17. The t_{RAD} (MAX) limit is no longer specified. t_{RAD} (MAX) was specified as a reference point only. If t_{RAD} was greater than the specified t_{RAD} (MAX) limit, then access time was controlled exclusively by t_{AA} (t_{RAC} and t_{CAC} no longer applied). With or without the t_{RAD} (MAX) limit, t_{AA}, t_{RAC} and t_{CAC} must always be met.
18. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
19. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
20. A HIDDEN Refresh may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
21. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
22. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
23. A +5ns timing skew from the DRAM to the module resulted from the addition of line drivers.
24. A -2ns (MIN) and a -5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A +2ns (MIN) and a +5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
26. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OE} met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS# remains LOW and OE# is taken back LOW after t_{OE} is met. If CAS# goes HIGH prior to OE# going back LOW, the DQs will remain open.
27. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
28. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters. t_{WCS} applies to EARLY WRITE cycles. t_{RWD}, t_{AWD} and t_{CWD} apply to READ-MODIFY-WRITE cycles. If t_{WCS} ≥ t_{WCS} (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If t_{WCS} < t_{WCS} (MIN) and t_{RWD} ≥ t_{RWD} (MIN), t_{AWD} ≥ t_{AWD} (MIN) and t_{CWD} ≥ t_{CWD} (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW results in a LATE WRITE (OE#-controlled) cycle. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not applicable in a LATE WRITE cycle.
29. Column address changed once each cycle.

NOTES (continued)

- 30. The 3ns minimum parameter guaranteed by design.
- 31. $t_{PD OFF MAX}$ is determined by the pull-up resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent DIMM position.
- 32. Measured with specified current load and 100pF.
- 33. For FAST PAGE MODE option, t_{OFF} is determined by the first RAS# or CAS# signal to transition HIGH. In comparison, t_{OFF} on an EDO option is determined by the latter of the RAS# and CAS# signal to transition HIGH.
- 34. Applies to both EDO and FAST PAGE MODEs.

READ CYCLE ³⁴



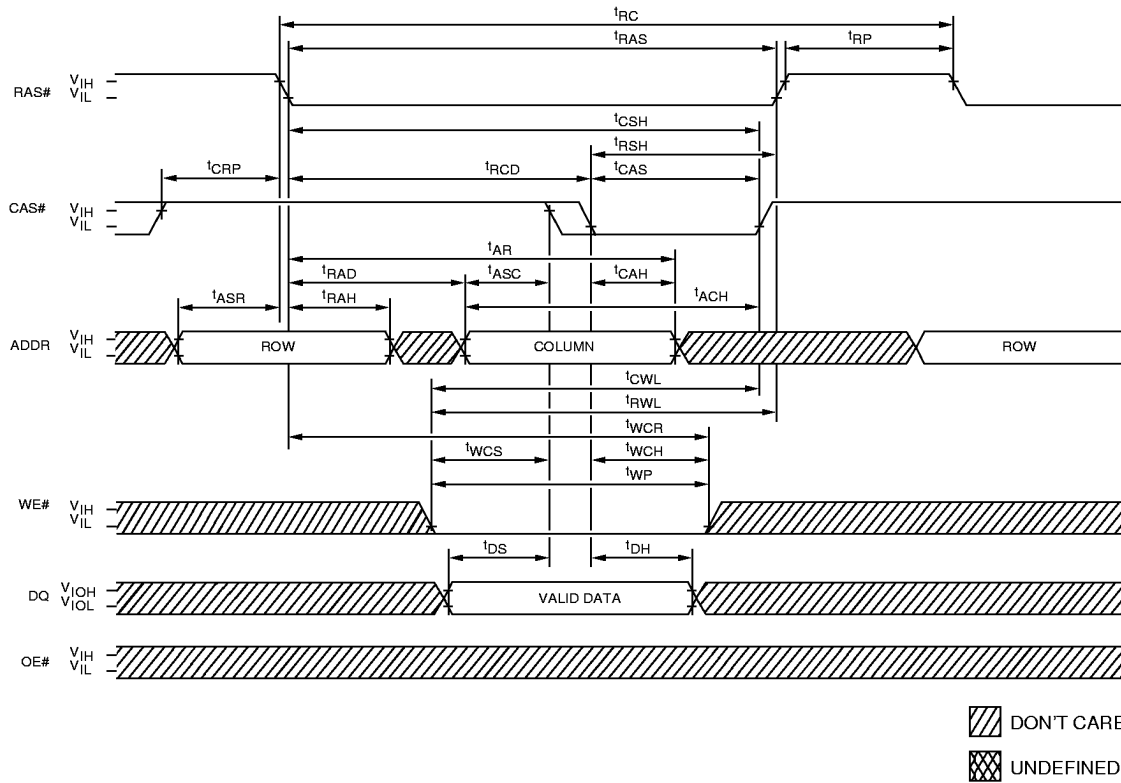
**FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS**

	-5*		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{AA}		30		35		40	ns
t _{ACH} (EDO)	12		15		15		ns
t _{AR} (EDO)	36		43		48		ns
t _{AR} (FPM)	—		48		53		ns
t _{ASC}	2		2		2		ns
t _{ASR}	5		5		5		ns
t _{CAC}		18		20		25	ns
t _{CAH} (EDO)	13		15		17		ns
t _{CAH} (FPM)	—		15		20		ns
t _{CAS} (EDO)	8	10,000	10	10,000	12	10,000	ns
t _{CAS} (FPM)	—	—	15	10,000	20	10,000	ns
t _{CLZ} (EDO)	2		2		2		ns
t _{CLZ} (FPM)	—		5		5		ns
t _{CRP}	10		10		10		ns
t _{CSH} (EDO)	36		43		48		ns
t _{CSH} (FPM)	—		58		68		ns
t _{OD} (EDO)	0	12	0	15	0	15	ns
t _{OD} (FPM)	—	—	3	15	3	20	ns

	-5*		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{OE}		12		15		20	ns
t _{OFF} (EDO)	2	17	2	20	2	20	ns
t _{OFF} (FPM)	—	—	5	20	5	25	ns
t _{RAC}		50		60		70	ns
t _{RAD} (EDO)	7		10		10		ns
t _{RAD} (FPM)	—		13		13		ns
t _{RAH}	7		8		8		ns
t _{RAS}	50	10,000	60	10,000	70	10,000	ns
t _{RC} (EDO)	84		104		124		ns
t _{RC} (FPM)	—		110		130		ns
t _{RCD} (EDO)	9		12		12		ns
t _{RCD} (FPM)	—		18		18		ns
t _{RCH}	2		2		2		ns
t _{RCS}	2		2		2		ns
t _{RP}	30		40		50		ns
t _{RRH}	0		0		0		ns
t _{RSH} (EDO)	18		20		20		ns
t _{RSH} (FPM)	—		20		25		ns

*EDO version only.

NOTE: 1. For EDO, t_{OFF} is referenced from rising edge of RAS# or CAS#, whichever occurs last. For FPM, t_{OFF} is referenced from rising edge of RAS# or CAS#, whichever occurs first.

EARLY WRITE CYCLE ³⁴

**FAST PAGE MODE AND EDO PAGE MODE
 TIMING PARAMETERS**

	-5*		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{ACH} (EDO)	12		15		15		ns
t _{AR} (FPM)	—		48		53		ns
t _{AR} (EDO)	36		43		48		ns
t _{ASC}	2		2		2		ns
t _{ASR}	5		5		5		ns
t _{CAH} (FPM)	—		15		20		ns
t _{CAH} (EDO)	13		15		17		ns
t _{CAS} (FPM)	—	—	15	10,000	20	10,000	ns
t _{CAS} (EDO)	8	10,000	10	10,000	12	10,000	ns
t _{CRP}	10		10		10		ns
t _{CSH} (FPM)	—		58		68		ns
t _{CSH} (EDO)	36		43		48		ns
t _{CWL} (FPM)	—		15		20		ns
t _{CWL} (EDO)	8		10		15		ns
t _{DH} (FPM)	—		15		20		ns
t _{DH} (EDO)	13		15		17		ns
t _{DS}	-2		-2		-2		ns
t _{RAD} (FPM)	—		13		13		ns

	-5*		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{RAD} (EDO)	7		10		10		ns
t _{RAH}	7		8		8		ns
t _{RAS}	50	10,000	60	10,000	70	10,000	ns
t _{RC} (FPM)	—		110		130		ns
t _{RC} (EDO)	84		104		124		ns
t _{RCD} (FPM)	—		18		18		ns
t _{RCD} (EDO)	9		12		12		ns
t _{RP}	30		40		50		ns
t _{RSH} (FPM)	—		20		25		ns
t _{RSH} (EDO)	18		20		20		ns
t _{RWL} (FPM)	—		20		25		ns
t _{RWL} (EDO)	18		20		20		ns
t _{WCH} (FPM)	—		15		20		ns
t _{WCH} (EDO)	13		15		17		ns
t _{WCR}	36		43		53		ns
t _{WCS}	2		2		2		ns
t _{WP} (FPM)	—		10		15		ns
t _{WP} (EDO)	5		5		5		ns

*EDO version only.

[illegible]

 DON'T CARE
 UNDEFINED

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
¹ AA		35		40	ns
¹ AR	48		53		ns
¹ ASC	2		2		ns
¹ ASR	5		5		ns
¹ CAC		20		25	ns
¹ CAH	15		20		ns
¹ CAS	15	10,000	20	10,000	ns
¹ CLZ	5		5		ns
¹ CP	10		10		ns
¹ CPA		40		45	ns
¹ CRP	10		10		ns
¹ CSH	58		68		ns
¹ OD	3	15	3	20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
¹ OE		15		20	ns
¹ OFF	5	20	5	25	ns
¹ PC	35		40		ns
¹ RAC		60		70	ns
¹ RAD	13		13		ns
¹ RAH	8		8		ns
¹ RASP	60	100,000	70	100,000	ns
¹ RCD	18		18		ns
¹ RCH	2		2		ns
¹ RCS	2		2		ns
¹ RP	40		50		ns
¹ RRH	0		0		ns
¹ RSH	20		25		ns

The diagram illustrates the timing relationships for a 2D DRAM array. It shows the signals RAS#, CAS#, ADDR, WE#, DQ, and OE# over time. The signals are divided into three main sections: Row Address Strobe (RAS), Column Address Strobe (CAS), and Data Output Strobe (OE). The timing parameters are defined as follows:

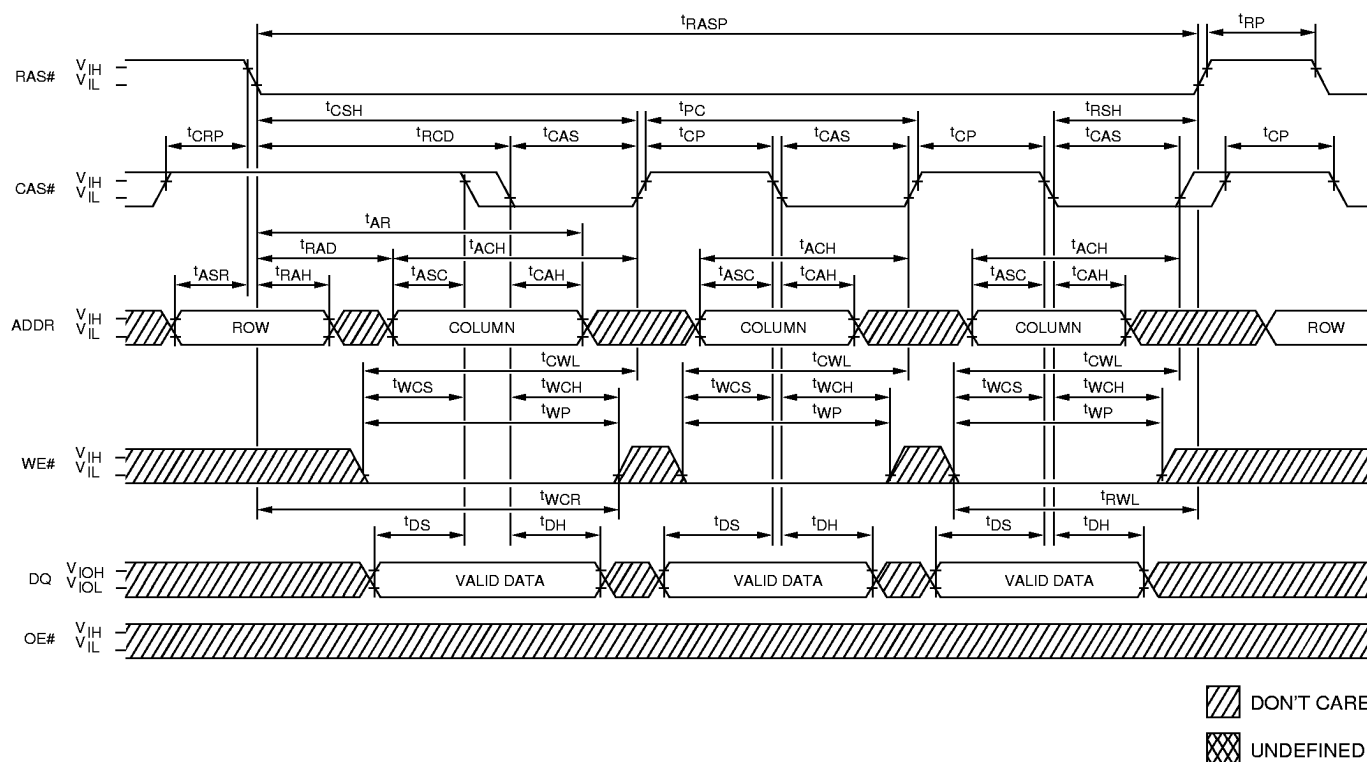
- t_{RASP} : RAS pulse width
- t_{CRP} : RAS to CAS delay
- t_{CSH} : CAS pulse width
- t_{RCD} : RAS to CAS delay
- t_{CAS} : CAS pulse width
- t_{PC} : Precharge time
- t_{CP} : CAS to Precharge delay
- t_{RSH} : RAS to Precharge delay
- t_{CASH} : CAS to Precharge delay
- t_{CP} : Precharge to CAS delay
- t_{RCH} : RAS to Precharge delay
- t_{RRH} : RAS to Precharge delay
- t_{AA} : Access time
- t_{RAC} : Read Access time
- t_{CAC} : Column Access time
- t_{CLZ} : Column Latency
- t_{COH} : Column Output Hold time
- t_{OEHC} : Output Enable Hold time
- t_{OE} : Output Enable pulse width
- t_{OD} : Output Delay
- t_{OES} : Output Enable Setup time
- t_{OEP} : Output Enable Pulse width
- t_{OFF} : Output Disable time
- t_{OD} : Output Delay
- t_{OE} : Output Enable pulse width
- t_{OES} : Output Enable Setup time
- t_{OEP} : Output Enable Pulse width

The diagram also shows the data output (DQ) signal, which is valid during the RAS and CAS pulses. The data output is divided into three sections: Row Address Strobe (RAS), Column Address Strobe (CAS), and Data Output Strobe (OE). The data output is valid during the RAS and CAS pulses. The data output is divided into three sections: Row Address Strobe (RAS), Column Address Strobe (CAS), and Data Output Strobe (OE). The data output is valid during the RAS and CAS pulses.

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
¹AA		30		35		40	ns
¹ACH	12		15		15		ns
¹AR	36		43		53		ns
¹ASC	2		2		2		ns
¹ASR	5		5		5		ns
¹CAC		18		20		25	ns
¹CAH	13		15		17		ns
¹CAS	8	10,000	10	10,000	12	10,000	ns
¹CLZ	2		2		2		ns
¹COH	5		5		5		ns
¹CP	8		10		10		ns
¹CPA		33		40		45	ns
¹CRP	10		10		10		ns
¹CSH	36		43		48		ns
¹OD	0	12	0	15	0	15	ns
¹OE		12		15		20	ns

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
'OEHC	5		10		10		ns
'OEP	5		5		5		ns
'OES	4		5		5		ns
'OFF	2	17	2	20	2	20	ns
'PC	20		25		30		ns
'RAC		50		60		70	ns
'RAD	7		10		10		ns
'RAH	7		8		8		ns
'RASP	50	125,000	60	125,000	70	125,000	ns
'RCD	9		12		12		ns
'RCH	2		2		2		ns
'RCS	2		2		2		ns
'RP	30		40		50		ns
'RRH	0		0		0		ns
'RSH	18		20		20		ns

FAST/EDO-PAGE-MODE EARLY-WRITE CYCLE



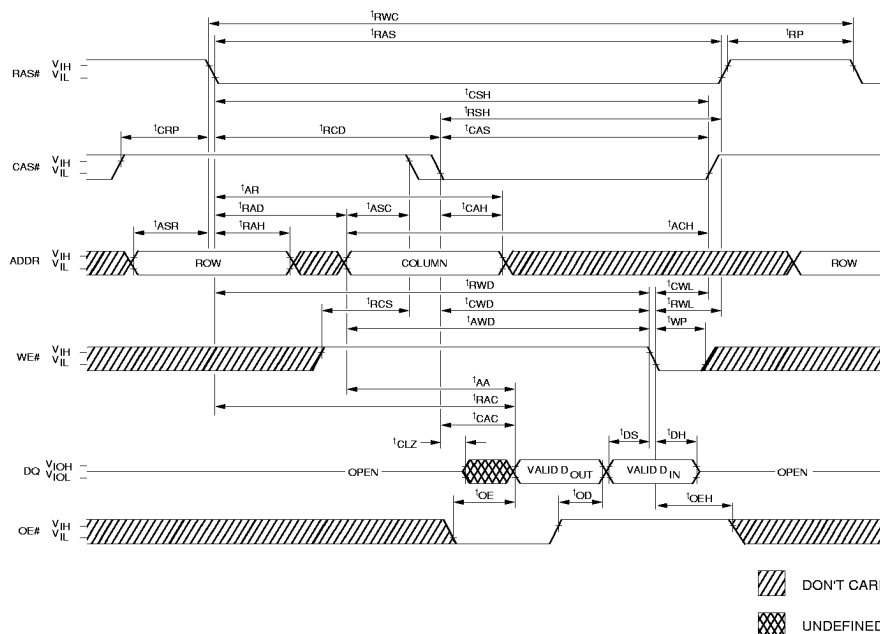
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-5*		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
†ACH (EDO)	12		15		15		ns
†AR (EDO)	36		43		48		ns
†AR (FPM)	—		48		53		ns
†ASC	2		2		2		ns
†ASR	5		5		5		ns
†CAH (EDO)	13		15		17		ns
†CAH (FPM)	—		15		20		ns
†CAS (EDO)	8	10,000	10	10,000	12	10,000	ns
†CAS (FPM)	—	—	15	10,000	20	10,000	ns
†CP	8		10		10		ns
†CRP	10		10		10		ns
†CSH (EDO)	36		43		48		ns
†CSH (FPM)	—		58		68		ns
†CWL (EDO)	8		10		15		ns
†CWL (FPM)	—		15		20		ns
†DH (EDO)	13		15		17		ns
†DH (FPM)	—		15		20		ns
†DS	-2		-2		-2		ns
†PC (EDO)	20		25		30		ns

	-5°		-6°		-7°		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
1PC (FPM)	—		35		40		ns
1RAD (EDO)	7		10		10		ns
1RAD (FPM)	—		13		13		ns
1RAH	7		8		8		ns
1RASP (EDO)	50	125,000	60	125,000	70	125,000	ns
1RASP (FPM)	—	—	60	100,000	70	100,000	ns
1RCD (EDO)	9		12		12		ns
1RCD (FPM)	—		18		18		ns
1RP	30		40		50		ns
1RSH (EDO)	18		20		20		ns
1RSH (FPM)	—		20		25		ns
1RWL (EDO)	18		20		20		ns
1RWL (FPM)	—		20		25		ns
1WCH (EDO)	13		15		17		ns
1WCH (FPM)	—		15		20		ns
1WCR	36		43		53		ns
1WCS	2		2		2		ns
1WP (EDO)	5		5		5		ns
1WP (FPM)	—		10		15		ns

*EDO version only.

READ WRITE CYCLE ³⁴ (LATE WRITE and READ-MODIFY-WRITE cycles)



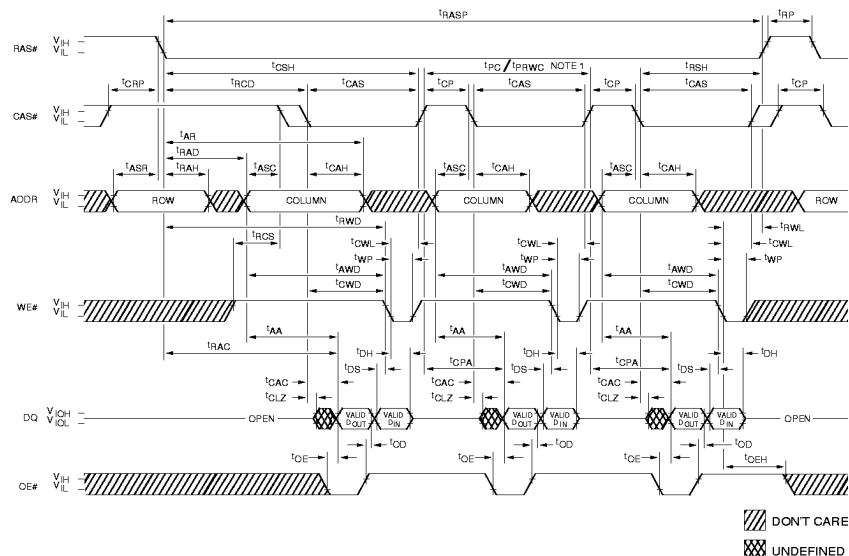
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-5*		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		30		35		40	ns
tACH (EDO)	12		15		15		ns
tAR	36		43		53		ns
tASC	2		2		2		ns
tASR	5		5		5		ns
tAWD (EDO)	42		49		59		ns
tAWD (FPM)	—		57		62		ns
tCAC		18		20		25	ns
tCAH (EDO)	13		15		17		ns
tCAH (FPM)	—		15		20		ns
tCAS (EDO)	8	10,000	10	10,000	12	10,000	ns
tCAS (FPM)	—	—	15	10,000	20	10,000	ns
tCLZ (EDO)	2		2		2		ns
tCLZ (FPM)	—		5		5		ns
tCRP	10		10		10		ns
tCSH (EDO)	36		43		48		ns
tCSH (FPM)	—		58		68		ns
tCWD (EDO)	30		37		42		ns
tCWD (FPM)	—		42		47		ns
tCWL (EDO)	8		10		15		ns
tCWL (FPM)	—		15		20		ns
tDH (EDO)	13		15		17		ns
tDH (FPM)	—		15		20		ns
tDS	-2		-2		-2		ns

	-5*		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tOD (EDO)	0	12	0	15	0	15	ns
tOD (FPM)	—	—	3	15	3	20	ns
tOE		12		15		20	ns
tOEH (EDO)	6		8		10		ns
tOEH (FPM)	—		13		18		ns
tRAC		50		60		70	ns
tRAD (EDO)	7		10		10		ns
tRAD (FPM)	—		13		13		ns
tRAH	7		8		8		ns
tRAS	50	10,000	60	10,000	70	10,000	ns
tRCD (EDO)	9		12		12		ns
tRCD (FPM)	—		18		18		ns
tRCS	2		2		2		ns
tRP	30		40		50		ns
tRSH (EDO)	18		20		20		ns
tRSH (FPM)	—		20		25		ns
tRWC (EDO)	121		145		175		ns
tRWC (FPM)	—		155		185		ns
tRWD (EDO)	69		81		92		ns
tRWD (FPM)	—		87		97		ns
tRWL (EDO)	18		20		20		ns
tRWL (FPM)	—		20		25		ns
tWP (EDO)	5		5		5		ns
tWP (FPM)	—		10		15		ns

*EDO version only.

FAST/EDO PAGE MODE-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE cycles)



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

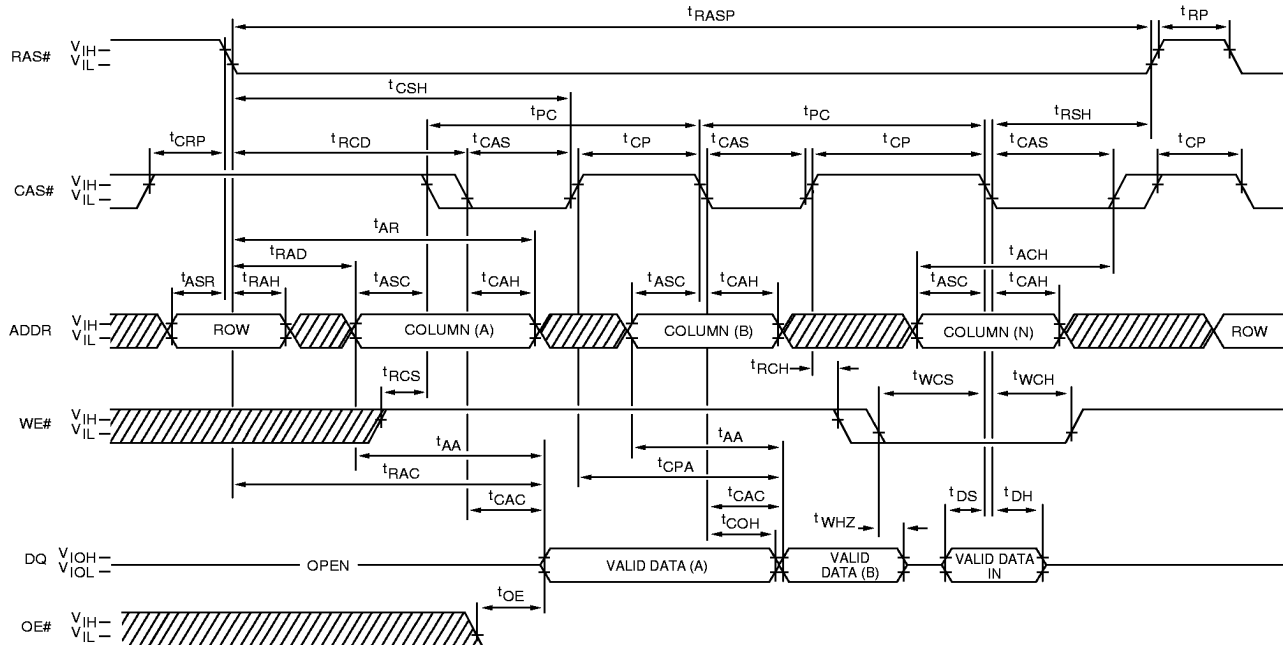
	-5°		-6°		-7°		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
1AA		30		35		40	ns
1AR (EDO)	36		43		48		ns
1AR (FPM)	—		48		53		ns
1ASC	2		2		2		ns
1ASR	5		5		5		ns
1AWD (EDO)	42		49		59		ns
1AWD (FPM)	—		57		62		ns
1CAC		18		20		25	ns
1CAH (EDO)	13		15		17		ns
1CAH (FPM)	—		15		20		ns
1CAS (EDO)	8	10,000	10	10,000	12	10,000	ns
1CAS (FPM)	—	—	15	10,000	20	10,000	ns
1CLZ (EDO)	2		2		2		ns
1CLZ (FPM)	—		5		5		ns
1CP	8		10		10		ns
1CPA		33		40		45	ns
1CRP	10		10		10		ns
1CSH (EDO)	36		43		48		ns
1CSH (FPM)	—		58		68		ns
1CWD (EDO)	30		37		42		ns
1CWD (FPM)	—		42		47		ns
1CWL (EDO)	8		10		15		ns
1CWL (FPM)	—		15		20		ns
1DH (EDO)	13		15		17		ns
1DH (FPM)	—		15		20		ns
1DS	-2		-2		-2		ns
1OD (EDO)	0	12	0	15	0	15	ns

	-5°		-6°		-7°		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
1°OD (FPM)	—	—	3	15	3	20	ns
1°OE		12		15		20	ns
1°OEH (EDO)	6		8		10		ns
1°OEH (FPM)	—		13		18		ns
1°PC (EDO)	20		25		30		ns
1°PC (FPM)	—		35		40		ns
1°PRWC (EDO)	49		58		73		ns
1°PRWC (FPM)	—		87		97		ns
1°RAC		50		60		70	ns
1°RAD (EDO)	7		10		10		ns
1°RAD (FPM)	—		13		13		ns
1°RAH	7		8		8		ns
1°RASP (EDO)	50	125,000	60	125,000	70	125,000	ns
1°RASP (FPM)	—	—	60	100,000	70	100,000	ns
1°RCD (EDO)	9		12		12		ns
1°RCD (FPM)	—		18		18		ns
1°RCS	2		2		2		ns
1°RP	30		40		50		ns
1°RSH (EDO)	18		20		20		ns
1°RSH (FPM)	—		20		25		ns
1°RWD (EDO)	69		81		92		ns
1°RWD (FPM)	—		87		97		ns
1°RWL (EDO)	18		20		20		ns
1°RWL (FPM)	—		20		25		ns
1°WP (EDO)	5		5		5		ns
1°WP (FPM)	—		10		15		ns

NOTE: 1. ^tPC is for LATE WRITE cycles only.

*EDO version only.

**EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)**



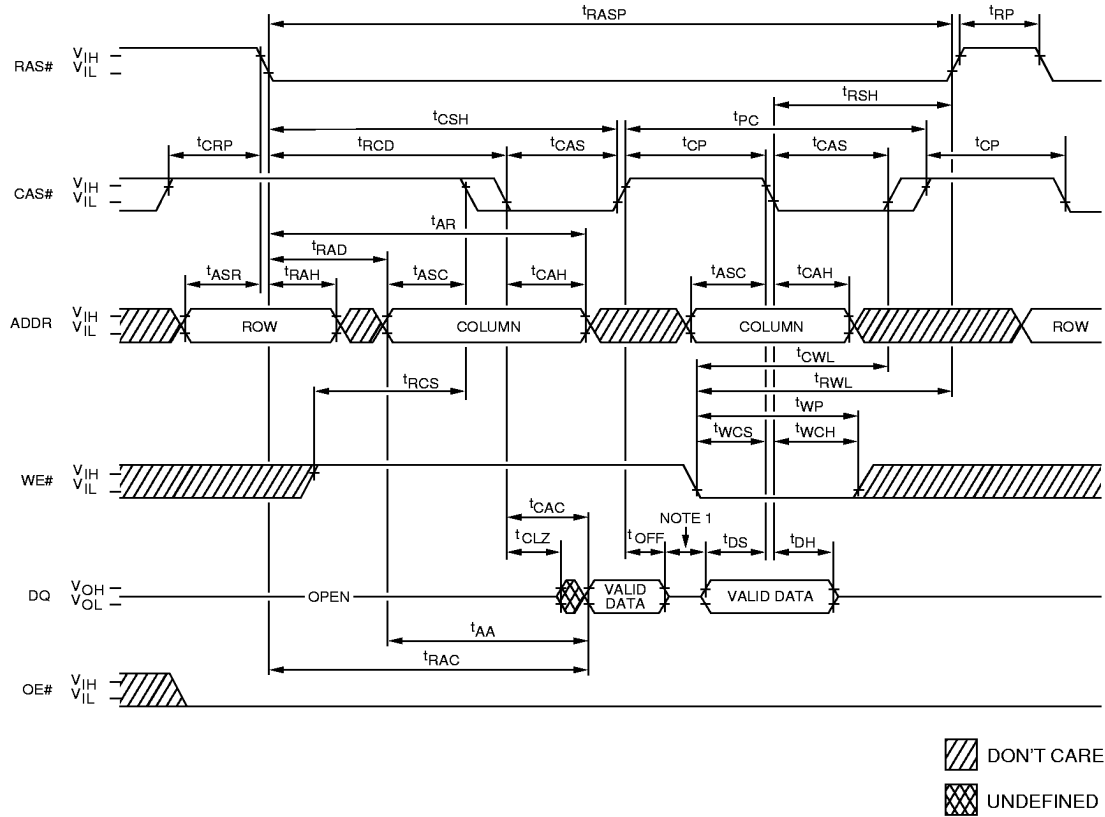
DON'T CARE
 UNDEFINED

**EDO PAGE MODE
TIMING PARAMETERS**

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{AA}		30		35		40	ns
t _{ACH}	12		15		15		ns
t _{AR}	36		43		48		ns
t _{ASC}	2		2		2		ns
t _{ASR}	5		5		5		ns
t _{CAC}		18		20		25	ns
t _{CAH}	13		15		17		ns
t _{CAS}	8	10,000	10	10,000	12	10,000	ns
t _{COH}	5		5		5		ns
t _{CP}	8		10		10		ns
t _{CPA}		33		40		45	ns
t _{CRP}	10		10		10		ns
t _{CSH}	36		43		48		ns
t _{DH}	13		15		17		ns
t _{DS}	-2		-2		-2		ns

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{OE}		12		15		20	ns
t _{PC}	20		25		30		ns
t _{RAC}		50		60		70	ns
t _{RAD}	7		10		10		ns
t _{RAH}	7		8		8		ns
t _{RASP}	50	125,000	60	125,000	70	125,000	ns
t _{RCD}	9		12		12		ns
t _{RCH}	2		2		2		ns
t _{RCS}	2		2		2		ns
t _{RP}	30		40		50		ns
t _{RSH}	18		20		20		ns
t _{WCH}	13		15		17		ns
t _{WCS}	2		2		2		ns
t _{WHZ}	2	17	2	20	2	20	ns

**FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)**



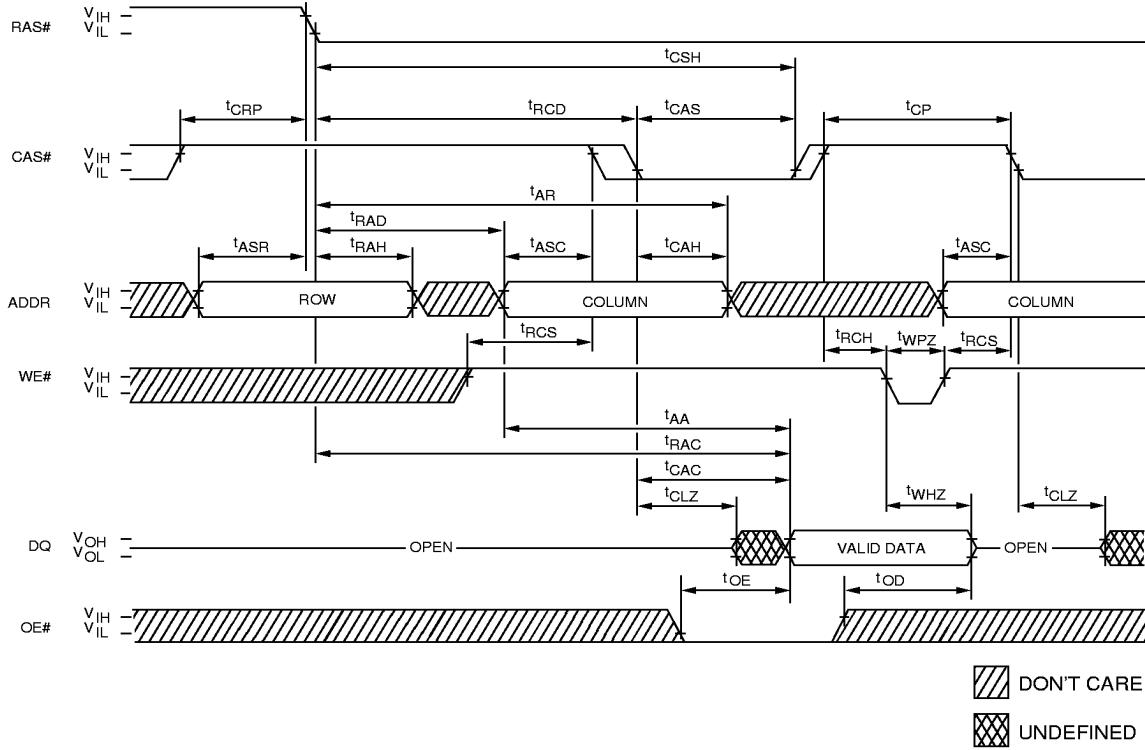
**FAST PAGE MODE
TIMING PARAMETERS**

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
t _{AA}		35		40	ns
t _{AR}	48		53		ns
t _{ASC}	2		2		ns
t _{ASR}	5		5		ns
t _{CAC}		20		25	ns
t _{CAH}	15		20		ns
t _{CAS}	15	10,000	20	10,000	ns
t _{CLZ}	5		5		ns
t _{CP}	10		10		ns
t _{CRP}	10		10		ns
t _{CSH}	58		68		ns
t _{CWL}	15		20		ns
t _{DH}	15		20		ns
t _{DS}	-2		-2		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
t _{OFF}	5	20	5	25	ns
t _{PC}	35		40		ns
t _{RAC}		60		70	ns
t _{RAD}	13		13		ns
t _{RAH}	8		8		ns
t _{RASP}	60	100,000	70	100,000	ns
t _{RCD}	18		18		ns
t _{RCS}	2		2		ns
t _{RP}	40		50		ns
t _{RSH}	20		25		ns
t _{RWL}	20		25		ns
t _{WCH}	15		20		ns
t _{WCS}	2		2		ns
t _{WP}	10		15		ns

NOTE: 1. Do not drive data prior to tristate.

EDO READ CYCLE
(with WE#-controlled disable)

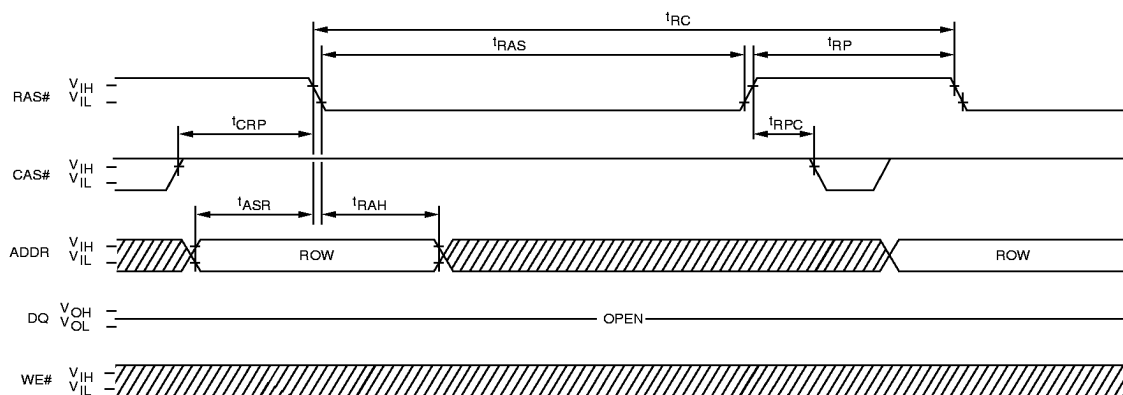


**EDO PAGE MODE
TIMING PARAMETERS**

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{AA}		30		35		40	ns
t _{AR}	36		43		48		ns
t _{ASC}	2		2		2		ns
t _{ASR}	5		5		5		ns
t _{CAC}		18		20		25	ns
t _{CAH}	13		15		17		ns
t _{CAS}	8	10,000	10	10,000	12	10,000	ns
t _{CLZ}	2		2		2		ns
t _{CP}	8		10		10		ns
t _{CRP}	10		10		10		ns
t _{CSH}	36		43		48		ns

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{OD}	0	12	0	15	0	15	ns
t _{OE}		12		15		20	ns
t _{RAC}		50		60		70	ns
t _{RAD}	7		10		10	30	ns
t _{RAH}	7		8		8		ns
t _{RCD}	9		12		12	45	ns
t _{RCH}	2		2		2		ns
t _{RCS}	2		2		2		ns
t _{WHZ}	2	17	2	20	2	20	ns
t _{WPZ}	10		10		12		ns

RAS#-ONLY REFRESH CYCLE ³⁴



DON'T CARE
 UNDEFINED

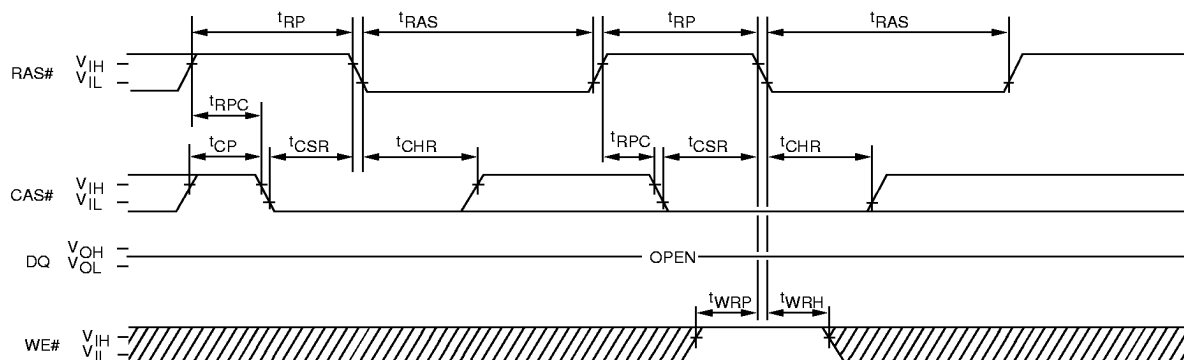
**FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS**

	-5*		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{ASR}	5		5		5		ns
t _{CRP}	10		10		10		ns
t _{CSR}	7		7		7		ns
t _{RAH}	7		8		8		ns
t _{RAS}	50	10,000	60	10,000	70	10,000	ns

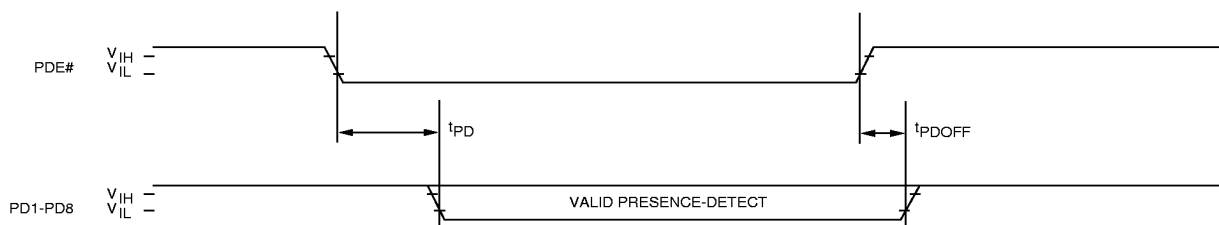
	-5*		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{RC} (FPM)	—		110		130		ns
t _{RC} (EDO)	84		104		124		ns
t _{RP}	30		40		50		ns
t _{RPC} (FPM)	—		0		0		ns
t _{RPC} (EDO)	5		5		5		ns

*EDO version only.

CBR REFRESH CYCLE ³⁴ (Addresses, OE# = DON'T CARE)



PRESENCE-DETECT READ CYCLE ³⁴



DON'T CARE
 UNDEFINED

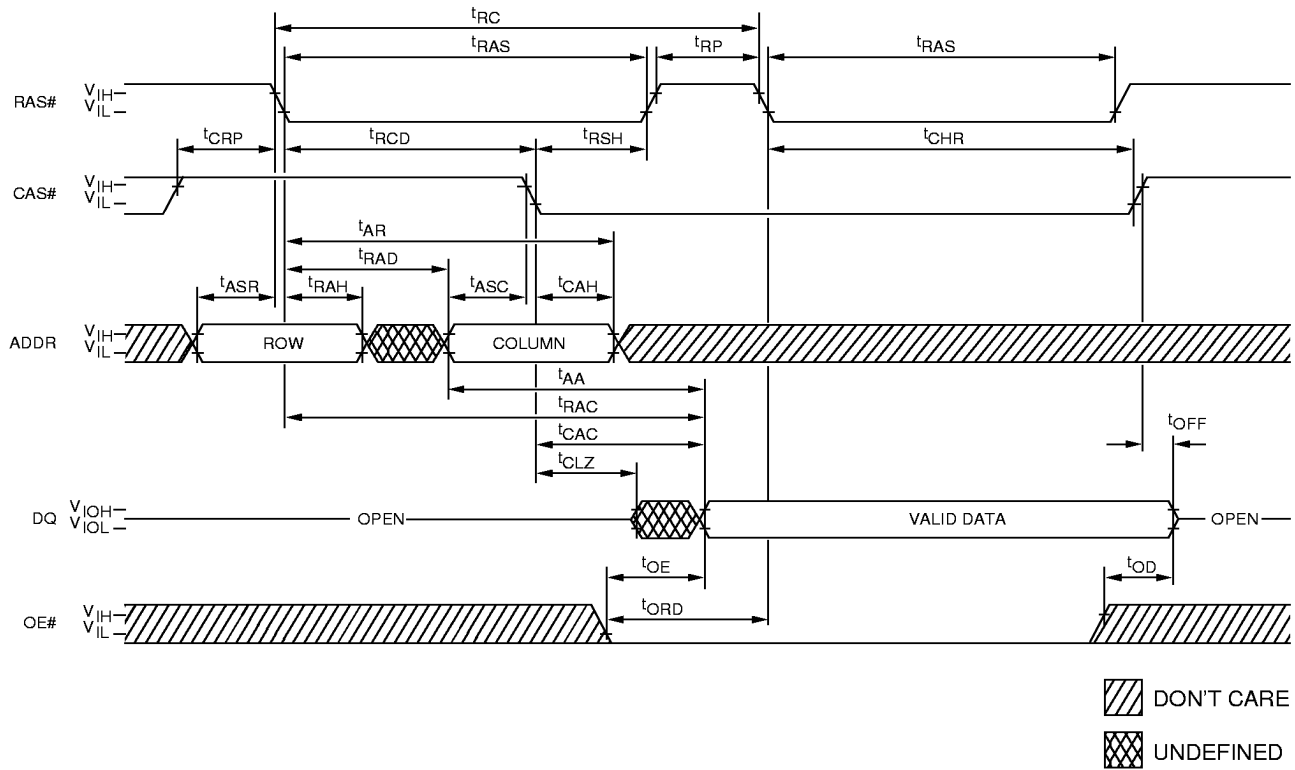
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-5*		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{CHR} (FPM)	—		8		13		ns
t _{CHR} (EDO)	6		8		10		ns
t _{CP}	8		10		10		ns
t _{CSR}	7		7		7		ns
t _{PD}		10		10		10	ns
t _{PDOFF}	2		2		2		ns

	-5*		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{RAS}	50	10,000	60	10,000	70	10,000	ns
t _{RP}	30		40		50		ns
t _{RPC} (FPM)	—		0		0		ns
t _{RPC} (EDO)	5		5		5		ns
t _{WRH}	6		8		8		ns
t _{WRP}	10		12		12		ns

*EDO version only.

NOTE: 1. PD pins must be pulled HIGH at next level of assembly.

HIDDEN REFRESH CYCLE 20, 34
 (WE# = HIGH; OE# = LOW)

**FAST PAGE MODE AND EDO PAGE MODE
 TIMING PARAMETERS**

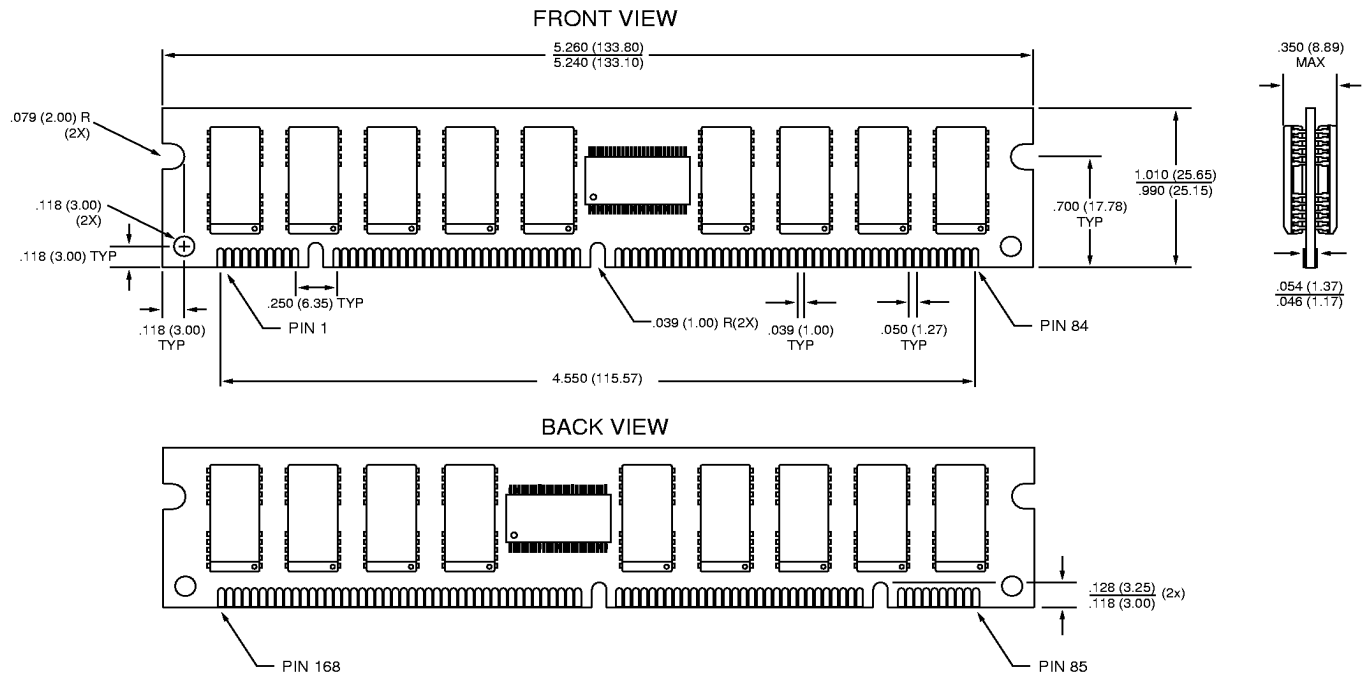
	-5*		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{AA}		30		35		40	ns
t _{AR} (FPM)	—		48		53		ns
t _{AR} (EDO)	36		43		48		ns
t _{ASC}	2		2		2		ns
t _{ASR}	5		5		5		ns
t _{CAC}		18		20		25	ns
t _{CAH} (FPM)	—		15		20		ns
t _{CAH} (EDO)	13		15		17		ns
t _{CHR} (FPM)	—		8		13		ns
t _{CHR} (EDO)	6		8		10		ns
t _{CLZ} (FPM)	—		5		5		ns
t _{CLZ} (EDO)	2		2		2		ns
t _{CRP}	10		10		10		ns
t _{OD} (FPM)	—	—	3	15	3	20	ns
t _{OD} (EDO)	0	12	0	15	0	15	ns

	-5*		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{OE}		12		15		20	ns
t _{ORD}	0		0		0		ns
t _{OFF} (FPM)	—	—	5	20	5	25	ns
t _{OFF} (EDO)	2	17	2	20	2	20	ns
t _{RAC}		50		60		70	ns
t _{RAD} (FPM)	—		13		13		ns
t _{RAD} (EDO)	7		10		10		ns
t _{RAH}	7		8		8		ns
t _{RAS}	50	10,000	60	10,000	70	10,000	ns
t _{RCD} (FPM)	—		18		18		ns
t _{RCD} (EDO)	9		12		12		ns
t _{RP}	30		40		50		ns
t _{RSH} (FPM)	—		20		25		ns
t _{RSH} (EDO)	18		20		20		ns

*EDO version only

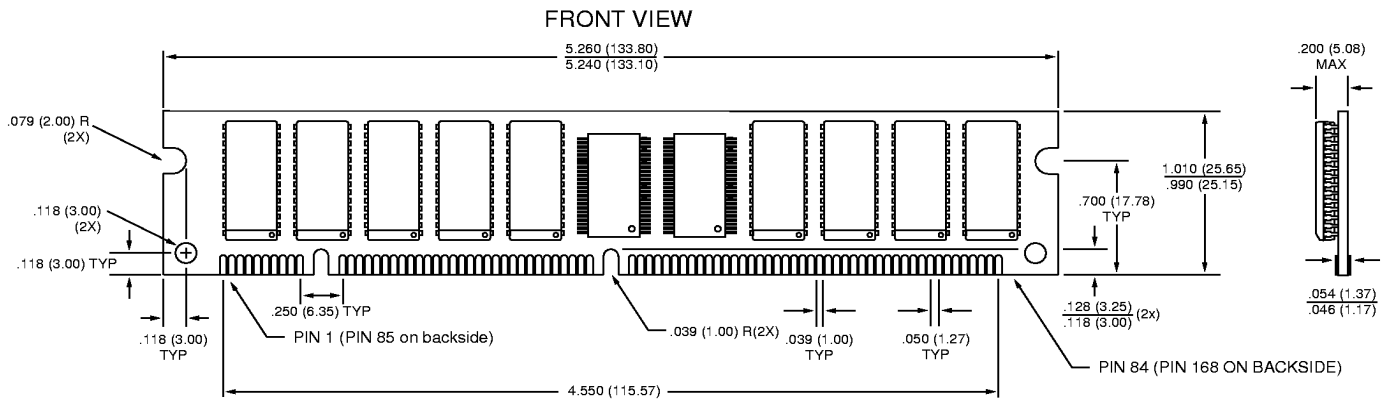
168-PIN DIMM

DE-7



168-PIN DIMM

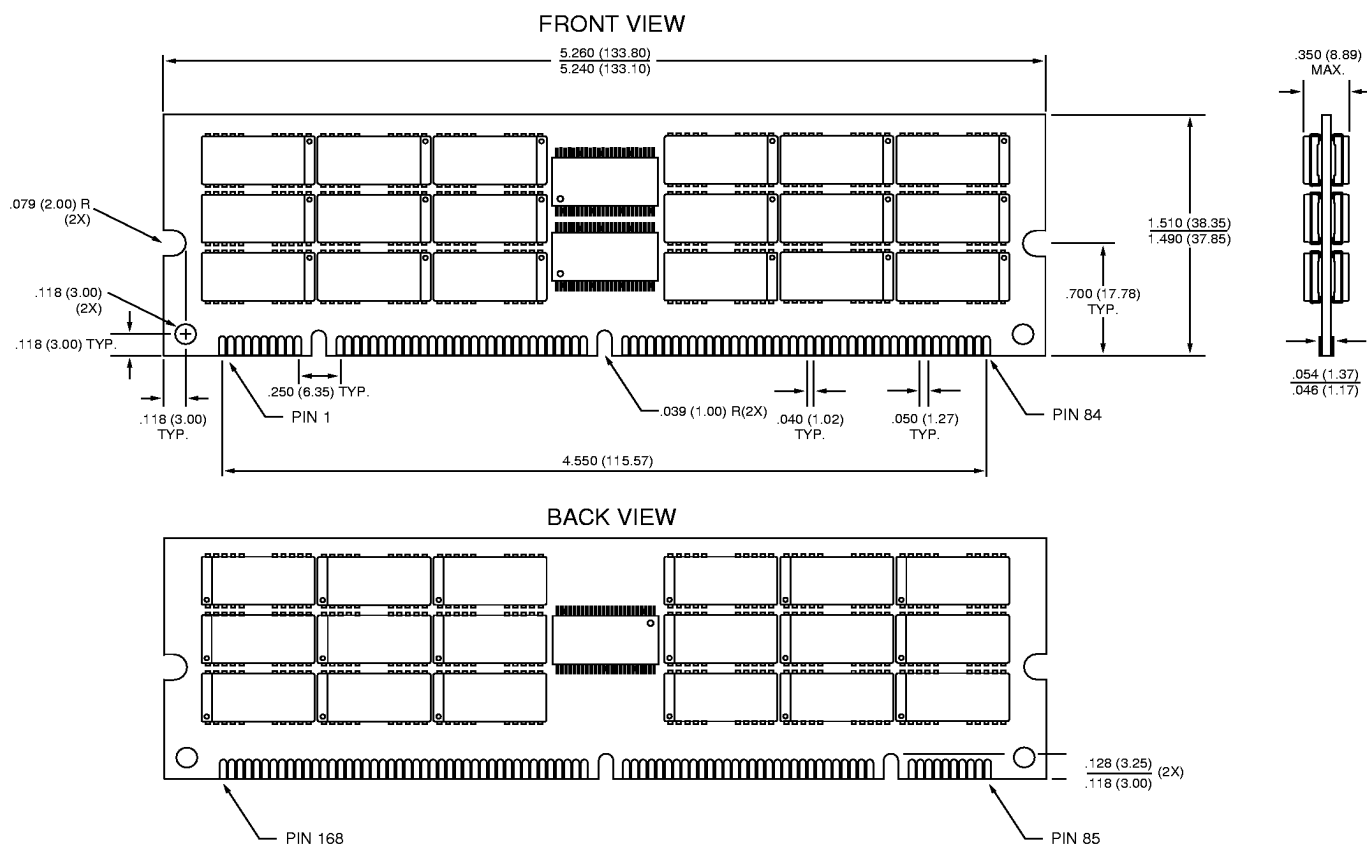
DE-8



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

168-PIN DIMM

DE-18



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.