PRELIMINARY PRODUCT SPECIFICATIONS

SHARP®

Integrated Circuits Group

LH5164AT-80L

64K SRAM

(Model No.: LH516AZE)

Spec No.: MS-J08905

Issue Date: September 20, 1996

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● When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliances
- Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-sale operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.

- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

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Contents

1. Decription

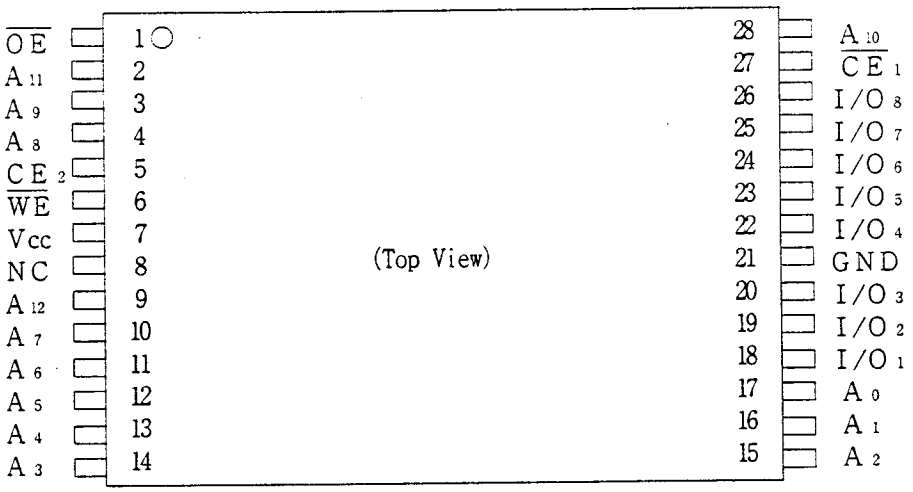
The LH5164AT-80L is a static RAM organized as 8,192×8 bit with provides low-power standby mode.
It is fabricated using silicon-gate CMOS process technology.

Features

○Access Time	· · · ·	80 ns (Max.)
○Operating current	· · · ·	55 mA (Max.)
	· · · ·	10 mA (Max. t_{RC}, t_{WC} = 1 μs)
○Standby current	· · · ·	1.0 μA (Max.)
○Data retention current	· · · ·	0.2 μA (Max. V_{CCDR} = 3V, Ta = 25℃)
○Single power supply	· · · ·	5V±10%
○Operating temperature	· · · ·	−10℃to +70℃

○Fully static operation
○Three-state output
○Not designed or rated as radiation hardened
○28 pin TSOP (TSOP28-P-0813) plastic package
○P-type bulk silicon

2. Pin Configuration



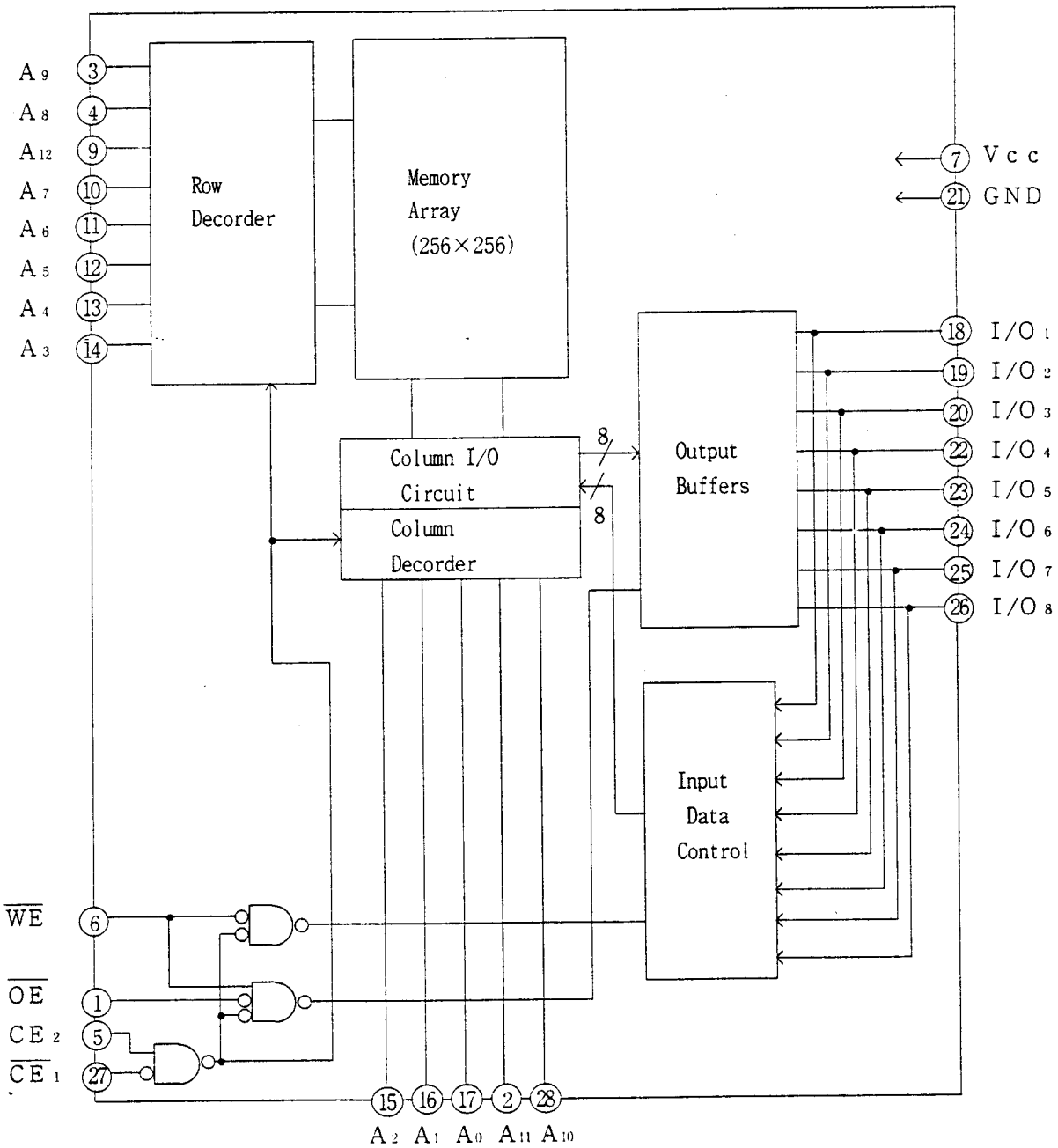
Pin Name	Function
A_0 to A_{12}	Address inputs
$\overline{CE}_1$/CE_2	Chip enable
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
I/O_1 to I/O_8	Data inputs/outputs
Vcc	Power supply
GND	Ground
NC	Non connection

3. Truth Table

$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	Mode	I/O_1 to I/O_8	Supply current
H	*	*	*	Standby	High impedance	Standby (I_{SB})
*	L	*	*	Standby	High impedance	Standby (I_{SB})
L	H	L	*	Write	Data input	Active (I_{CC})
L	H	H	L	Read	Data output	Active (I_{CC})
L	H	H	H	Read	High impedance	Active (I_{CC})

(*=Don't Care, L=Low, H=High)

4. Block Diagram



5. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage (*1)	V_{CC}	−0.3 to +7.0	V
Input voltage (*1)	V_{IN}	−0.3 (*2) to Vcc+0.3	V
Operating temperature	T_{opr}	−10 to +70	℃
Storage temperature	T_{stg}	−65 to +150	℃

Note) *1. The maximum applicable voltage on any pin with respect to GND.
*2. Undershoot of −3.0V is allowed width of pluse bellow 50ns.

6. Recommended DC Operating Conditions

(Ta= −10℃to +70℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		Vcc+0.3	V
	V_{IL}	−0.3 (*3)		0.8	V

Note) *3. Undershoot of −3.0V is allowed width of pluse below 50ns.

7. DC Electrical Characteristics

(Ta= −10℃to +70℃, Vcc=5V±10%)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input leakage current	I_{LI}	V_{IN}=0V to V_{CC}		−1.0		1.0	μA
Output leakage current	I_{LO}	$\overline{CE_1}$=V_{IH} or CE_2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=0V to V_{CC}		−1.0		1.0	μA
Operating supply current	I_{CC}	$\overline{CE_1}$=V_{IL}, V_{IN}=V_{IL} or V_{IH} CE_2=V_{IH}, $I_{I/O}$=0mA	t_{CYCLE} = 80ns			55	mA
	I_{CC1}	$\overline{CE_1}$=0.2V, V_{IN}=0.2V or V_{CC}−0.2V CE_2=V_{CC}−0.2V, $I_{I/O}$=0mA	t_{CYCLE} =1.0μs			10	mA
Standby current	I_{SB}	$\overline{CE_1}$, CE_2≧V_{CC}−0.2V or CE_2≦0.2V				1.0	μA
	I_{SB1}	$\overline{CE_1}$=V_{IH} or CE_2=V_{IL}				5	mA
Output voltage	V_{OL}	I_{OL}= 2.1mA				0.4	V
	V_{OH}	I_{OH}=−1.0mA		2.4			V

8. AC Eiectrical Characteristics

AC Test Conditions

Input pulse level	0.6V to 2.4V
Input rise and fall time	10ns
Input and Output timing Ref. level	1.5V
Output load	1TTL+C_L (100pF) (*4)

Note) *4. Including scope and jig capacitance.

Read cycle (Ta=−10℃to+70 ℃, Vcc=5V±10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Read cycle time	t_{RC}	80			ns
Address access time	t_{AA}			80	ns
$\overline{CE_1}$ access time	t_{ACE1}			80	ns
CE_2 access time	t_{ACE2}			80	ns
Output enable to output valid	t_{OE}			40	ns
Output hold from address change	t_{OH}	10			ns
$\overline{CE_1}$ Low to output active	t_{LZ1}	10			ns
CE_2 High to output active	t_{LZ2}	10			ns
$\overline{OE}$ Low to output active	t_{OLZ}	5			ns
$\overline{CE_1}$ High to output in High impedance	t_{HZ1}	0		30	ns
CE_2 Low to output in High impedance	t_{HZ2}	0		30	ns
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0		20	ns

Write cycle (Ta=−10℃to+70 ℃, Vcc=5V±10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Write cycle time	t_{WC}	80			ns
$\overline{CE_1}$ Low to end of write	t_{CW1}	70			ns
CE_2 High to end of write	t_{CW2}	70			ns
Address valid to end of write	t_{AW}	70			ns
Address setup time	t_{AS}	0			ns
Write pluse width	t_{WP}	60			ns
Write recovery time	t_{WR}	0			ns
Input data setup time	t_{DW}	40			ns
Input data hold time	t_{DH}	0			ns
$\overline{WE}$ High to output active	t_{OW}	10			ns
$\overline{WE}$ Low to output in High impedance	t_{WZ}	0		30	ns
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0		20	ns

9. Data Retention Characteristics

(Ta=−10℃ to+70℃)

Paramenter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Data Retention supply voltage	V_{CCDR}	$CE_2 \leqq 0.2$ V or $\overline{CE}_1 \geqq V_{CCDR}-0.2$ V (*5)		2.0		5.5	V
Data Retention supply current	I_{CCDR}	$V_{CCDR}=3$ V	Ta=25℃			0.2	μA
		$CE_2 \leqq 0.2$ or	Ta=40℃			0.4	μA
		$\overline{CE}_1 \geqq V_{CCDR}-0.2$ V (*5)				0.6	μA
Chip enable setup time	t_{CDR}			0			ns
Chip enable hold time	t_R			(*6) t_{RC}			ns

Note) *5. $CE_2 \geqq V_{CCDR}-0.2$ V or $CE_2 \leqq 0.2$ V
*6. Read Cycle

10. Pin Capacitance

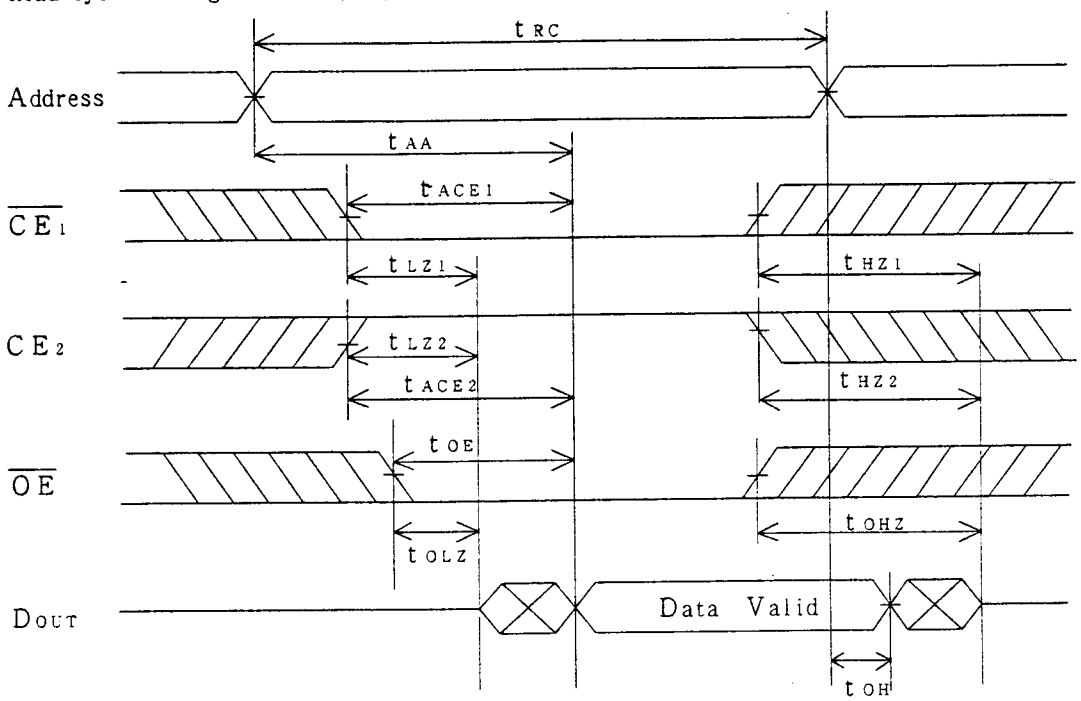
(Ta=25℃, f=1MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input capacitance	C_{IN}	$V_{IN}=0$ V			7	pF	*7
I/O capacitance	$C_{I/O}$	$V_{I/O}=0$ V			10	pF	*7

Note) *7. This parameter is sampled and not production tested.

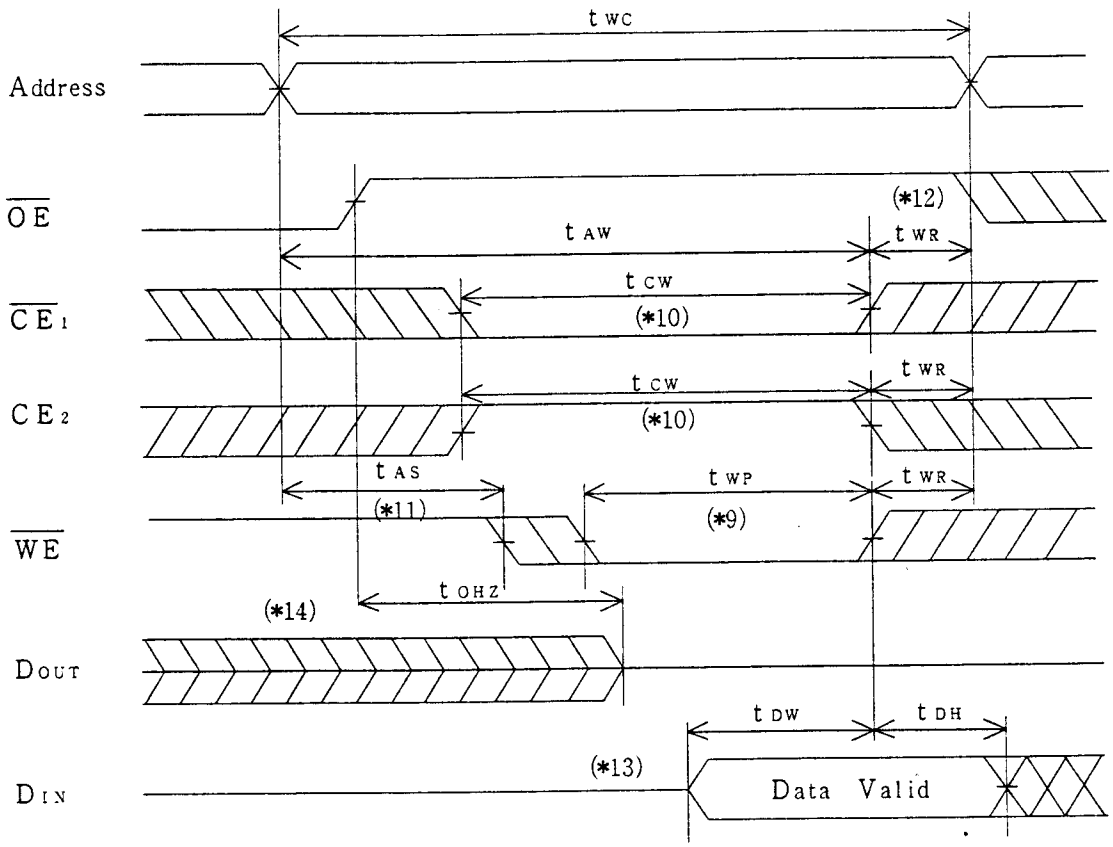
11. Timing Chart

Read cycle timing chart— (*8)

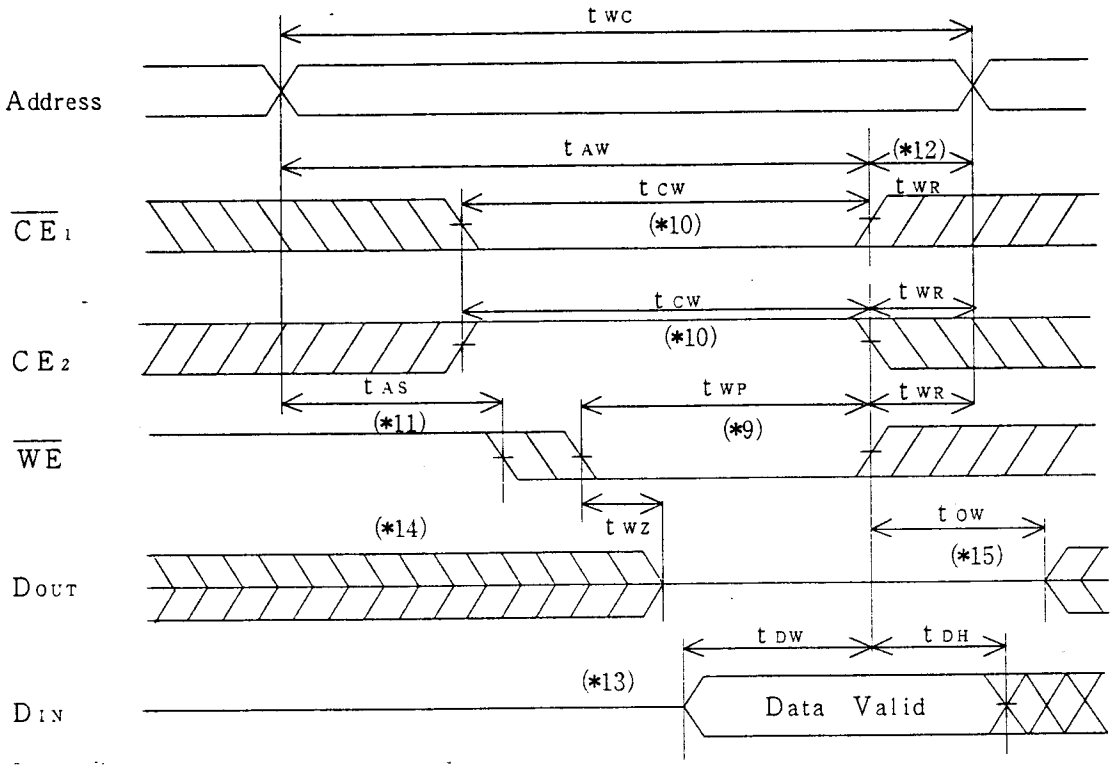


Note) *8. $\overline{WE}$ is high for Read cycle.

Write cycle timing chart— ($\overline{OE}$ Controlled)



Write cycle timing chart— ($\overline{OE}$ Low fixed)



Note) * 9. A write occurs during the overlap of a low $\overline{CE_1}$, a high CE_2 and a low $\overline{WE}$.
A write begins at the latest transition among $\overline{CE_1}$ going low, CE_2 going high and $\overline{WE}$ going low.
A write ends at the earliest transition among $\overline{CE_1}$ going high, CE_2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

* 10. t_{CW} is measured from the later of $\overline{CE_1}$ going low or CE_2 going high to the end of write.

* 11. t_{AS} is measured from the address valid to the beginning of write.

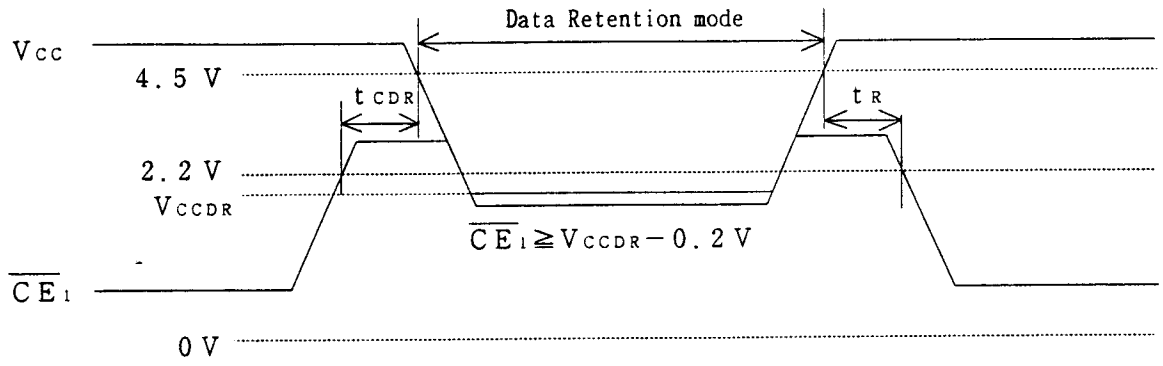
* 12. t_{WR} is measured from the end of write to the address change. t_{WR1} applies in case a write ends at $\overline{CE_1}$ or $\overline{WE}$ going high. t_{WR2} applies in case a write ends at CE_2 going low.

* 13. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

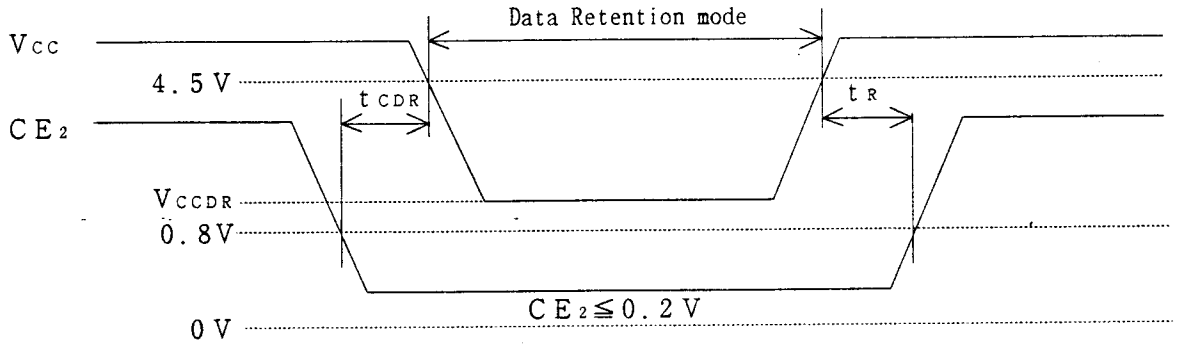
* 14. If $\overline{CE_1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

* 15. If $\overline{CE_1}$ goes high simultaneously with $\overline{WE}$ going high or before $\overline{WE}$ going high, the outputs remain in high impedance state.

Data Retention timing chart— $\overline{CE_1}$ Controlled) (*16)



Data Retention timing chart— (CE_2 Controlled)



Note) *16. To control the data retention mode at $\overline{CE_1}$, fix the input level of CE_2 between V_{CCDR} and $V_{CCDR}-0.2V$ or 0V and 0.2V during the data retention mode.

STATIC SRAM RAM Random Access Memory TSOP LH5164AT-80L CMOS 64K (8K x 8)