

### DESCRIPTION

The HY5117100A is the new generation and fast dynamic RAM organized 16,777,216 x 1-bit. The HY5117100A utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY5117100A to be packaged in standard 24/26 pin plastic SOJ, TSOP-II and Reverse TSOP-II.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 5 V $\pm$ 10% tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

### FEATURES

- Low power dissipation  
Max. battery back-up 2.75mW (SL-part)  
Max. CMOS standby 2.2mW (SL-part)  
5.5mW  
Max. TTL standby 11.0mW

Max. operating

| Speed | Power |
|-------|-------|
| 50    | 798mW |
| 60    | 660mW |
| 70    | 550mW |

- Single power supply of 5V $\pm$ 10%
- TTL compatible inputs and outputs
- Fast access time

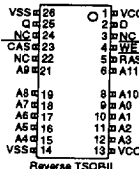
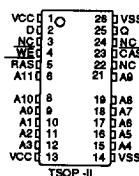
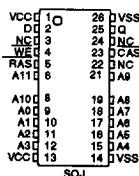
| Speed | t <sub>TRAC</sub> | t <sub>CAC</sub> | t <sub>PC</sub> |
|-------|-------------------|------------------|-----------------|
| 50    | 50ns              | 13ns             | 35ns            |
| 60    | 60ns              | 15ns             | 40ns            |
| 70    | 70ns              | 18ns             | 45ns            |

- Fast page mode operation
- Multi-bit test capability
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh and Self Refresh
- 2048 refresh cycles / 256ms (SL-part)
- 2048 refresh cycles / 32ms

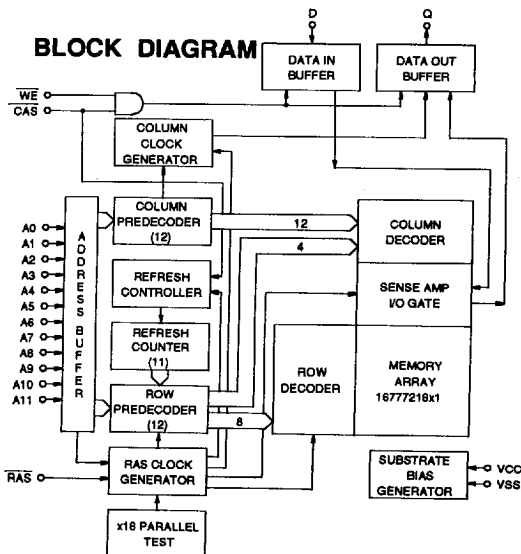
### PIN DESCRIPTION

|        |                       |
|--------|-----------------------|
| RAS    | Row Address Strobe    |
| CAS    | Column Address Strobe |
| WE     | Write Enable          |
| A0-A11 | Address Input         |
| D      | Data Input            |
| Q      | Data Output           |
| Vcc    | Power (+5V)           |
| Vss    | Ground                |

### PIN CONNECTION



### BLOCK DIAGRAM



This document is a general product description and is subject to change without notice. Hyundai electronics does not assume any responsibility for use of circuits described. No patent licences are implied.  
1AD20-10-MAR94

**ABSOLUTE MAXIMUM RATINGS**

| SYMBOL    | PARAMETER                          | RATING      | UNIT   |
|-----------|------------------------------------|-------------|--------|
| TA        | Ambient Temperature                | 0 to 70     | °C     |
| TSTG      | Storage Temperature                | -55 to 150  | °C     |
| VIN, VOUT | Voltage on Any Pin Relative to Vss | -1.0 to 7.0 | V      |
| Vcc       | Voltage on Vcc Relative to Vss     | -1.0 to 7.0 | V      |
| Ios       | Short Circuit Output Current       | 50          | mA     |
| Pd        | Power Dissipation                  | 1.02        | W      |
| TSOLDER   | Soldering Temperature•Time         | 260•10      | °C•sec |

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(TA= 0°C to 70°C)

| SYMBOL | PARAMETER            | MIN. | TYP. | MAX.     | UNIT |
|--------|----------------------|------|------|----------|------|
| Vcc    | Power Supply Voltage | 4.5  | 5.0  | 5.5      | V    |
| VIH    | Input High Voltage   | 2.4  | -    | Vcc+ 1.0 | V    |
| VIL    | Input Low Voltage    | -1.0 | -    | 0.8      | V    |

NOTE : All voltages are referenced to Vss.

**DC CHARACTERISTICS**

(TA=0°C to 70°C, VCC=5V±10%, VSS=0V, unless otherwise noted.)

| SYMBOL | PARAMETER                                                | TEST CONDITIONS                                                                                                             | SPEED                              | MIN.        | MAX.              | UNIT | NOTE  |
|--------|----------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|------------------------------------|-------------|-------------------|------|-------|
| ILI    | Input Leakage Current<br>(Any Input Pins)                | VSS≤VIN≤VCC+1.0,<br>All other pins not under test=VSS                                                                       |                                    | -10         | 10                | μA   |       |
| ILO    | Output Leakage Current<br>(High Impedance State)         | VSS≤VOUT≤VCC,<br>RAS & CAS at VIH                                                                                           |                                    | -10         | 10                | μA   |       |
| ICC1   | VCC Supply Current,<br>Operating                         | tRC=tRC (min.)                                                                                                              | 50<br>60<br>70                     | -<br>-<br>- | 145<br>120<br>100 | mA   | 1,2,3 |
| ICC2   | VCC Supply Current,<br>TTL Standby                       | RAS & CAS at VIH(min.),<br>other inputs ≥ VSS                                                                               |                                    | -           | 2                 | mA   |       |
| ICC3   | VCC Supply Current,<br>RAS-only refresh                  | tRC=tRC (min.),                                                                                                             | 50<br>60<br>70                     | -<br>-<br>- | 145<br>120<br>100 | mA   | 1,3   |
| ICC4   | VCC Supply Current,<br>Fast Page mode                    | tPC=tPC (min.),                                                                                                             | 50<br>60<br>70                     | -<br>-<br>- | 90<br>80<br>70    | mA   | 1,2,3 |
| ICC5   | VCC Supply Current,<br>CMOS Standby                      | RAS & CAS ≥ VCC - 0.2V                                                                                                      | SL-part                            | -<br>-      | 1<br>0.4          | mA   | 5     |
| ICC6   | VCC Supply Current,<br>CAS-before-RAS refresh            | tRC=tRC (min.),                                                                                                             | 50<br>60<br>70                     | -<br>-<br>- | 145<br>120<br>100 | mA   | 1,3   |
| ICC7   | VCC Supply Current,<br>Battery Back Up<br>(SL-part only) | tRC=125μs,<br>CAS=CBR cycling or 0.2V,<br>WE=VCC-0.2V,<br>A0-A11=VCC-0.2V or 0.2V,<br>D=VCC - 0.2V, 0.2V or open,<br>Q=open | tRAS≤<br>300ns<br><br>tRAS≤<br>1μs | -<br>-<br>- | 300<br><br>500    | μA   | 1,4,5 |
| ICC8   | VCC Supply Current<br>Self Refresh<br>(SL-part only)     | RAS & CAS ≤0.2V<br>WE & A0-A11=VCC-0.2V or 0.2V,<br>D=VCC - 0.2V, 0.2V or open,<br>Q=open                                   |                                    |             | 300               | μA   | 5     |
| VOL    | Output Low Voltage                                       | IOL=4.2mA                                                                                                                   |                                    | -           | 0.4               | V    |       |
| VOH    | Output High Voltage                                      | IOH=5mA                                                                                                                     |                                    | 2.4         | -                 | V    |       |

**NOTE :**

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rate.
2. ICC1 and ICC4 depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while RAS=VIL and CAS=VIH.
4. tRAS(max.)=1μs is only applied to refresh of battery backup but tRAS(max.)=10μs is applied to normal functional operating.
5. ICC5(max.)=0.4mA and ICC7 and ICC8 are applied to SL-part only (HY5117100ASLJ, HY5117100ASLT and HY5117100ASLR).

**AC CHARACTERISTICS**

(TA=0°C to 70°C, VCC=5V±10%, VSS=0V, unless otherwise noted.) NOTE : 1, 2, 3

| TA=0°C to 70°C, VCC=5V±10%, VSS=0V, unless otherwise noted. NOTE 1, 2, 3 |        |                                             |                                   |      |      |      |      |      |      |        |
|--------------------------------------------------------------------------|--------|---------------------------------------------|-----------------------------------|------|------|------|------|------|------|--------|
| #                                                                        | SYMBOL | PARAMETER                                   | HY5117100AJC/TC/RC/SLJC/SLTC/SLRC |      |      |      |      |      | UNIT | NOTE   |
|                                                                          |        |                                             | -50                               |      | -60  |      | -70  |      |      |        |
|                                                                          |        |                                             | MIN.                              | MAX. | MIN. | MAX. | MIN. | MAX. |      |        |
| 1                                                                        | tRC    | Random Read or Write Cycle Time             | 90                                | -    | 110  | -    | 130  | -    | ns   |        |
| 2                                                                        | tRWC   | Read-Modify-Write Cycle Time                | 110                               | -    | 130  | -    | 155  | -    | ns   |        |
| 3                                                                        | tPC    | Fast Page Mode Cycle Time                   | 35                                | -    | 40   | -    | 45   | -    | ns   |        |
| 4                                                                        | tPRWC  | Fast Page Mode Read-Modify-Write Cycle Time | 55                                | -    | 60   | -    | 70   | -    | ns   |        |
| 5                                                                        | tRAC   | Access Time from RAS                        | -                                 | 50   | -    | 60   | -    | 70   | ns   | 4,9,10 |
| 6                                                                        | tCAC   | Access Time from CAS                        | -                                 | 13   | -    | 15   | -    | 18   | ns   | 4,9    |
| 7                                                                        | tAA    | Access Time from Column Address             | -                                 | 25   | -    | 30   | -    | 35   | ns   | 4,10   |
| 8                                                                        | tCPA   | Access Time from CAS Precharge              | -                                 | 30   | -    | 35   | -    | 40   | ns   | 4      |
| 9                                                                        | tCLZ   | CAS to Output Low Impedance                 | 0                                 | -    | 0    | -    | 0    | -    | ns   | 4      |
| 10                                                                       | tOFF   | Output Buffer Turn-off Delay                | 0                                 | 10   | 0    | 13   | 0    | 15   | ns   | 5      |
| 11                                                                       | tT     | Transition Time (Rise and Fall)             | 3                                 | 50   | 3    | 50   | 3    | 50   | ns   | 3      |
| 12                                                                       | tRP    | RAS Precharge Time                          | 30                                | -    | 40   | -    | 50   | -    | ns   |        |
| 13                                                                       | tRAS   | RAS Pulse Width                             | 50                                | 10K  | 60   | 10K  | 70   | 10K  | ns   |        |
| 14                                                                       | tRASP  | RAS Pulse Width (Fast Page Mode)            | 50                                | 200K | 60   | 200K | 70   | 200K | ns   |        |
| 15                                                                       | tRSH   | RAS Hold Time                               | 13                                | -    | 15   | -    | 18   | -    | ns   |        |
| 16                                                                       | tCSH   | CAS Hold Time                               | 50                                | -    | 60   | -    | 70   | -    | ns   |        |
| 17                                                                       | tCAS   | CAS Pulse Width                             | 13                                | 10K  | 15   | 10K  | 18   | 10K  | ns   |        |
| 18                                                                       | tRCD   | RAS to CAS Delay                            | 13                                | 37   | 20   | 45   | 20   | 52   | ns   | 9      |
| 19                                                                       | tRAD   | RAS to Column Address Delay Time            | 13                                | 25   | 15   | 30   | 15   | 35   | ns   | 10     |
| 20                                                                       | tCRP   | CAS to RAS Precharge Time                   | 5                                 | -    | 5    | -    | 5    | -    | ns   |        |
| 21                                                                       | tCP    | CAS Precharge Time                          | 10                                | -    | 10   | -    | 10   | -    | ns   |        |
| 22                                                                       | tASR   | Row Address Set-up Time                     | 0                                 | -    | 0    | -    | 0    | -    | ns   |        |
| 23                                                                       | tRAH   | Row Address Hold Time                       | 10                                | -    | 10   | -    | 10   | -    | ns   |        |
| 24                                                                       | tASC   | Column Address Set-up Time                  | 0                                 | -    | 0    | -    | 0    | -    | ns   |        |
| 25                                                                       | tCAH   | Column Address Hold Time                    | 10                                | -    | 10   | -    | 10   | -    | ns   |        |
| 26                                                                       | tAR    | Column Address Hold Time from RAS           | 45                                | -    | 50   | -    | 55   | -    | ns   |        |
| 27                                                                       | tRAL   | Column Address to RAS Lead Time             | 25                                | -    | 30   | -    | 35   | -    | ns   |        |
| 28                                                                       | tRCS   | Read Command Set-up Time                    | 0                                 | -    | 0    | -    | 0    | -    | ns   |        |
| 29                                                                       | tRCH   | Read Command Hold Time Referenced to CAS    | 0                                 | -    | 0    | -    | 0    | -    | ns   | 6      |
| 30                                                                       | tRRH   | Read Command Hold Time Referenced to RAS    | 0                                 | -    | 0    | -    | 0    | -    | ns   | 6      |
| 31                                                                       | tWCH   | Write Command Hold Time                     | 8                                 | -    | 10   | -    | 10   | -    | ns   |        |
| 32                                                                       | tWCR   | Write Command Hold Time from RAS            | 50                                | -    | 55   | -    | 60   | -    | ns   |        |
| 33                                                                       | tWP    | Write Command Pulse Width                   | 8                                 | -    | 10   | -    | 10   | -    | ns   |        |
| 34                                                                       | tRWL   | Write Command to RAS Lead Time              | 13                                | -    | 15   | -    | 18   | -    | ns   |        |
| 35                                                                       | tCWL   | Write Command to CAS Lead Time              | 13                                | -    | 15   | -    | 18   | -    | ns   |        |
| 36                                                                       | tDS    | Data-In Set-up Time                         | 0                                 | -    | 0    | -    | 0    | -    | ns   | 7      |
| 37                                                                       | tDH    | Data-In Hold Time                           | 10                                | -    | 10   | -    | 10   | -    | ns   | 7      |
| 38                                                                       | tDHR   | Data-In Hold Time Referenced to RAS         | 50                                | -    | 55   | -    | 60   | -    | ns   |        |
| 39                                                                       | tREF   | Refresh Period (2048 cycles)                | -                                 | 32   | -    | 32   | -    | 32   | ms   | 12     |
|                                                                          |        | SL-part                                     | -                                 | 256  | -    | 256  | -    | 256  |      | 11     |
| 40                                                                       | tWCS   | Write Command Set-up Time                   | 0                                 | -    | 0    | -    | 0    | -    | ns   | 8      |

**AC CHARACTERISTICS**

(continued)

| #  | SYMBOL | PARAMETER                                   | HY5117100AJC/TC/RC/SLJC/SLTC/SLRC |      |      |      |      |      | UNIT | NOTE |
|----|--------|---------------------------------------------|-----------------------------------|------|------|------|------|------|------|------|
|    |        |                                             | -50                               |      | -60  |      | -70  |      |      |      |
|    |        |                                             | MIN.                              | MAX. | MIN. | MAX. | MIN. | MAX. |      |      |
| 41 | tCWD   | CAS to WE Delay Time                        | 13                                | -    | 15   | -    | 18   | -    | ns   | 8    |
| 42 | tRWD   | RAS to WE Delay Time                        | 50                                | -    | 60   | -    | 70   | -    | ns   | 8    |
| 43 | tAWD   | Column Address to WE Delay Time             | 25                                | -    | 30   | -    | 35   | -    | ns   | 8    |
| 44 | tCSR   | CAS Set-up Time (CBR Cycle)                 | 5                                 | -    | 5    | -    | 5    | -    | ns   |      |
| 45 | tCHR   | CAS Hold Time (CBR Cycle)                   | 10                                | -    | 15   | -    | 15   | -    | ns   |      |
| 46 | tRPC   | RAS to CAS Precharge Time                   | 0                                 | -    | 0    | -    | 0    | -    | ns   |      |
| 47 | tCPT   | CAS Precharge Time (CBR Counter Test)       | 15                                | -    | 20   | -    | 25   | -    | ns   |      |
| 48 | tCPWD  | WE Delay Time from CAS Precharge            | 30                                | -    | 35   | -    | 40   | -    | ns   | 8    |
| 49 | tRHCP  | RAS Hold Time from CAS Precharge            | 30                                | -    | 35   | -    | 40   | -    | ns   |      |
| 50 | tWRP   | WE to RAS Precharge Time (CBR Cycle)        | 10                                | -    | 10   | -    | 10   | -    | ns   |      |
| 51 | tWRH   | WE to RAS Hold Time (CBR Cycle)             | 10                                | -    | 10   | -    | 10   | -    | ns   |      |
| 52 | tWTS   | Write Command Set-up Time<br>(Test Mode In) | 10                                | -    | 10   | -    | 10   | -    | ns   |      |
| 53 | tWTH   | Write Command Hold Time<br>(Test Mode In)   | 10                                | -    | 10   | -    | 10   | -    | ns   |      |
| 54 | tRASS  | RAS Pulse Width (Self Refresh)              | 100                               | -    | 100  | -    | 100  | -    | μs   |      |
| 55 | tRPS   | RAS Pre charge Time (Self Refresh)          | 120                               | -    | 130  | -    | 150  | -    | ns   |      |
| 56 | tCHS   | CAS Hold Time from RAS (Self Refresh)       | -50                               | -    | -50  | -    | -50  | -    | ns   |      |

**AC CHARACTERISTICS IN TEST MODE** NOTE 13

| #  | SYMBOL | PARAMETER                                   | HY5117100AJ/T/R/SLJ/SLT/SLR/ |      |      |      |      |      | UNIT | NOTE   |
|----|--------|---------------------------------------------|------------------------------|------|------|------|------|------|------|--------|
|    |        |                                             | -50                          |      | -60  |      | -70  |      |      |        |
|    |        |                                             | MIN.                         | MAX. | MIN. | MAX. | MIN. | MAX. |      |        |
| 1  | tRC    | Random Read or Write Cycle Time             | 95                           | -    | 115  | -    | 135  | -    | ns   |        |
| 2  | tRWC   | Read-Modify-Write Cycle Time                | 115                          | -    | 135  | -    | 160  | -    | ns   |        |
| 3  | tPC    | Fast Page Mode Cycle Time                   | 40                           | -    | 45   | -    | 50   | -    | ns   |        |
| 4  | tPRWC  | Fast Page Mode Read-Modify-Write Cycle Time | 60                           | -    | 65   | -    | 75   | -    | ns   |        |
| 5  | tRAC   | Access Time from RAS                        | -                            | 55   | -    | 65   | -    | 75   | ns   | 4,9,10 |
| 6  | tCAC   | Access Time from CAS                        | -                            | 18   | -    | 20   | -    | 23   | ns   | 4,9    |
| 7  | tAA    | Access Time from Column Address             | -                            | 30   | -    | 35   | -    | 40   | ns   | 4,10   |
| 8  | tCPA   | Access Time from CAS Precharge              | -                            | 35   | -    | 40   | -    | 45   | ns   | 4      |
| 13 | tRAS   | RAS Pulse Width                             | 55                           | 10K  | 65   | 10K  | 75   | 10K  | ns   |        |
| 14 | tRASP  | RAS Pulse Width (Fast Page Mode)            | 55                           | 200K | 65   | 200K | 75   | 200K | ns   |        |
| 15 | tRSH   | RAS Hold Time                               | 18                           | -    | 20   | -    | 23   | -    | ns   |        |
| 16 | tCSH   | CAS Hold Time                               | 55                           | -    | 65   | -    | 75   | -    | ns   |        |
| 17 | tCAS   | CAS Pulse Width                             | 18                           | 10K  | 20   | 10K  | 23   | 10K  | ns   |        |
| 27 | tRAL   | Column Address to RAS Lead Time             | 30                           | -    | 35   | -    | 40   | -    | ns   |        |
| 41 | tCWD   | CAS to WE Delay Time                        | 18                           | -    | 20   | -    | 23   | -    | ns   | 8      |
| 42 | tRWD   | RAS to WE Delay Time                        | 55                           | -    | 65   | -    | 75   | -    | ns   | 8      |
| 43 | tAWD   | Column Address to WE Delay Time             | 30                           | -    | 35   | -    | 40   | -    | ns   | 8      |

**NOTE :**

1. An initial pause of 200 $\mu$ s is required after power-up followed by any 8 RAS only or CAS-before-RAS refresh cycle before proper device operation is achieved.
2. If RAS=Vss during power-up, the HY5117100A could begin an active cycle. These condition results in higher current than necessary which is demanded from the power supply during power-up. It is recommended that RAS and CAS track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH(min.) and VIL(max.), and are assumed to be 5ns for all inputs.
4. Measured at VOH=2.4V and VOL=0.4V with a load equivalent to 2 TTL loads and 100pF.
5. toFF(max.) and toEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles and to WE leading edge in Read-Modify-Write cycles.
8. twCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If twCS(twCS(min.)), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tRWD(tRWD(min.)), tCWD(tCWD(min.)), tAWD(tAWD(min.)), and tCPWD(tCPWD(min.)), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. tREF(max.)=256ms is applied to SL-Parts (HY5117100ASLJ, HY5117100ASLT and HY5117100ASLR).
12. A burst of 2048 CAS-before-RAS refresh cycles must be executed within 32ms(256ms for SL-part) after exiting self refresh.
13. These specifications are applied to the test Mode.

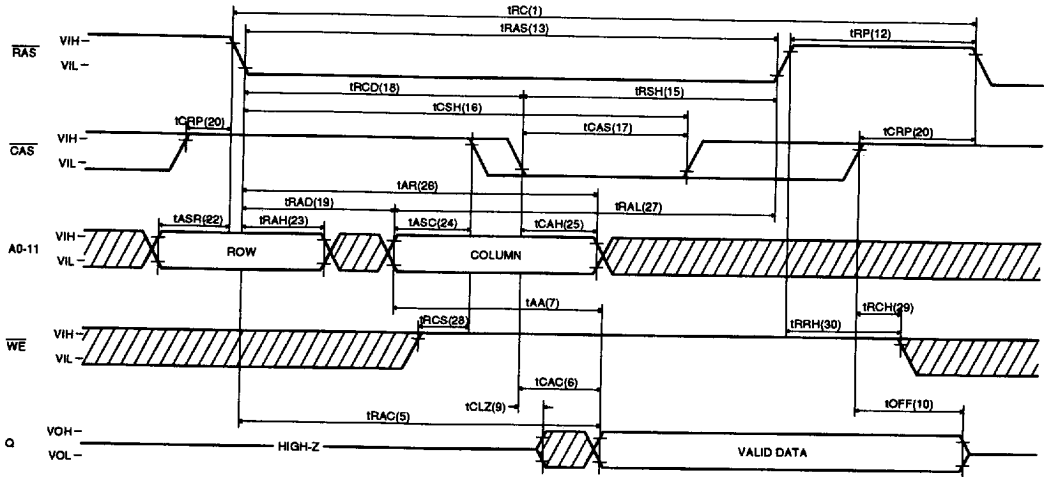
**CAPACITANCE**

(TA=25°C, VCC=5V, 10%, VSS=0V, f=1MHz, unless otherwise noted.)

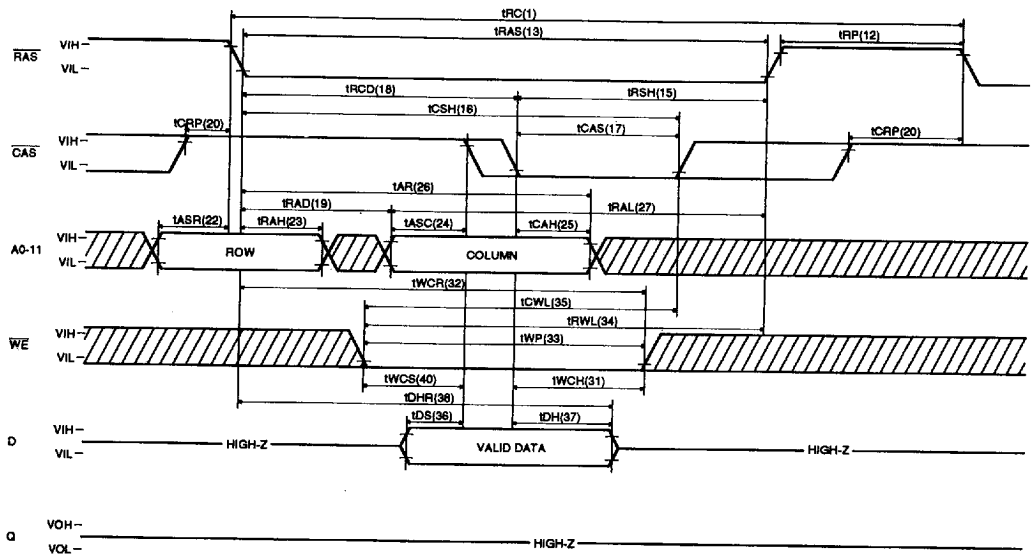
| SYMBOL | PARAMETER                        | TYP. | MAX. | UNIT |
|--------|----------------------------------|------|------|------|
| CIN1   | Input Capacitance (A0-A10)       | -    | 5    | pF   |
| CIN2   | Input Capacitance (RAS, CAS, WE) | -    | 7    | pF   |
| COUT   | Output Capacitance (Q)           | -    | 7    | pF   |

**TIMING DIAGRAM**

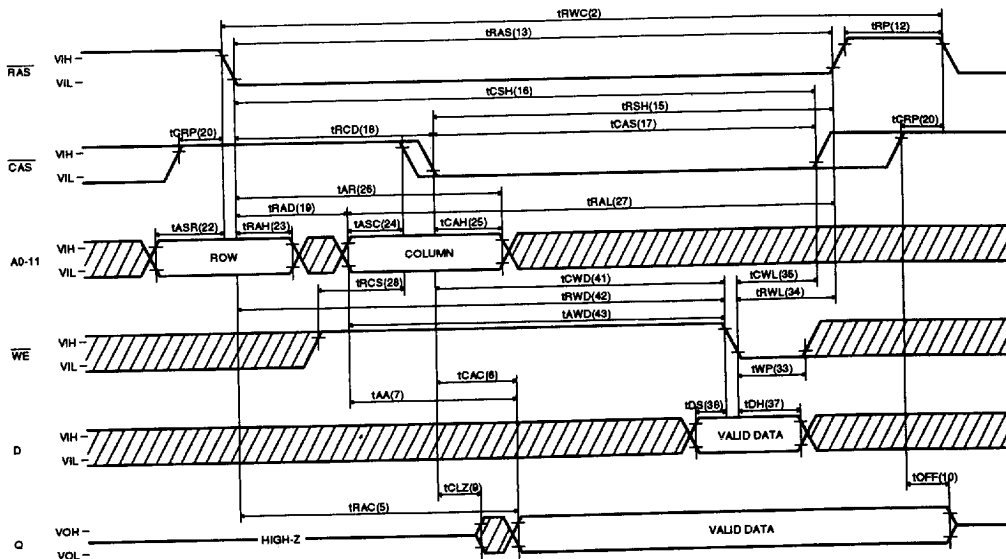
**READ CYCLE**



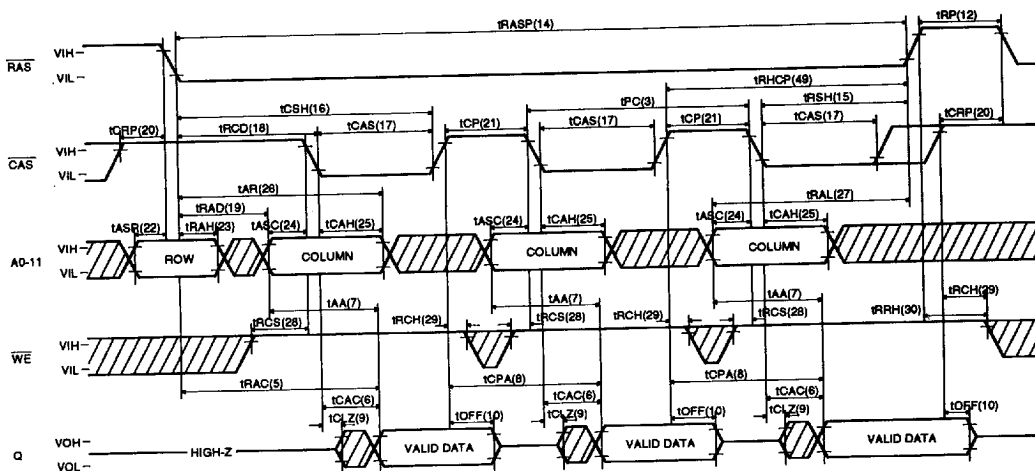
**EARLY WRITE CYCLE**



READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

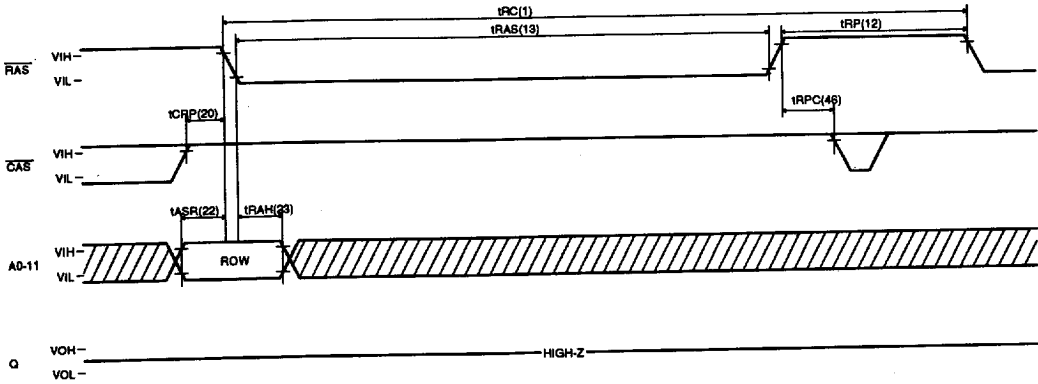




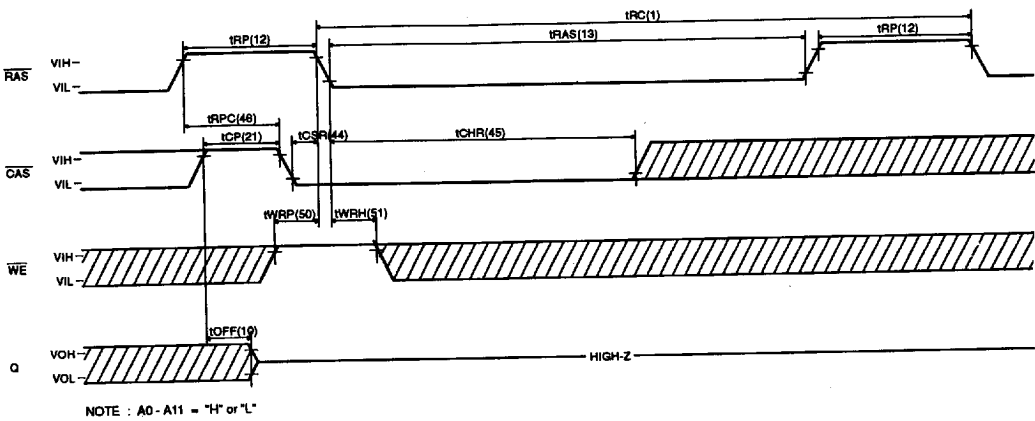
The timing diagram illustrates the sequence of signals for the 64K1602 LCD module. The signals and their timing parameters are as follows:

- RAS:** High Voltage Input (VIH), Low Voltage Input (VIL). Timing parameters:  $t_{RASP}(14)$ ,  $t_{RCP}(20)$ ,  $t_{RSH}(15)$ ,  $t_{RCP}(20)$ .
- CAS:** High Voltage Input (VIH), Low Voltage Input (VIL). Timing parameters:  $t_{RCD}(18)$ ,  $t_{CAS}(17)$ ,  $t_{CP}(21)$ ,  $t_{CAS}(17)$ ,  $t_{CP}(21)$ ,  $t_{CAS}(17)$ ,  $t_{RCP}(20)$ .
- A0-11:** Address bus. Timing parameters:  $t_{AR}(26)$ ,  $t_{RAD}(19)$ ,  $t_{RAH}(23)$ ,  $t_{ASC}(24)$ ,  $t_{CAH}(25)$ ,  $t_{ASC}(24)$ ,  $t_{CAH}(25)$ ,  $t_{ASC}(24)$ ,  $t_{CAH}(25)$ .
- WE:** Write Enable. Timing parameters:  $t_{RWD}(42)$ ,  $t_{AWD}(43)$ ,  $t_{CWL}(35)$ ,  $t_{AWD}(43)$ ,  $t_{CWL}(35)$ ,  $t_{AWD}(43)$ ,  $t_{CWL}(35)$ ,  $t_{AWD}(43)$ ,  $t_{CWL}(35)$ .
- D:** Data bus. Timing parameters:  $t_{RPS}(28)$ ,  $t_{CWD}(41)$ ,  $t_{WP}(33)$ ,  $t_{CWD}(41)$ ,  $t_{WP}(33)$ ,  $t_{CWD}(41)$ ,  $t_{WP}(33)$ ,  $t_{CWD}(41)$ ,  $t_{WP}(33)$ .
- Q:** Output bus. Timing parameters:  $t_{AA}(7)$ ,  $t_{CAC}(6)$ ,  $t_{DS}(36)$ ,  $t_{DH}(37)$ ,  $t_{CAC}(6)$ ,  $t_{DS}(36)$ ,  $t_{DH}(37)$ ,  $t_{CAC}(6)$ ,  $t_{DS}(36)$ ,  $t_{DH}(37)$ .
- Other parameters:**  $t_{RAC}(5)$ ,  $t_{CPA}(8)$ ,  $t_{OFF}(10)$ ,  $t_{CLZ}(9)$ ,  $t_{CPA}(8)$ ,  $t_{OFF}(10)$ ,  $t_{CLZ}(9)$ ,  $t_{OFF}(10)$ .

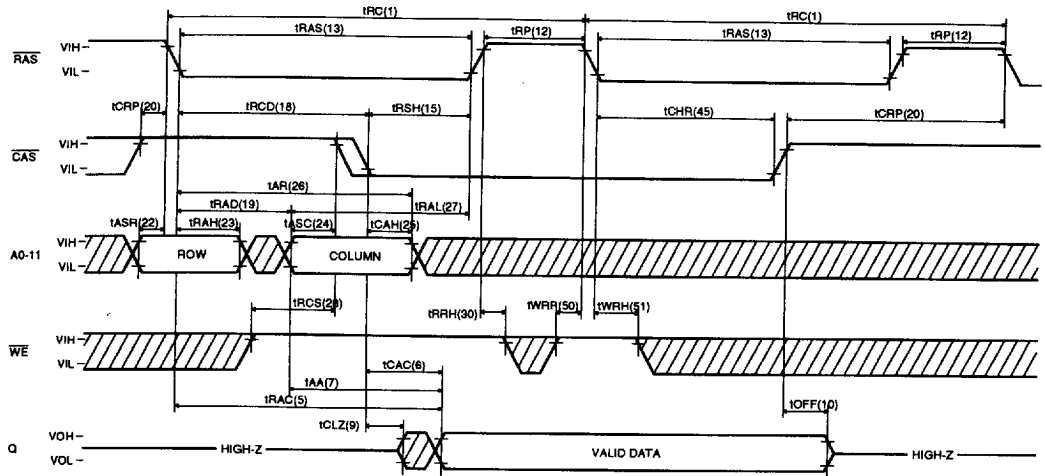
**RAS-ONLY REFRESH CYCLE**



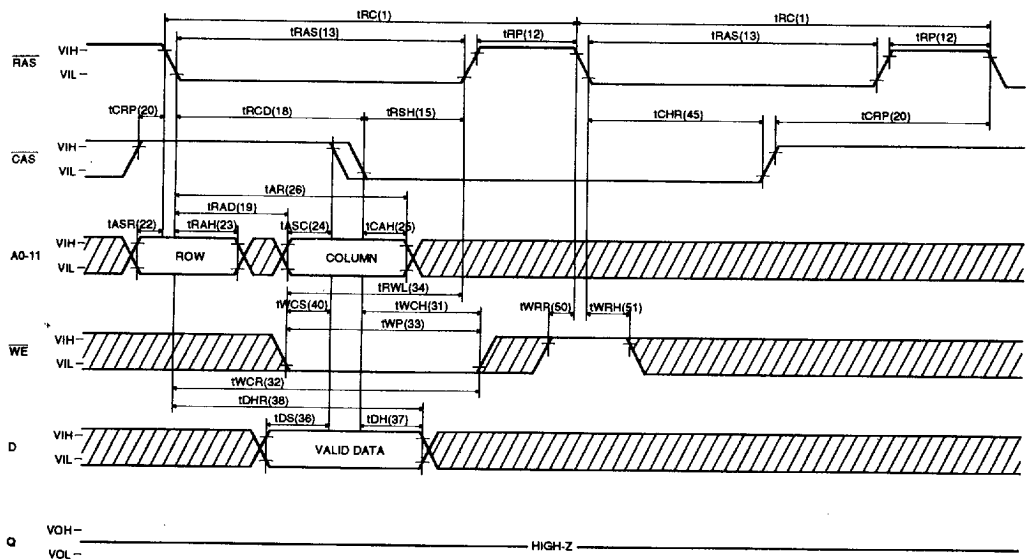
**CAS-BEFORE-RAS REFRESH CYCLE**



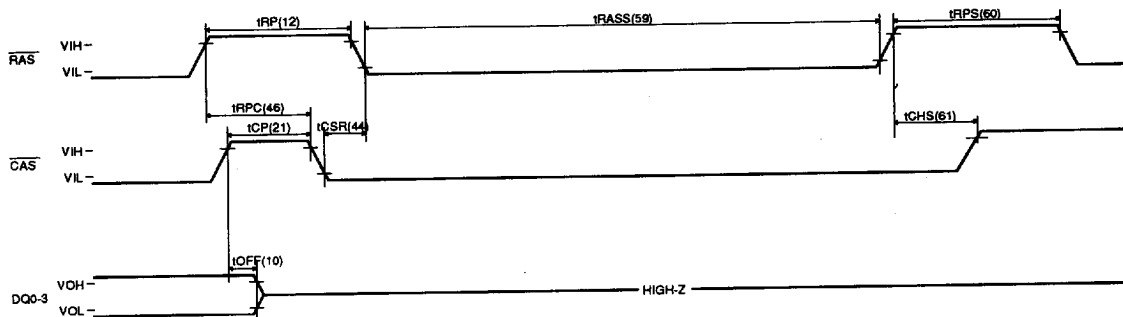
**HIDDEN REFRESH CYCLE (READ)**



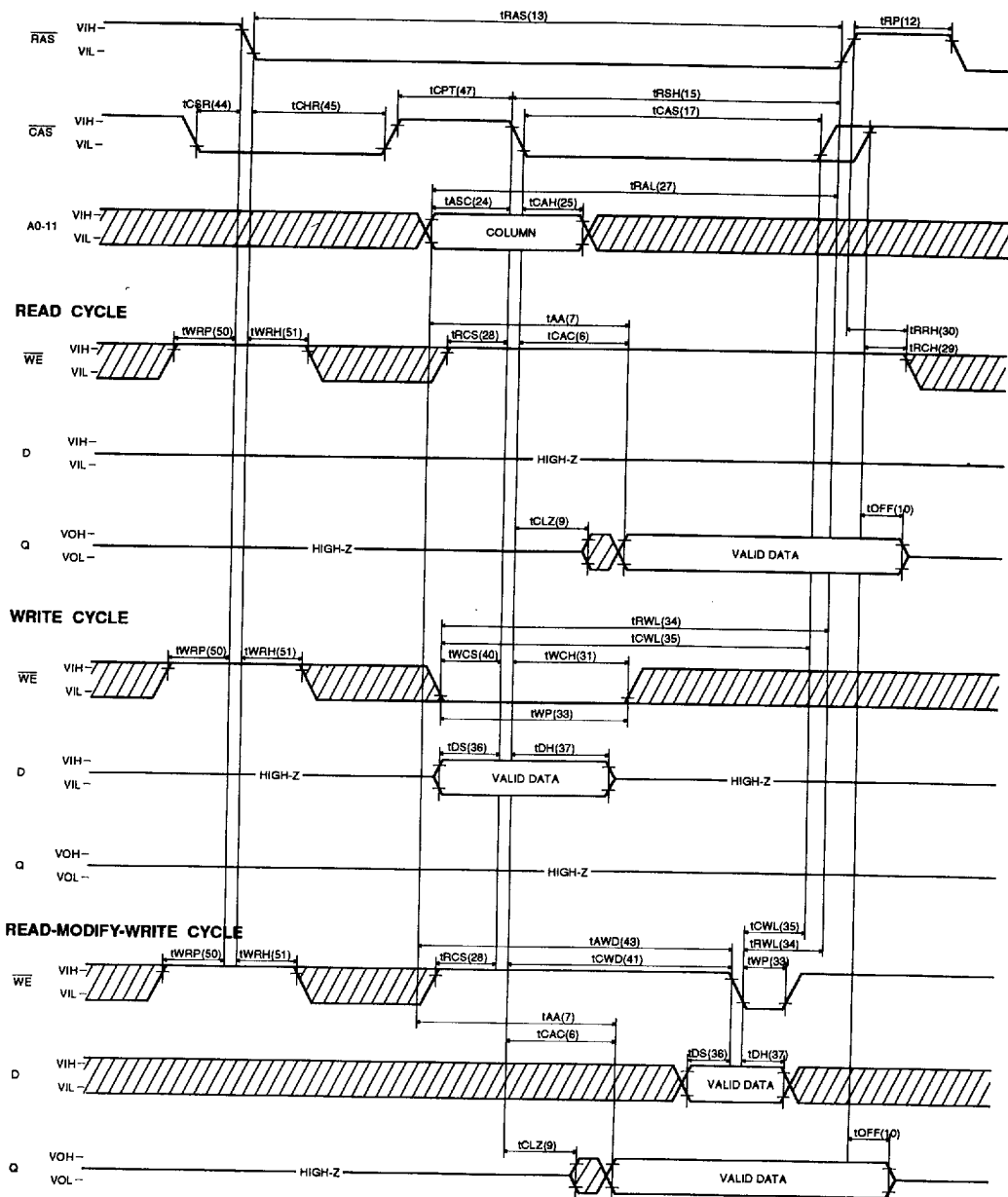
**HIDDEN REFRESH CYCLE (WRITE)**



**CAS-BEFORE-RAS SELF REFRESH**



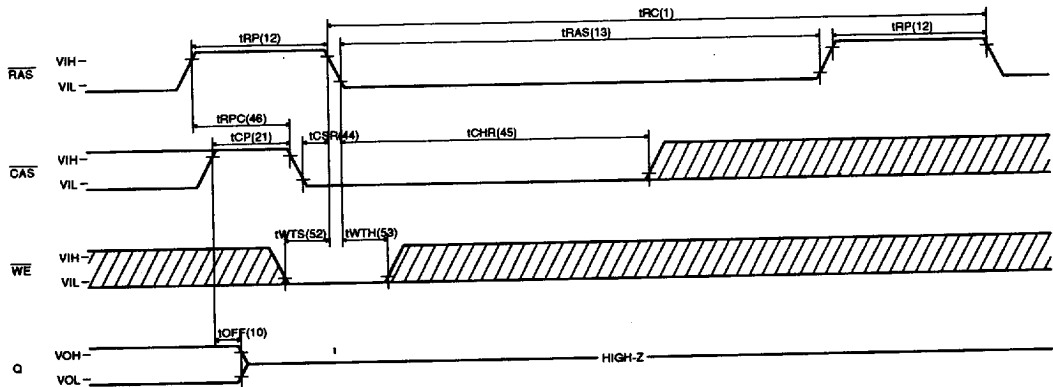
**CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE**



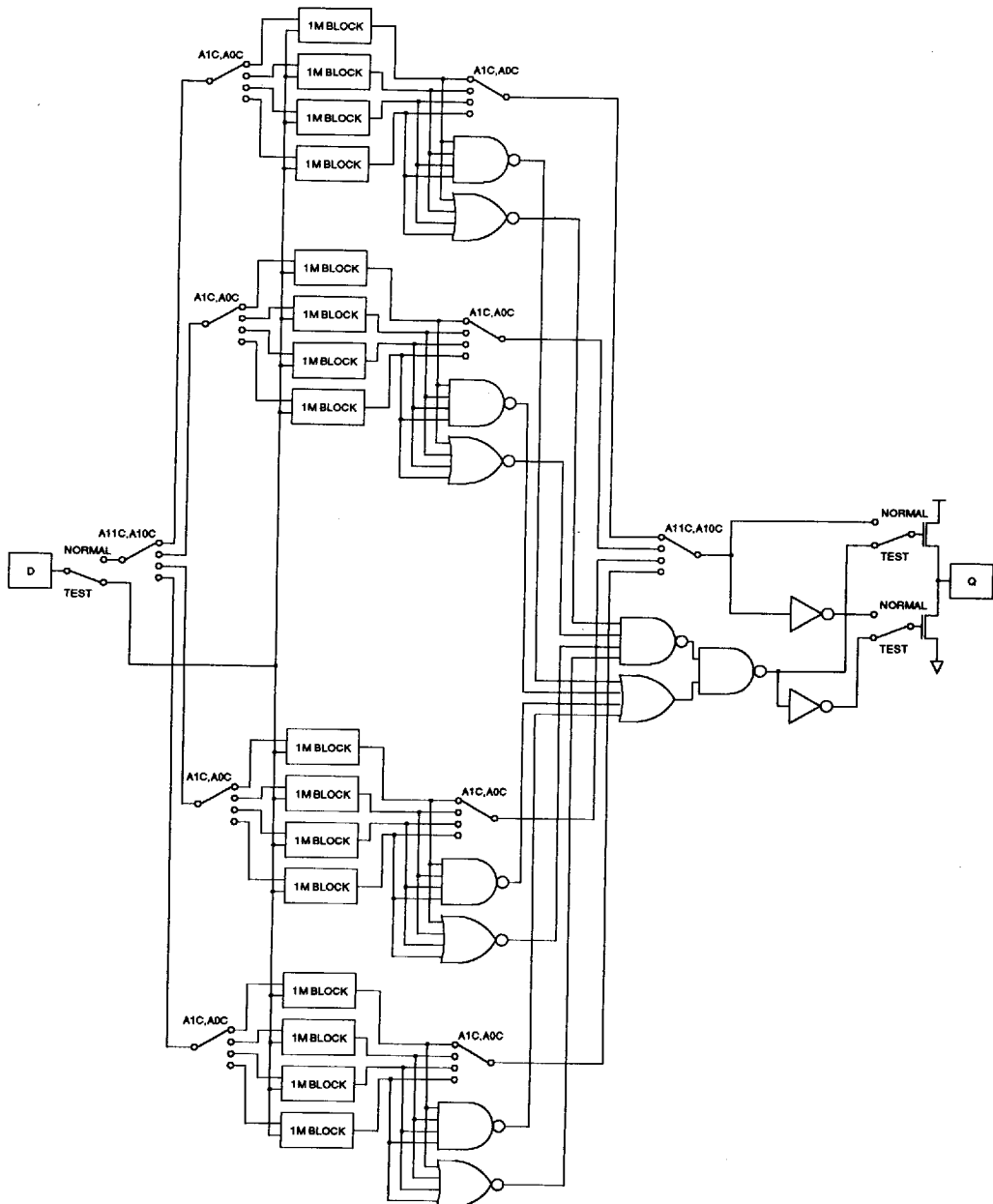
## TEST MODE

The HY5117100A is a DRAM organized 16,777,216 x 1-bit. It is internally organized 1,048,576 x 16-bit. In Test Mode, data are written into 16 sectors (Each is composed of 1M bits) in parallel and retrieved the same way. Column address A0, A1, A10 and A11 are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the Q pin indicates a "1". If they are not equal, the Q pin indicates a "0". Belowing shows the timing diagram of the HY5117100A to enter Test Mode. In Test Mode, the 16Mx1 DRAM can be tested as if it were a 1Mx1 DRAM. WE, CAS-before-RAS cycle (Test Mode In Cycle) puts the HY5117100A into Test Mode and CAS-before-RAS or RAS-only refresh cycle puts it back into Normal Mode. In Test Mode, WE, CAS-before-RAS cycle shall be used for the refresh operation. The Test Mode function reduces test time (1/16 in case of N test pattern)

## TEST MODE IN CYCLE



**BLOCK DIAGRAM IN TEST MODE**



**ORDERING INFORMATION**

| PART NO       | SPEED    | POWER   | PACKAGE    |
|---------------|----------|---------|------------|
| HY5117100AJ   | 50/60/70 |         | SOJ        |
| HY5117100ASLJ | 50/60/70 | SL-part | SOJ        |
| HY5117100AT   | 50/60/70 |         | TSOP-II    |
| HY5117100ASLT | 50/60/70 | SL-part | TSOP-II    |
| HY5117100AR   | 50/60/70 |         | TSOP-II(R) |
| HY5117100ASLR | 50/60/70 | SL-part | TSOP-II(R) |