622 Mbps Multimode Fiber Transceiver for ATM, SONET STS-12/SDH STM-4

Technical Data

HFBR-5207

Features

- **1300 nm LED-based Transceiver for 500 m Links with MMF Cables**
- **Compliant with ATM Forum 622.08 Mbps Physical Layer Specification AF-PHY-0046.000**
- **Compliant with Specifications Proposed to ANSI T1E1.2 Committee for Inclusion in T1.646-1995 Broadband ISDN and T1E1.2/96-002 SONET Network to Customer Installation Interface Standards**
- **Compliant with Specifications Proposed to ANSI T1X1.5 Committee for Inclusion in T1.105.06 SONET Physical Layer Specifications Standard**
- **Multisourced 2 x 9 Pin-out Package Style Derived from 1 x 9 Pin-out Industry Standard Package Style**
- **Integral Duplex SC Connector Receptacle Compliant with TIA/EIA and IEC Standards**
- **Single +5 V Power Supply Operation and PECL Logic Interfaces**
- **Integral Digital PLL Provides Regenerated Differential Clock Output**
- **Integral Decision Circuit Provides Re-timed Differential Data Output**
- **Optional Internally Generated Receiver Clock**
- **Wave Solder and Aqueous Wash Process Compatible**
- **Manufactured in an ISO 9001 Certified Facility**

Applications

- **ATM 622 Mbps MMF Links from Switch-to-Switch or Switch-to-Server in the End-User Premise**
- **SONET STS-12/SDH STM-4 MMF Interconnections**

Description

General

The HFBR-5207 is a 1300 nm LED-based transceiver with integral clock and data recovery circuits. It provides a very cost-effective solution to 500 metre 622 Mbps data link requirements in the Customer Premise ATM and Telecom Office markets.

The HFBR-5207 provides a low-cost 622 Mbps Multimode Fiber

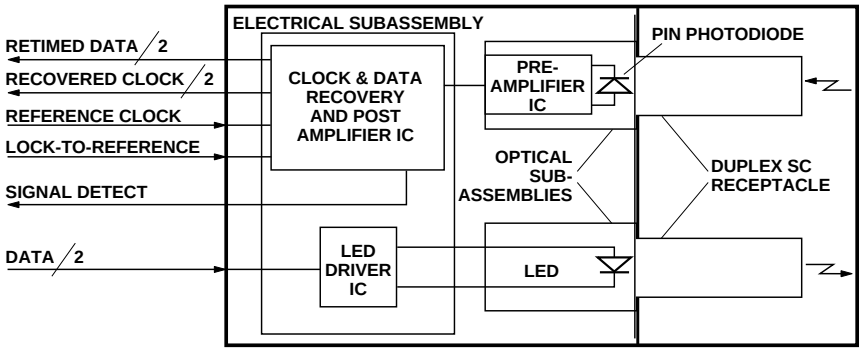
(MMF) interconnection for ATM switch-to-switch and switch-to-server applications within a customer premise.

The HFBR-5207 also provides a low-cost alternative to traditional 1300 nm laser-based, single-mode fiber transmitter/receiver solutions for SONET/SDH connections up to 500 metres long within telecommunication systems.

The new multisourced 2 x 9 footprint package style is a variation of the standard 1 x 9 package with an integral Duplex SC connector receptacle. The extra row of 9 pins provides connections for the additional recovered clock output as well as an option to generate a local clock from an external, low-frequency reference clock to replace the recovered clock when in-coming optical signals become unusable.

Single Mode Transceiver

This new 2 x 9 package style also is available in a single mode fiber transceiver version, the CDX2622, with 15 km performance. This single mode product uses the same pin-out so that a single board layout can be designed to provide either multimode or single mode fiber performance depending on which transceiver is inserted. In addition to the integral clock and data recovery circuit, the CDX2622 also provides the traditional telecom laser diode bias current and output power monitors as well as a transmitter disable function.



Block Diagram.

Transmitter Section

The transmitter section of this transceiver is similar to 1300 nm LED transceivers in use at the 155 Mbps rate. It consists of a 1300 nm InGaAsP LED in an optical sub-assembly (OSA) which mates to the fiber cable. The LED OSA is driven by a custom, silicon bipolar IC which converts differential input PECL logic signals, ECL referenced to a +5 volt supply, into an analog LED drive current.

Receiver Section

The receiver section of the transceiver provides a full set of features including an integral clock and data recovery (CDR) circuit together with an optional, selectable receiver local clock source. The receiver starts with an InGaAs PIN photo-diode mounted together with a custom, silicon bipolar transimpedance preamplifier IC in an OSA. This OSA is connected to a custom, silicon bipolar circuit providing post-amplification and quantization, CDR function, and optical signal detection.

The custom, silicon bipolar circuit includes a Signal Detect circuit which provides a PECL logic-high output upon detection of a usable input optical signal level. Signal Detect is a basic fiber failure indicator. This signal-ended low-power PECL output is designed to drive a standard PECL input using a 10 kΩ load instead of the normal 50 Ω PECL load.

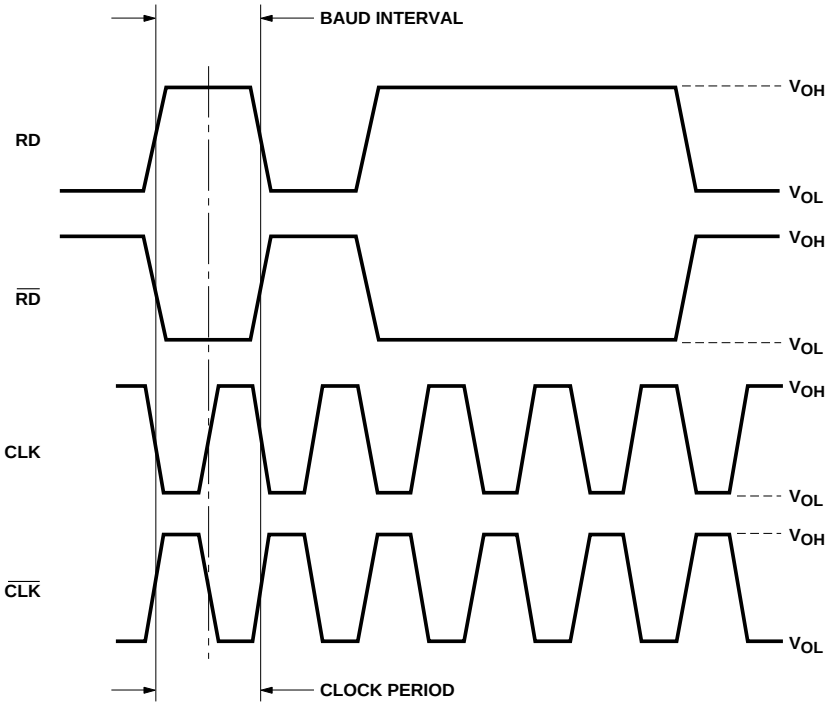


Figure 1. Relative Timing Relationship Between Output Re-timed Data and Recovered Clock Signals.

Detailed Description of Receiver CDR Function

In normal operation, the CDR data loop is able to acquire and maintain bit lock without the use of the optional, external reference clock. This loop consists of a patented phase/frequency detector with false-lock protection. The recovered clock is used to re-time the quantizer data output, which completes the full CDR function.

The relative timing relationship between the output re-timed data and the recovered clock signals is shown graphically in Figure 1. Fundamentally, the rising edge of the Clock and the falling edge of the clock bar will occur at the center of the Data or Data-bar baud interval. Conversely, the Clock falling edge and the Clock-bar rising edge will be at the edges of the Data or Data-bar baud interval.

For input optical power greater than the specified receiver sensitivity of -26 dBm, the bit-error-ratio will be better than 1×10^{-10}. As the input power is decreased by several dB, the bit-error-ratio degrades. Within 1 dB below the 1×10^{-2} BER input optical power level, the CDR will begin to lose lock and the clock frequency will drift from 622.08 MHz. Once the CDR loses lock, the clock frequency will sweep in the entire VCO range, about 540 to 700 MHz. The rate of the sweep will depend on the input optical power. The sweep rate gets faster the lower the input optical power is. Once the input optical power is 2 dB below the lock point, the sweep rate approaches the maximum. At this point the clock and data outputs look no different than the case with no input optical power. There will be a data edge for every clock edge. The data output will consist of randomly switching data bits, i.e., noise.

Detailed Description of Receiver Signal Detect Feature

As the input optical power is decreased, Signal Detect will switch from high to low (de-assert point) somewhere between 3 dB below sensitivity and the no light input level. As the input optical power is increased from very low levels, Signal Detect will switch from low to high (assert point) somewhere between 2 dB below sensitivity and no input optical power at all. The assert level will be at least 1.0 dB higher than the de-assert level.

Optional Local Clock Generation

In applications where the receiver recovered clock frequency is not allowed to drift upon loss of input optical signal, this transceiver has the ability to generate a local clock output by multiplying an optional, external 19.44 MHz reference clock up to the OC-12 (622.08 MHz) rate.

This feature is possible because the clock recovery system consists of two loops: a data loop which locks onto the incoming optical data stream, and a second reference loop which locks onto the optional external reference clock.

This optional feature is initiated by applying a Lock-to-Reference logic low signal to pin 2 (Lck Ref-) which switches the loop to the external reference clock and disables the received data outputs.

Pin 2 (Lck Ref-) can be driven from the Signal Detect pin 15 (SD) output or from other logic further upstream in the ATM interface which may be monitoring the quality of the received data stream.

Product Variations Available by Special Request

Transceiver Without CDR Function

The HFBR-5208 Transceiver is available in the smaller 1 x 9 pin-out package style without integral Clock and Data Recovery functions for those designers who prefer the flexibility of designing with a different partitioning of the physical layer interface.

Transceiver Specified for Wide Temperature Range Operation

The HFBR-5207 is specified for operation over normal commercial temperature range of 0°C to 70°C. The product has been characterized and is available with guaranteed performance over wider temperature ranges by special request.

Other Members of HP 622 Mb/s Product Family

- HFBR-5208, 1300 nm LED-based transceiver in 1 x 9 package for 500 m links with MMF cables
- CDX2622, 1300 nm laser-based transceiver with integral clock and data recovery in 2 x 9 package for links with SMF cables
- XMT5360-622, 1300 nm laser-based transmitter in pigtailed package for 2 km and 15 km links with SMF cables
- XMT5160-622, 1300 nm laser-based transmitter in pigtailed package for 40 km links with SMF cables
- RCV1201D-622, receiver in pigtailed package for 2 km, 15 km and 40 km links with SMF cables
- RGR1622, receiver with integral clock and data recovery in pigtailed packages for 2 km, 15 km and 40 km Links with SMF cables
- HP is planning to have a compatible SMF 1X9 solution available. Please contact your HP field sales representative for additional information.

Applications Information

Typical BER Performance of Receiver versus Input Optical Power Level

The HFBR-5207 transceiver can be operated at Bit-Error-Ratio conditions other than the required BER = 1 x 10^{-10} of the 622 MBd ATM Forum 622.08 Mbps Physical Layer Standard. The typical trade-off of BER versus Relative Input Optical Power is shown in Figure 2. The Relative Input Optical Power in dB is referenced to the Input Optical Power parameter value in the Receiver Optical Characteristics table. For better BER condition than 1 x 10^{-10}, more input signal is needed (+dB). For example, to operate the HFBR-5207 at a BER of 1 x 10^{-12}, the receiver will require an input signal approximately 0.6 dB higher than the -26 dBm level required for 1 x 10^{-10} operation, i.e. -25.4 dBm.

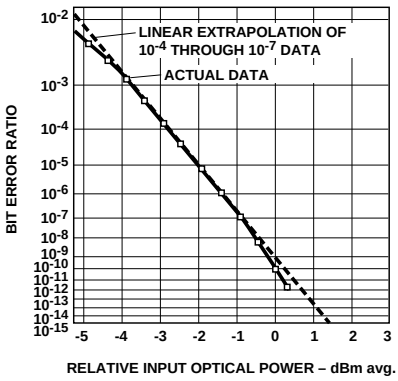


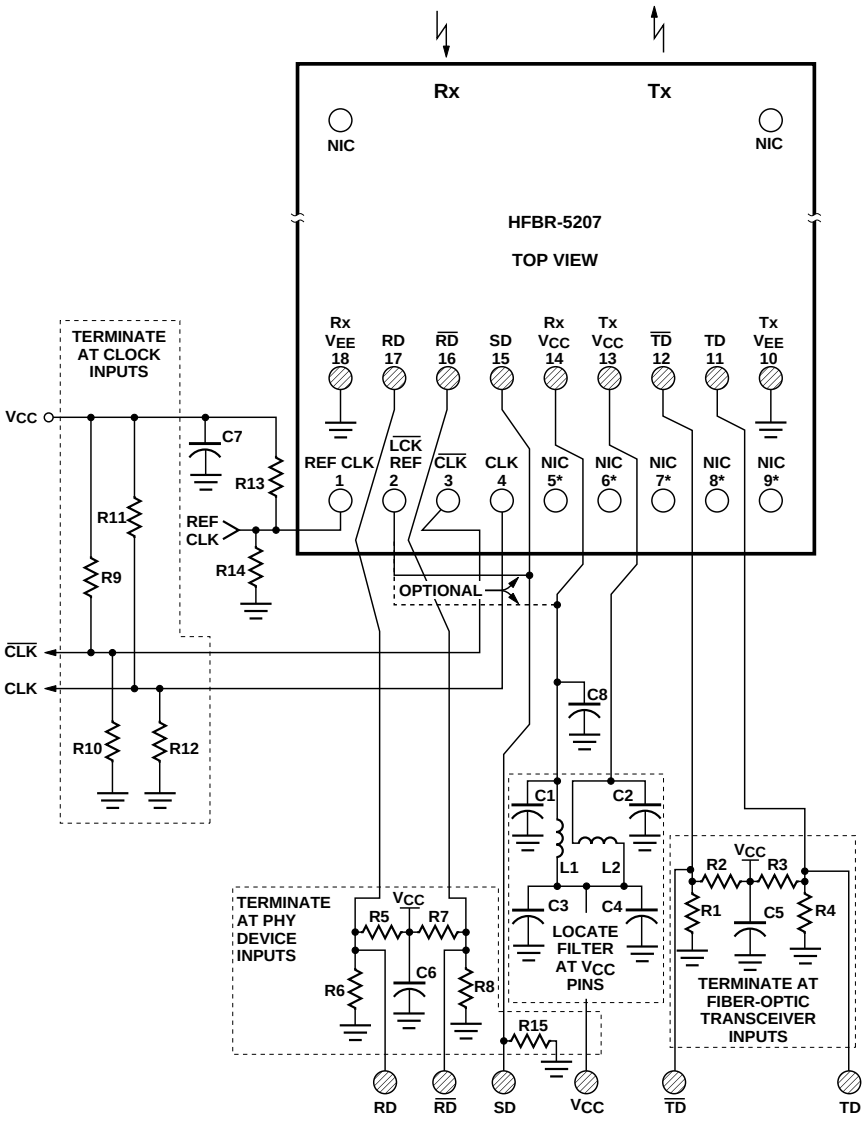
Figure 2. Relative Input Optical Power – dBm avg.

Recommended Circuit Schematic

When designing the HFBR-5207 circuit interface, there are a few fundamental guidelines to follow. For example, in the Recommended Circuit Schematic, Figure 3, the differential data lines should be treated as 50 Ohm Microstrip or stripline transmission lines. This will help to minimize the parasitic inductance and capacitance effects. Proper termination of the differential data and clock signals will prevent reflections and ringing which would compromise the signal fidelity and generate unwanted electrical noise. Locate termination at the received signal end of the transmission line. The length of these lines should be kept short and of equal length to prevent pulse-width distortion and data-to-clock timing skew from occurring. For the high-speed signal lines, differential signals should be used, not single-ended signals. These differential signals need to be loaded symmetrically to prevent unbalanced currents from flowing which will cause distortion in the signal.

Maintain a solid, low inductance ground plane for returning signal currents to the power supply. Multi-layer plane printed circuit board is best for distribution of V_{CC}, returning ground currents, forming transmission lines and shielding. Also, it is important to suppress noise from influencing the fiber-optic transceiver performance, especially the receiver and the clock recovery circuits. Proper power supply filtering of V_{CC} for this transceiver is accomplished by using the recommended, separate filter circuits shown in the Recommended Circuit Schematic figure for the transmitter and receiver sections. These filter circuits suppress V_{CC} noise of 50 mV peak-to-peak or less over a broad frequency range. This prevents receiver sensitivity degradation as well as false-lock or loss-of-lock in the clock recovery circuitry due to V_{CC} noise. It is recommended that surface-mount components be used. Use tantalum capacitors for the 10 µF capacitors and monolithic, ceramic bypass capacitors for the 0.1 µF capacitors. Also, it is recommended that a surface-mount coil inductor of 1 µH be used. Ferrite beads can be used to replace the coil inductors when using quieter V_{CC} supplies, but a coil inductor is recommended over a ferrite bead. Coils with a low, series dc resistance (<0.7 Ohms) and high, self-resonating frequency are recommended. All power supply components need to be placed physically next to the V_{CC} pins of the receiver and transmitter. Use a good, uniform ground plane with a minimum number of holes to provide a low-inductance ground current return path for the power supply currents.

In addition to these recommendations, Hewlett-Packard's Application Engineering staff is available for consulting on best layout practices with various vendors mux/demux, clock generator and clock recovery circuits. HP has participated in several reference design studies and is prepared to share the findings of these studies with interested customers. Contact your local HP sales representative to arrange for this service.



NOTES:
THE SPLIT-LOAD TERMINATIONS FOR PECL SIGNALS NEED TO BE LOCATED AT THE INPUT OF DEVICES RECEIVING THOSE PECL SIGNALS.
R1 = R4 = R6 = R8 = R10 = R12 = R14 = 130 Ω.
R2 = R3 = R5 = R7 = R9 = R11 = R13 = 82 Ω.
C1 = C2 = C3 = C5 = C6 = C7 = 0.1 µF.
C4 = C8 = 10 µF.
L1 = L2 = 1 µH COIL.
R15 = 10 kΩ.
NIC = NO INTERNAL CONNECTION
* FOR THIS MULTIMODE HFBR-5207 TRANSCEIVER, PINS 5-9 ARE NOT USED. FOR THE SINGLE-MODE CDX2622 TRANSCEIVER, PINS 5-9 ARE USED FOR LASER DIODE BIAS AND OPTICAL POWER MONITORING AS WELL AS TO PROVIDE A TRANSMITTER DISABLE FUNCTION.

Figure 3. Recommended Circuit Schematic.

Evaluation Circuit Boards

Evaluation circuit boards implementing this recommended circuit design are available from Hewlett-Packard's Application Engineering staff. Contact your local HP sales representative to arrange for access to one if needed.

Operation in -5.2 V Designs

For applications that require -5.2 Vdc power supply level for true ECL logic circuits, the HFBR-5207 transceiver can be operated with a V_{CC} = 0 Vdc and a V_{EE} = -5.2 Vdc. This transceiver is not specified with an operating, negative power supply voltage. The potential compromises that can occur with use of -5.2 Vdc power are that the absolute voltage states for V_{OH} and V_{OL} will be changed slightly due to the 0.2 V difference in supply levels. Also, noise immunity may be compromised for the HFBR-5207 transceiver because the ground plane is now the V_{CC} supply point. The suggested power supply filter circuit shown in the Recommended Circuit Schematic figure should be located in the V_{EE} paths at the transceiver supply pins. Direct coupling of the differential data and clock signals can be done between the HFBR-5207 transceiver and the standard ECL circuits. For guaranteed -5.2 Vdc operation, contact our local Hewlett-Packard Component Field Sales Engineer for assistance.

Recommended Solder and Wash Process

The HFBR-5207 is compatible with industry-standard wave or hand solder processes.

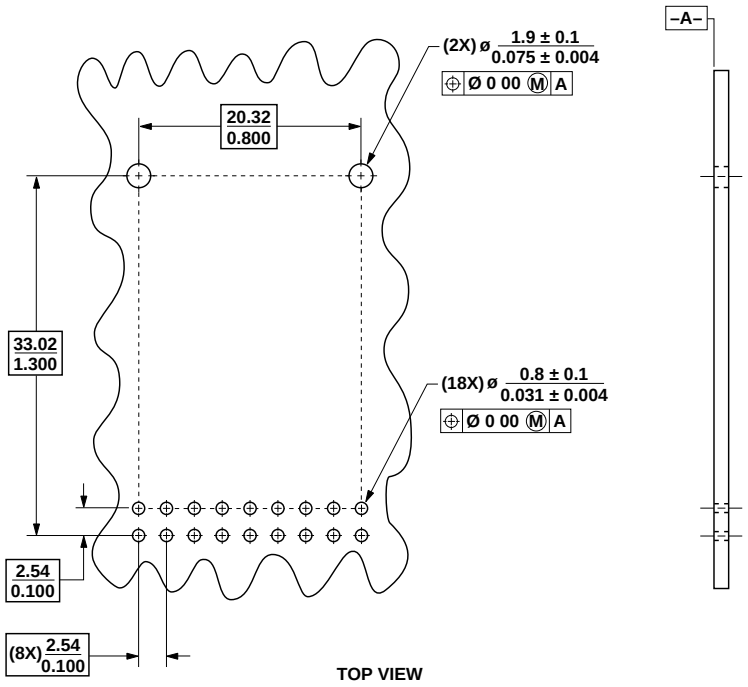


Figure 4. Recommended Board Layout Hole Pattern

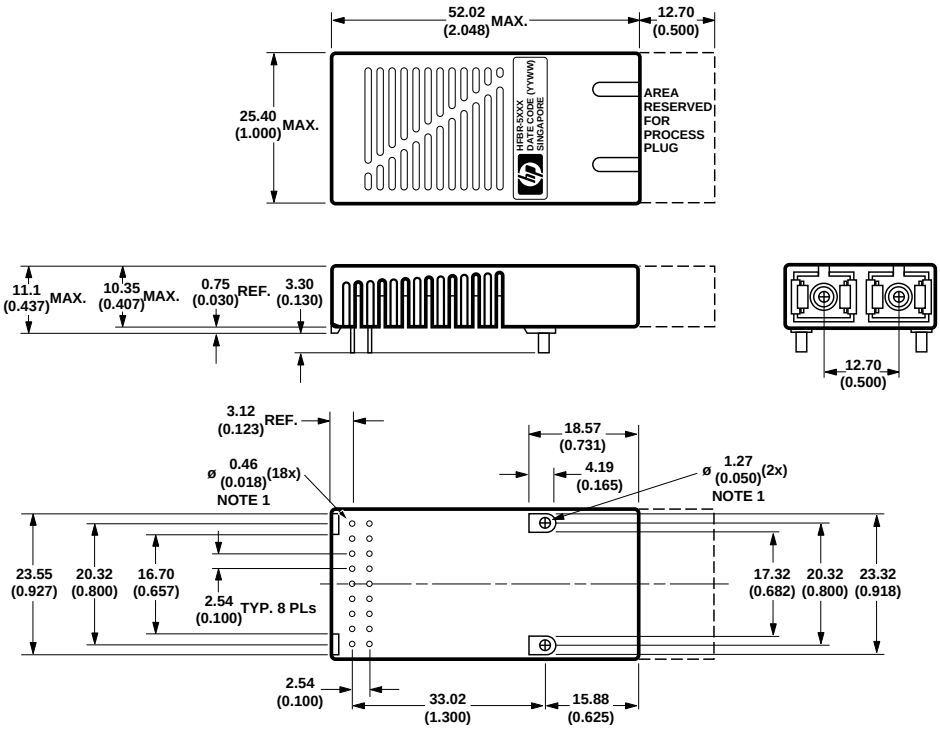
HFBR-5200 Process Plug

The HFBR-5207 transceiver is supplied with a process plug, the HFBR-5200, for protection of the optical ports with the Duplex SC connector receptacle. This process plug prevents contamination during wave solder and aqueous rinse as well as during handling, shipping or storage. It is made of high-temperature, molded, sealing material that will withstand 80°C and a rinse pressure of 50 lb/in^2.

Recommended Solder Fluxes and Cleaning/Degreasing Chemicals

Solder fluxes used with the HFBR-5207 fiber-optic transceiver should be water-soluble, organic solder fluxes. Some recommended solder fluxes are Lonco 3355-11 from London Chemical West, Inc. of Burbank, CA, and 100 Flux from Alpha-metals of Jersey City, NJ.

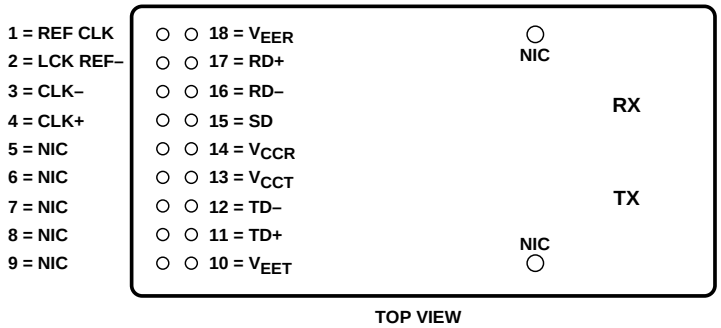
Recommended cleaning and degreasing chemicals for the HFBR-5207 are alcohols (methyl, isopropyl, isobutyl), aliphatics (hexane, heptane) and other chemicals, such as soap solution or naphtha. Do not use partially halogenated hydrocarbons for cleaning/degreasing. Examples of chemicals to avoid are 1,1.1 trichloroethane, ketones (such as MEK), acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride or N-methylpyrolldone.



NOTE 1: SOLDER POSTS AND ELECTRICAL PINS ARE TIN/LEAD PLATED.

DIMENSIONS ARE IN MILLIMETERS (INCHES).

HFBR-5207 Package Outline



TOP VIEW

NIC = NO INTERNAL CONNECTION

Figure 5. Package Outline Drawing and Pinout

Regulatory Compliance

These transceiver products are intended to enable commercial system designers to develop equipment that complies with the various regulations governing certification of Information Technology Equipment. See the Regulatory Compliance Table for details. Additional information is available from your Hewlett-Packard sales representative.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas.

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the duplex SC connector receptacle is exposed to the outside of the equipment chassis, it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Hewlett-Packard will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

The HFBR-5207 EMI has been characterized without a chassis enclosure to demonstrate the robustness of the parts integral shielding. Performance of a system containing these transceivers within a well designed chassis is expected to be better than the results of these tests with no chassis enclosure.

Immunity

Equipment utilizing these HFBR-5207 transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers, with their integral shields, have been characterized without the benefit of a normal equipment chassis enclosure and the results are reported below. Performance of a system containing these transceivers within a well-designed chassis is expected to be better than the results of these tests without a chassis enclosure.

Regulatory Compliance – Typical Performance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.4	Class 1 (>1000 volts)
Electrostatic Discharge (ESD) to the Duplex SC Receptacle	Variation of IEC 801-2	Typically withstand at least 25 kV without damage when the Duplex SC Connector Receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMI)	FCC Class B CENELEC EN55022 Class B (CISPR 22B) VCCI Class 2	Typically provide a 4 dB margin to FCC Class B and a 1 dB margin to the other noted standard limits when tested at a certified test range with the transceiver mounted to a circuit card without a chassis enclosure at frequencies up to 1 GHz. Margins above 1 GHz are dependent on customer board and chassis designs.
Immunity	Variation of IEC 801-3	Typically show no measurable effect from a 3 V/m field swept from 10 to 450 MHz applied to the transceiver when mounted to a circuit card without a chassis enclosure.

The HFBR-5207 LED transmitters are classified as IEC 825-1 Accessible Emission Limit (AEL) Class 1 based upon the current proposed draft scheduled to go into effect on January 1, 1997. AEL Class 1 LED devices are considered eye safe.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Storage Temperature	T_S	-40		85	℃	
Lead Soldering Temperature	T_{SOLD}			260	℃	
Lead Soldering Time	t_{SOLD}			10	sec.	
Supply Voltage	V_{CC}	-0.5		7.0	V	
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Transmitter Differential Input Voltage	V_D			1.6	V	Note 1
Output Current	I_O			50	mA	
Relative Humidity	RH	0		95	%	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Ambient Operating Temperature	T_A	0		70	℃	
Supply Voltage	V_{CC}	4.75		5.25	V	
Power Supply Rejection	PSR		50		mV_{P-P}	Note 2
Transmitter Data Input Voltage-Low	V_{IL}-V_{CC}	-1.810		-1.475	V	Note 3
Transmitter Data Input Voltage-High	V_{IH}-V_{CC}	-1.165		-0.880	V	Note 3
Transmitter Differential Input Voltage	V_D	0.3		1.6	V	
Receiver Lck Ref- & Ref Clk Single-Ended Input Voltage-Low	V_{IL}-V_{CC}	-1.950		-1.620	V	Note 3
Receiver Lck Ref- & Ref Clk Single-Ended Input Voltage-High	V_{IH}-V_{CC}	-1.045		-0.740	V	Note 3
Clock and Data Output Load	R_{CL}/R_{DL}	50			Ω	Note 4
Signal Detect Output Load	R_{SDL}	7	10		kΩ	Note 5

Notes:

1. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs without damaging the ESD protection circuit.
2. Tested with a 50 mV_{P-P} sinusoidal signal in the frequency range from 500 Hz to 450 MHz imposed on the V_{CC} supply with the recommended power supply filter in place, see Figure 3. Typically less than a 0.25 dB change in sensitivity is experienced.
3. Compatible with 10K, 10KH and 100K ECL and PECL output signals.
4. The outputs are terminated to V_{CC} - 2 V.
5. The output is terminated to ground.

Transmitter Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CCT}		150	200	mA	Note 6
Power Dissipation	P_{DIST}		0.75	1.05	W	
Data Input Current-Low	I_{IL}	-350	0		µA	
Data Input Current-High	I_{IH}		16	350	µA	

Receiver Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CCR}		225	300	mA	
Power Dissipation	P_{DISR}		1.02	1.49	W	Note 7
Data and Clock Output Voltage-Low	V_{OL}-V_{CC}	-1.950		-1.620	V	Note 8
Data and Clock Output Voltage-High	V_{OH}-V_{CC}	-1.045		-0.740	V	Note 8
Data and Clock Output Rise Ti9	t_r	0.2	0.3	0.51	ns	Note 9
Data and Clock Output Fall Time	t_f	0.2	0.3	0.51	ns	Note 9
Signal Detect Output Voltage-Low (De-asserted)	V_{OL}-V_{CC}	-1.950		-1.620	V	Note 8
Signal Detect Output Voltage-High (Asserted)	V_{OH}-V_{CC}	-1.045		-0.740	V	Note 8
Signal Detect Assert Time (off to on)	t_{SDA}			100	µs	Note 10
Signal Detect De-asserted Time (on to off)	t_{SDD}			100	µs	Note 11
Ref Clk & Lck Ref-Input Current-Low	I_{IL}	-500	-20		µA	
Ref Clk & Lck Ref-Input Current-High	I_{IH}		80	500	µA	

Notes:

6. The I_{CC} value is held nearly constant to minimize unwanted electrical noise from being generated and conducted or emitted into neighboring circuitry.
7. Power dissipation value is the power dissipated in the receiver itself. It is calculated as the sum of the products of V_{CC} and I_{CC} minus the sum of the products of the output voltages and load currents.
8. These outputs are compatible with 10K, 10KH and 100K ECL and PECL inputs.
9. These are 20% - 80% values.
10. The Signal Detect output will change from logic “0” to “1” within 100 µs of a step transition in input optical power from no light to -26 dBm avg.
11. The Signal Detect output will change from logic “1” to “0” within 100 µs of a step transition in input optical power from -28 dBm avg. to no light.

Transmitter Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Output Optical Power 62.5/125 µm, NA = 0.275 fiber	P_O (BOL) P_O (EOL)	-19 -20		-14 -14	dBm avg.	
Output Optical Power 50/125 µm, NA = 0.20 fiber	P_O (BOL) P_O (EOL)		-21.5 -22.5	-14 -14	dBm avg.	
Output Optical Power at Logic "0" State	P_O ("O")		-60		dBm avg.	
Optical Extinction Ratio		10	46		dB	
Center Wavelength	λc	1270	1330	1380	nm	
Spectral Width-FWHM	σ		136	200	nm	
Optical Rise/Fall Times	t_r/t_f		0.9	1.25	ns	Note 12
Overshoot				25	%	
Systematic Jitter Contributed by the Transmitter	SJ		0.04	0.23	ns p-p	Note 13
Random Jitter Contributed by the Transmitter	RJ		0.0	0.10	ns p-p	Note 14

Receiver Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Input Optical Power	P_{IN}	-26		-14	dBm avg.	Note 15
Input Optical Wavelength	λ	1270		1380	nm	
Output Static Clock/Data Alignment Jitter	$SAJ_{C/D}$	-120	± 25	120	ps	
Output Clock Random Jitter	RJ_C		60	110	ps p-p	
Signal Detect-Asserted	P_A	P_D+1.0 dB		-28	dBm avg.	
Signal Detect-De-asserted	P_D	-45			dBm avg.	
Signal Detect-Hysteresis	P_A - P_D	1.0			dB	

Notes:

12. These are 10-90% values.

13. This contributed jitter allows the incoming data signal to contribute additional jitter without violating the 0.4 ns maximum allowed optical output systematic jitter per the ATM Forum specification for this MMF interface.

14. This contributed jitter allows the incoming data signal to contribute additional jitter without violating the 0.15 ns maximum allowed optical output random jitter per the ATM Forum specification for this MMF interface.

15. The sensitivity is provided at a BER of 1 x 10^{-10} or better with an input signal consisting of 622.08 Mb/s, 2^{23} - 1 PRBS pattern sections with 72 "1"s and 72 "0"s inserted per ITU-T G.958 Appendix I. The transmitter is operating at the 622.08 Mb/s rate during the test to simulate any cross-talk effects between the transmitter and receiver sections of the transceiver. The output signal is re-timed data.

Table 1. Pin Out Table

Pin	Symbol	Functional Description
Mounting Studs		The mounting studs are provided for transceiver mechanical attachment to the circuit board. They are embedded in the non-conductive plastic housing and are not connected to the transceiver internal circuit. They should be soldered into plated-through holes on the printed circuit board.
1	Ref Clk	Reference Clock - Optional Feature Reference Clock can be used as an optional, internally generated local receiver clock when the Input Optical Signal is disrupted. See Pin 2 Lck Ref-description. This input is not required for the normal operation of the Clock recovery circuit. This is a single-ended PECL input. If this Reference Clock input is used, provide a 19.44 MHz external reference clock signal and terminate at this input pin with standard PECL techniques. If this Reference Clock input is not used, leave the input open-circuited. With the input open-circuited, an internal pull-down resistor will bias this input to a low-state condition.
2	Lck Ref-	Lock-to-Reference Clock Bar - Optional Feature Lock-to-Reference Clock Bar can be used to help manage the performance of the receiver when the Input Optical Signal is disrupted. When used, it places the received data outputs in static states and it triggers an internally generated local receiver clock to be output on Clk/Clk- in substitution of recovered clock. This is a single-ended PECL input. For normal operation of the transceiver, connect this Lock-to-Reference-bar input to V_{CC} or a PECL high-state (V_{IH}) which causes the internal CDR circuit to output recovered differential clock on Clk/Clk- and re-timed differential data on RD/RD-. For optional use to make static the received data outputs and to output the internally generated local receiver clock, connect Lck Ref- input to a PECL low-state (V_{IL}), or leave this input open-circuited. When this is done it will cause: 1) the Received Data outputs to change to static PECL logic levels (RD = V_{OL} and RD- = V_{OH}), 2) the internal CDR circuit to switch over to using the external reference clock, if provided, as the timing source to generate a 622.08 Mb/s clock output on Clk/Clk-. If the feature is used, one way to implement it is to connect this pin to Signal Detect directly with a single pull-down resistor of 10 kΩ to ground. If this Lock-to-Reference feature is not used, this pin must be connected directly to V_{CC} or a PECL high-state to disable it.
3	Clk-	Received Recovered Clock Out Bar See pins 1 & 2 for optional, local generated clock output. The rising edge occurs coincident with the edges of the Received Data output. The falling edge occurs in the middle of the Received Data baud period. Terminate this high-speed, complementary, differential clock output with standard PECL techniques at the clock input point of the follow-on device. If this clock output is not used, leave it open-circuited with no printed circuit board trace attached to this output pin.

Table 1. Pin Out Table (continued)

Pin	Symbol	Functional Description
4	Clk+	Received Recovered Clock Out See pins 1 & 2 for optional, local generated clock output. The falling edge occurs coincident with the edges of the Received Data output. The rising edge occurs in the middle of the Received Data baud period. Terminate this high-speed, complementary, differential clock output with standard PECL techniques at the clock input point of the follow-on device. If this clock output is not used, leave it open-circuited with no printed circuit board trace attached to this output pin.
5	NIC	Pins 5 through 9 are not connected to the transceiver internal circuit. They are reserved for use with the complementary Hewlett-Packard CDX2622 single mode fiber-optic transceiver which is provided in the same 2 x 9 package style. See the Hewlett-Packard CDX2622 data sheet for full details on the use of these pins.
6	NIC	
7	NIC	
8	NIC	
9	NIC	
10	Veet	Transmitter Signal Ground Directly connect this pin to the transmitter signal ground plane.
11	TD+	Transmitter Data In Terminate this high-speed, differential Transmitter Data Bar input with standard PECL techniques at the transmitter input pin.
12	TD-	Transmitter Data In Bar Terminate this high-speed, differential Transmitter Data input with standard PECL techniques at the transmitter input pin.
13	V_{CCT}	Transmitter Power Supply Provide +5 Vdc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCT} pin.
14	V_{CCR}	Receiver Power Supply Provide +5 Vdc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCR} pin.
15	SD	Signal Detect Normal input optical power levels to the receiver result in a logic “1” output (Asserted). Low input optical power levels to the receiver result in a fault indication shown by a logic “0” output (De-asserted). Signal Detect is a single-ended, low-power, PECL output. Since SD is a low-power PECL output, complete the interconnection of SD output with other PECL inputs using a 10 kΩ pull-down resistor to V_{EE} to allow biasing of this interconnection. Do not load this SD output with standard PECL, 50 Ω to Vcc-2V, termination. If Signal Detect output is not used, leave it open-circuited. This Signal Detect output can be used to drive a PECL input on an upstream circuit, such as, Signal Detect input, Loss of Signal-bar input, or to optionally drive the Lock-to-Reference-bar input (pin 2) of this transceiver.

Table 1. Pin Out Table (continued)

Pin	Symbol	Functional Description
16	RD-	Re-timed Receiver Data Out Bar Terminate this high-speed, differential, PECL output with standard PECL techniques at the follow-on device input pin.
17	RD+	Re-timed Receiver Data Out Terminate this high-speed, differential, PECL output with standard PECL techniques at the follow-on device input pin.
18	V_{EER}	Receiver Signal Ground Directly connect this pin to receiver signal ground plane.

For technical assistance or the location of your nearest Hewlett-Packard sales office, distributor or representative call:

Americas/Canada: 1-800-235-0312 or 408-654-8675

Far East/Australasia: (65) 290-6305

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