

# Quad high-speed differential line receivers

**AM26LS32/  
AM26LS33**

## DESCRIPTION

The AM26LS32 and AM26LS33 are quad line receivers designed to meet all of the requirements of RS-422 and RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The AM26LS32 features an input sensitivity of  $\pm 200\text{mV}$  over the common mode input range of  $\pm 7\text{V}$ .

The AM26LS33 features an input sensitivity of  $\pm 500\text{mV}$  over the common mode input voltage range of  $\pm 15\text{V}$ .

The AM26LS32 and AM26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-State outputs with  $8\text{mA}$  sink capability and incorporate a fail-safe input-output relationship which forces the outputs high when the inputs are open.

## FEATURES

- Input voltage range of  $15\text{V}$  (differential or common mode) on AM26LS33;  $7\text{V}$  (differential or common mode) on AM26LS32
- $\pm 0.2\text{V}$  sensitivity over the input voltage range on AM26LS32
- $\pm 0.5\text{V}$  sensitivity on AM26LS33
- $6\text{k}\Omega$  minimum input impedance
- The AM26LS32 meets all the requirements of RS-422 and RS-423

## ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	$0^\circ\text{C}$ to $+70^\circ\text{C}$	AM26LS32CN	0406C
16-Pin Small Outline (SO) Package	$0^\circ\text{C}$ to $+70^\circ\text{C}$	AM26LS32CD	0005D
16-Pin Plastic Dual In-Line Package (DIP)	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	AM26LS32IN	0406C
16-Pin Small Outline (SO) Package	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	AM26LS32ID	0005D
16-Pin Plastic Dual In-Line Package (DIP)	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	AM26LS32MN	0406C
16-Pin Plastic Dual In-Line Package (DIP)	$0^\circ\text{C}$ to $+70^\circ\text{C}$	AM26LS33CN	0406C
16-Pin Small Outline (SO) Package	$0^\circ\text{C}$ to $+70^\circ\text{C}$	AM26LS33CD	0005D
16-Pin Plastic Dual In-Line Package (DIP)	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	AM26LS33IN	0406C
16-Pin Small Outline (SO) Package	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	AM26LS33ID	0005D
16-Pin Plastic Dual In-Line Package (DIP)	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	AM26LS33MN	0406C

## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Power supply	7	V
$V_{IN}$	Power supply	7	V
	Output sink current	50	mA
	Common mode range	$\pm 25$	V
$V_{TH}$	Differential input voltage	$\pm 25$	V
$T_{STG}$	Storage temperature range	$-65$ to $+150$	$^\circ\text{C}$

## DISSIPATION OPERATING TABLE

PACKAGE	POWER DISSIPATION	DERATING FACTOR	ABOVE $T_A$
N	1,275mW	10.2mW/ $^\circ\text{C}$	$25^\circ\text{C}$
D	1,262W	10.1mW/ $^\circ\text{C}$	$25^\circ\text{C}$

■ 7110826 0078829 718 ■

## Quad high-speed differential line receivers

AM26LS32/  
AM26LS33

## DC AND AC ELECTRICAL CHARACTERISTICS

 $V_{CC} = 5.0V \pm 10\%$  for AM26LS32/33MX,  $V_{CC} = 5.0V \pm 5\%$  for AM26LS32/33CX and AM26LS32/33IX over operating temperature range unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
			AM26LS32/33				
			Min	Typ <sup>1</sup>	Max		
$V_{TH}$	Differential input voltage	$V_{OUT} = V_{OL}$ or $V_{OH}$ AM26LS32, $-7V \leq V_{CM} \leq +7V$	-0.2		0.2	V	
		AM26LS33, $-15V \leq V_{CM} \leq +15V$	-0.5		0.5		
$R_{IN}$	Input resistance	$-15V \leq V_{CM} \leq +15V$ (One input AC ground)	6.0	9.8		$k\Omega$	
$I_{IN}$	Input current (under test)	$V_{IN} = +15V$ Other input $-15V \leq V_{IN} \leq +15V$			2.3	mA	
$I_{IN}$	Input current (under test)	$V_{IN} = -15V$ Other input $+15V \leq V_{IN} \leq -15V$			-2.8	mA	
$V_{OH}$	Output HIGH voltage	$V_{CC} = \text{Min.}$ , $I_{OH} = -440\mu A$	Com'l	2.7	3.4	V	
		$\Delta V_{IN} = +1.0V$	Mil	2.5	3.4		
$V_{OL}$	Output LOW voltage	$V_{CC} = \text{Min.}$ , $V_{ENABLE} = 0.8V$ $\Delta V_{IN} = +1.0V$	$I_{OL} = 4.0\text{mA}$		0.3	0.4	
			$I_{OL} = 8.0\text{mA}$			0.45	
$V_{IL}$	Enable LOW voltage					0.8	
$V_{IH}$	Enable HIGH voltage			2.0		V	
$V_I$	Enable clamp voltage	$V_{CC} = \text{Min.}$ , $I_{IN} = -18\text{mA}$				-1.5	
$I_O$	Off state (high impedance) output current	$V_{CC} = \text{Max.}$	$V_O = 2.4V$		20	$\mu A$	
			$V_O = 0.4V$		-20		
$I_{IL}$	Enable LOW current	$V_{IN} = 0.4V$			-0.2	-0.36	
$I_{IH}$	Enable HIGH current	$V_{IN} = 2.7V$			0.5	20	
$I_I$	Enable input HIGH current	$V_{IN} = 5.5V$			1	100	
$I_{SC}$	Output short circuit current	$V_{CC} = \text{Max.}$ , $\Delta V_{IN} = +1V$ , $V_{OUT} = 0V$	-15	-60	-85	mA	
$I_{CC}$	Power supply current	$V_{CC} = \text{Max.}$ ; All $V_{IN} = \text{GND}$ outputs disabled		52	70	mA	
$V_{HYST}$	Input hysteresis	$T_A = 25^\circ C$ , $V_{CC} = 5.0V$ , $V_{CM} = 0V$	AM26LS32	120		mV	
			AM26LS33	120			
$t_{PLH}$	Input to output	$T_A = 25^\circ C$ , $V_{CC} = 5.0V$ $C_L = 15\text{pF}$ (see test condition)		10	25	ns	
$t_{PHL}$	Input to output	$T_A = 25^\circ C$ , $V_{CC} = 5.0V$ $C_L = 15\text{pF}$ (see test condition)		10	25	ns	
$t_{LZ}$	Enable to output	$T_A = 25^\circ C$ , $V_{CC} = 5.0V$ $C_L = 5\text{pF}$ (see test condition)		15	30	ns	
$t_{HZ}$	Enable to output	$T_A = 25^\circ C$ , $V_{CC} = 5.0V$ $C_L = 5\text{pF}$ (see test condition)		12	22	ns	
$t_{ZL}$	Enable to output	$T_A = 25^\circ C$ , $V_{CC} = 5.0V$ $C_L = 15\text{pF}$ (see test condition)		8	22	ns	
$t_{ZH}$	Enable to output	$T_A = 25^\circ C$ , $V_{CC} = 5.0V$ $C_L = 15\text{pF}$		9	22	ns	

## NOTE:

- All typical values are  $T_A = 25^\circ C$ ,  $V_{CC} = 5.0V$ .

## Quad high-speed differential line receivers

AM26LS32/  
AM26LS33

## FUNCTION TABLE (EACH RECEIVER)

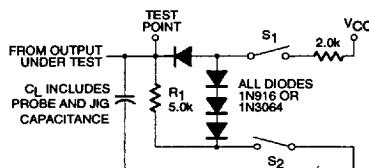
DIFFERENTIAL INPUT	ENABLES E E		OUTPUT
$V_{ID} \geq V_{TH}$	H	X	H
	X	L	H
$V_{TL} \leq V_{ID} \leq V_{TH}$	H	X	?
	X	L	?
$V_{ID} \leq V_{TL}$	X	L	L
	H	X	X
X	L	H	Z

## NOTES:

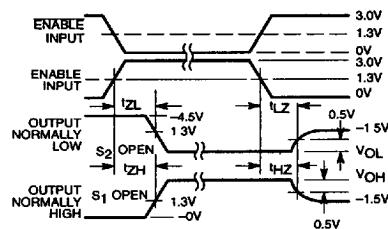
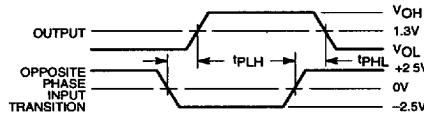
H = High level, L = Low level, X = irrelevant

Z = High impedance (off), ? = Indeterminate

E = Enable, E = Enable



Load Test Circuit for 3-State Outputs

Enable and Disable Times<sup>2, 3, 4</sup>Propagation Delay<sup>1, 4</sup>

## NOTES:

1. Diagram shown for Enable Low.
2. Enable is tested with Enable High, Enable is tested with Enable Low.
3. S<sub>1</sub> and S<sub>2</sub> of Load Circuit are closed except where shown.
4. Pulse Generator for All Pulses. Rate  $\leq 1.0\text{MHz}$ ,  $Z_O = 50\Omega$ ;  $t_r \leq 15\text{ns}$ ;  $t_f \leq 6.0\text{ns}$