82C614
DATA BOOK

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Revision 1.6

CHIPS AND TECHNOLOGIES, INC.
3050 ZANKER ROAD
SAN JOSE, CA 95134
(408) 434-0600

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1.0. Overview

The 82C614 is a chip for the MicroChannel Architecture that provides bus master capabilities to peripherals which would normally use the system board DMA controller. The advantage of doing this is greatly increased bandwidth (at least double for any given system) which means more time is available on the MicroChannel for other tasks. It also allows 4 concurrently operating DMA devices to share the same MicroChannel arbitration level.

Some of the possible applications for the 82C614 are as follows:

- SCSI Host Adapters
- High Performance Hard Disk Controllers
- Multiple high speed serial adapters
- High Performance LAN adapters
- Graphics adapters
- Modem and FAX adapters
- High Speed Printer Controllers
- ISDN adapters

The goal of this chip is to make it easy and cost effective enough that board designers will make almost every high-level function MicroChannel adapter a bus master instead of a DMA slave.

The 82C614 is a single 160 pin device which requires an absolute minimum of external logic to interface to both the MicroChannel and the local "Adapter Side." The 82C614 provides the following 3 major functions for a peripheral board:

- Complete interface between the MicroChannel and peripheral devices or memory. This includes converting the MicroChannel signals to read and write strobes which are more easily used by peripheral chips, adding programmed wait states, providing chip selects, and interrupt routing. The 82C614 also contains the data buffers between the MicroChannel and the peripheral devices.
- Four DMA controllers with internal FIFO buffers. The FIFOs allow the data to be read from or written to the MicroChannel in blocks using burst mode and streaming data cycles (if supported by the system), while being written to or read from the local peripheral at what ever rate it requires. This reduces the amount of MicroChannel bandwidth required by the peripheral. On the local side, DMA REQuest and DMA ACKnowledge signals are provided to interface directly to the peripheral devices. In addition, a DMA address may be provided on the local side to DMA to or from I/O ports and memory areas. On the MicroChannel side the 82C614 performs the DMA transfers as a bus master.

- The 82C614 contains all of the POS registers for the adapter card. It decodes the memory and/or I/O ranges used by the local peripherals and provides POS relocation for these decodes, allowing multiple boards (up to 8) of identical design to appear in the same system.

1.1 MicroChannel Interface

The 82C614 contains a complete interface to the MicroChannel that requires only one external TTL buffer. It arbitrates for use of the bus, and when granted the bus it generates and drives all of the necessary bus signals. The 82C614 supports a 32 bit address bus and a 16 bit data bus. The data bus has support for parity checking and generation.

The 82C614 supports fairness and burst transfer modes. It also contains a preempt timer that will transfer as much data as possible before relinquishing the bus.

The 82C614 also supports 100 ns streaming data transfers, thus allowing a maximum peak transfer rate of 20 megabytes per second. This compares favorably with the maximum transfer rate of 5 megabytes per second using the system board DMA controller in today's MicroChannel machines. Even without streaming data transfers, the 82C614 can transfer data at 10 megabytes per second - double the current DMA bandwidth.

For normal operation (as opposed to setup and configuration), the 82C614 is intended to be programmed from the MicroChannel Host Processor.

The 82C614 can cause an interrupt on the MicroChannel in response to a number of programmed conditions, or in response to a local interrupt input. It can also cause -CHCK to be asserted in response to a serious error. This can be due to internally detected conditions or in response to the local error input.

1.2 Local Interface

The goal of the local interface is to provide a set of signals that look as much like the AT bus as possible, allowing the designer to easily convert existing designs. This also works out well for most peripheral chips. In addition to the standard signals, a group of Multifunction Pins allows further "customizing" of the local bus interface as required by an individual adapter card design.

The local bus interface supports a full 16 bit data path. In addition, 16 local address lines are available, multiplexed with the data lines.

The 82C614 contains four programmable decodes which allow any type of MicroChannel access to produce a local side peripheral chip select. These programmable decodes have relocation control structures that are optimized for I/O, memory, and BIOS ROM spaces. Relocation can be controlled with the POS bits. Each decode can be programmed to respond to I/O cycles from the MicroChannel. One of the decodes may be programmed to respond to a memory range anywhere in the 32 bit address space, another may respond to a memory range in the bottom 1M only. They can be programmed to respond to Read cycles, Write cycles, or both. Each address bit may be compared to a 0, 1, or masked for a "don't care" condition. The number of wait states and the data size of the peripheral may also be programmed.

The 82C614 also contains 8 Multifunction Pins or MFPs. The board designer can customize the interface to fit the peripheral chips or functions being used with these pins. Some of the functions

which may be programmed include AEN, DMA Terminal Count, POS bits, local CPU interface, etc.

1.3 DMA Channels

The 82C614 contains 4 independent DMA channels, but uses only one ARB level on the bus. This allows multiple devices to be resident on the same adapter card. It also allows "full duplex" DMA where one channel is dedicated to the "receive" function and another to the "transmit" function. This greatly reduces the software overhead on the host CPU and allows for greater system throughput since data can flow in both directions at the same time. This is only possible with a bus master implementation.

Each DMA channel has a DREQ and DACK line to interface to the peripheral chip. A local address may be provided for the peripheral access.

The 82C614 also supports linked list array chaining. This allows a series of commands to be placed in memory for the DMA Channel to execute. Once the list of commands is set up, all the host processor needs to do is issue a "start" command and the 82C614 will execute the entire sequence without any further processor intervention. Each entry of the linked list table provides the source and destination addresses, byte count, direction of transfer, and a pointer to the next linked list entry. The linked list entries are read from MicroChannel memory.

1.4 FIFO Buffers

In order to minimize the time spent on the bus, the 82C614 contains 80 bytes of FIFO buffer. This buffer may be allocated to the DMA channels in several ways to optimize for the application. All DMA transfers between the local devices and the MicroChannel go through the FIFO.

To minimize the time on the bus and prevent extra arbitration cycles from occurring, transfers on the MicroChannel side of the buffer may be non-contiguous. This means that if there is data waiting to be transferred for more than one DMA channel, all the data may be transferred in one burst even though the addresses are non-contiguous.

The buffer has programmable threshold levels to select the amount of space left in the FIFO before initiating a transfer on the MicroChannel. When transferring from the local side to the MicroChannel side, the buffer also has programmable "Flush" timers so that if the threshold has not been reached in a certain time, the transfer will be initiated anyway. This prevents data from being stuck in the buffer if the peripheral does not send data very often.

1.5 Initialization ROM

Since the 82C614 requires more configuration bits than are supported by the POS mechanism, a facility is provided to download these bits from a small PROM located on the board. If the adapter board contains a BIOS ROM, the Initialization data may be contained in a section of it.

The board designer programs the INIT ROM to customize the 82C614 to the application. The INIT ROM provides the POS ID bytes, the I/O address for the 82C614's registers, the addresses (memory and/or I/O) for the local peripherals, and other configuration information.

2.0 REGISTERS

The 82C614 registers occupy a block of 256 addresses in the MicroChannel I/O space. The 82C614 registers may be located anywhere in the I/O space, on a 256 port boundary. The I/O port range is determined by the INIT ROM and POS bits. A8-12 are set by the INIT ROM. POS register 2 defines A13-15 of the I/O address. This provides 8 different I/O locations, allowing up to 8 boards of identical design (same INIT ROM) to reside in the same system. In order to comply with the Assignable I/O Address mechanism, the INIT ROM should program A8-9 as 0s and A10-12 as 1s. The value written by the INIT ROM may be overwritten by an Extended POS access.

Within the 256 port block, there are 5 address ranges which are not used by the 82C614 and may be used by the local peripherals connected to the 82C614. There is one block of 32 ports and 4 blocks of 8 ports each available. The "Fixed Decodes" provide chip selects for these areas, and are available through the multifunction pins. When a peripheral uses a Fixed Decode, its I/O is addressed as if it were 82C614 registers. The 82C614 will respond to accesses to the entire 256 port range regardless of whether the fixed decodes are used.

2.1 Register Summary

RW = Read/Write
RO = Read Only
WO = Write Only

I/O Address	RW/ RO/WO	INIT ROM Load	Function
xx00	RO	N	Revision code of chip.
xx01	RO	N	Features supported by chip.
xx02	RW	Y	Revision code of board.
xx03	RW	Y	Features supported by board.
xx04	RW	Y	MicroChannel side Configuration Register.
xx05	RW	Y	Local Bus Configuration Register.
xx06	RW	Y	I/O address of 82C614 register set.
xx07	RW	Y	CDSLFBK, Card Size Indicator.
xx08	RW	Y	Fixed Decode Configuration.
xx09	RW	Y	DMA Implicit I/O wait states.
xx0A	RW	Y	CHCK Interrupt Enable Register.
xx0B	RW	Y	CHCK status Register.
xx0C	RW	Y	Interrupt Enable Register.
xx0D	RW	Y	Interrupt status Register.
xx0E	RW	Y	Reserved.
xx0F	RW	Y	Multifunction pin I/O Port.

2.1 Register Summary (continued)

I/O Address	RW/ RO/WO	INIT ROM Load	Function
xx10-xx17	-	-	Reserved for future 82C614 Registers requiring INIT ROM setup.
xx18	RW	Y	POS 0 alternate addressing (for loading by INIT ROM).
xx19	RW	Y	POS 1 alternate addressing (for loading by INIT ROM).
xx1A-xx1B	-	-	Reserved for future 82C614 Registers requiring INIT ROM setup.
xx1C-xx1F	RW	Y	Multifunction Pin assignment.
xx20-xx23	RW	Y	Decode 0 Address Registers.
xx24-xx27	RW	Y	Decode 0 Mask Registers.
xx28-xx2B	RW	Y	Decode 1 Address Registers.
xx2C-xx2F	RW	Y	Decode 1 Mask Registers.
xx30-xx31	RW	Y	Decode 2 Address Registers.
xx32-xx33	RW	Y	Decode 2 Mask Registers.
xx34-xx35	RW	Y	Decode 3 Address Registers.
xx36-xx37	RW	Y	Decode 3 Mask Registers.
xx38-xx3F	RW	Y	Decode 0-3 control.
xx40	RW	N	Buffer Testing Control Register.
xx41	RW	N	Buffer Testing Data Register.
xx42-xx47	RW	N	POS2-7 Alternate locations.
xx48-xx4F	-	N	Reserved.
xx50-xx5F	-	N	Reserved for future 82C614 registers not requiring INIT ROM setup.
xx60-xx7F	RW	N	Decode #8 I/O space. Mapped to the local side.
xx80-xx97	RW	N	DMA Controller 0 Registers (some regs are RO or WO).
xx98-xx9F	RW	N	Decode #4 I/O space. Mapped to the local side.
xxA0-xxB7	RW	N	DMA Controller 1 Registers.
xxB8-xxBF	RW	N	Decode #5 I/O space. Mapped to the local side.
xxC0-xxD7	RW	N	DMA Controller 2 Registers.
xxD8-xxDF	RW	N	Decode #6 I/O space. Mapped to the local side.
xxE0-xxF7	RW	N	DMA Controller 3 Registers.
xxF8-xxFF	RW	N	Decode #7 I/O space. Mapped to the local side.

2.2 POS Registers

These registers are accessed when in Card Setup Mode. They may also be accessed by I/O locations in the 82C614's normal I/O space when not in Card Setup Mode.

Register	Bit	Function
POS0, POS1		**Adapter ID Bytes.** Defined by the board designer. Loaded by the INIT ROM. XX at RESET. RO from System processor. System processor reads 00 until the INIT ROM is fully loaded. These registers may be read and written by the system using I/O ports xx18 & xx19.
POS2		**Card Enable & I/O Select.** 00 at RESET. RW. Also accessible through I/O address xx42.
	0	Card Enable. 1=enable. Default at reset is 0.
	1-3	I/O address selection. Used for bits 13-15 of system I/O address decode for 82C614 registers. Set to 0 at reset.
	4-7	Programmable Decode Relocation. These bits specify address bits A16-13 of any programmable decode configured for 8K relocation. Used mainly for ROM BIOS relocation.

Register	Bit	Function
POS3		**Extended POS Register** if POS7 not= 00. Extended POS is used for POS access of 82C614 register set and some local bus I/O. **Standard POS Register** if POS7 = 00. **Arbitration Level, Parity, SFDBKRTN Check, & Streaming Data Enable.** 90 at RESET. RW. Also accessible through I/O address xx43.
	0-3	Arbitration level which the 82C614 will use.
	4	Fairness bit. When set to 1, fairness algorithm must be used.
	5	Parity check 0= no parity generated or checked. 1= Generate and check MicroChannel Data Parity.
	6	Check SFDBKRTN. 1 enables checking SFDBKRTN when a bus master, 0 disables. Register xx07 bit 4 must also be a 1 for SFDBKRTN to be checked. Lack of SFDBKRTN when checking is enabled will be indicated in the appropriate DMA status register, and that DMA channel will optionally halt.
	7	Streaming Data cycle select. 0= allow streaming cycles, 1= don't allow streaming cycles.
POS4		**Extended POS Register** if POS7 not= 00. Extended POS is used for POS access of 82C614 register set and some local bus I/O. **Standard POS Register** if POS7 = 00. 00 at RESET. RW. Also accessible through I/O address xx44.
	0-7	Programmable Decode relocation bits. These can work multiple ways. See text.

Register	Bit	Function
POS5		Interrupt Select, MFP Outputs, Channel Check. C0 at RESET. RW. Also accessible through I/O address xx45.
	0-1	Interrupt Level used. 10 00 = IRQA (a dedicated pin). 01 = IRQB (a dedicated pin). 10 = IRQC (a multifunction pin). 11 = IRQD (a multifunction pin).
	2-3	Not used. Reserved.
	4-5	Not used.
	6	Set to 0 when CHCK is asserted by the 82C614 to indicate that POS6 contains CHCK status. This bit is always the same as bit 7, and is read only.
	7	Set to 0 when CHCK is asserted by the 82C614. Writing a 1 to this bit sets this bit and bit 6 to a 1, and clears all of the CHCK sources.
POS6		Extended POS Address Low & CHCK Status. When POS5 bits 7-6 =00, contains CHCK status and is Read only. Otherwise, treated as extended POS address register and is R/W. 00 at RESET. RW. Also accessible through I/O address xx46.
	0	CHCK status: 1= Data parity error when written to as a slave.
	1	1= -CHCKIN input from local side active during MicroChannel access to local device.
	2-7	Always 0.
POS7	8-15	Extended POS Address. 00 at RESET. RW. Also accessible through I/O address xx47.

2.3 I/O Port Registers

I/O Address	Bit	Function
xx00		Revision Code of the 82C614. RO (hardwired by chip design). The INIT ROM will not overwrite the hardwired value. 00= Initial revision.
	0-3	For minor revision.
	4-7	For major revision.
xx01		Features supported by this Rev of the 82C614. 1= Supported. The INIT ROM will not overwrite the hardwired value. RO (hardwired by chip design).
	0-7	Reserved. Read as 0.
xx02		Revision Code of Board. These bits are defined by the designer of the adapter card.
	0-3	It is suggested that these bits are used for minor Revisions.
	4-7	It is suggested that these bits are used for major Revisions.
		XX at reset. Set by INIT ROM. RW.
xx03		Features supported by board.
		1= Supported. These bits are defined by the designer of the adapter card.
		XX at RESET. Set by INIT ROM. RW.
		0-7 User defined.

I/O Address	Bit	Function
xx04		**MicroChannel Side Configuration Register** /Buffer Allocation. XX at RESET. Set by INIT ROM. RW.
	0	Arbitration method of the MicroChannel side of the DMA controllers. 0=rotating arbitration. 1=fixed arbitration (channel 0 is highest priority).
	1	Halt DMA controllers on Channel Check. If a 1, all four DMA controllers will halt if -CHCK goes low on the MicroChannel (even if the 82C614 is not involved in the operation). If 0 they will not halt.
	2	Extended POS support. 0 disables extended support, 1 allows POS (register 3 and register 4) to become windows into extended POS.
	3	128 byte relocation mode for Programmable Decodes. 0=mode 0, 1=mode 1.
	4	-PREEMPT Release. 0 = Conservative, 1 = Aggressive. When programmed as Aggressive, the release time after -PREEMPT will be extended (approximately doubled) by the 82C614.
	5	-CMD Active during Streaming Data. 0 = conservative, 1 = Aggressive. When programmed as Aggressive, the -CMD active period is extended (approximately doubled) by the 82C614.
	6-7	Buffer configuration. These bits program how the 80 bytes of FIFO buffer are divided amoung the 4 DMA channels. The table below lists the number of bytes for each channel for the 4 combinations of these bits. The buffer configuration should be selected such that each device on the local bus using DMA has enough FIFO space to prevent overrun and underrun conditions. Performance considerations should also be taken into account when selecting the buffer configurations.

76	CH0	CH1	CH2	CH3	
00	32	16	16	16	
01	32	32	8	8	
10	32	32	16	0	(channel 3 local to local only)
11	64	16	0	0	(channels 2 & 3 local to local only)

I/O Address	Bit	Function
xx05		**Local Bus Configuration Register.** XX at RESET. Set by INIT ROM.
	0	Arbitration method of local side of the DMA controllers. 0=rotating arbitration. 1=fixed arbitration.
	1	Fixed priority order for the local side. 0=priority order is 0-1-2-3. 1=priority order is 3-2-1-0. Also affects direction for rotating priority.
	2	Local side arbitration time-out enable. Prevents a DMA channel from holding on to the local bus too long when other DMAs are pending. If a channel has had the bus for more than 4uS, it will not start a new bus cycle if a DMA from another channel is pending. 0=time-out disabled, 1=enabled.
	3	Local side compressed timing. 0=normal timing (default) 1=compressed.
	4	8 bit data mode. When set to 8 bit data mode, AD8-15 are address only lines, and do not need a latch. The data path on the local side is only 8 bits wide. 1=8 bit mode. 0=normal 16 bit mode.
	5	Address select for 8 bit data mode. Selects which address lines appear on AD8-15 when in 8 bit data mode. 0=A8-15. 1=A0-7. This bit has no effect when bit 4 is a 0. If bits 4 & 5 are both 1s, A8-15 are not available on the local side at all.
	6	DREQ polarity. 0=active low, 1=active high. Active high is most common.
	7	DACK polarity. 0=active low, 1=active high. Active low is most common.
xx06		**I/O Address of 82C614 Register Set.** XX at reset. Set by INIT ROM. RW (with extreme caution). INIT ROM should normally program a 1C at this location to comply with the Assignable I/O Address mechanism.
	0-4	Selects address bits 8-12 for I/O accesses to the 82C614 register set. (Bits 13-15 are supplied by POS2 bits 1-3).
	5-7	Not used.

I/O Address	Bit	Function
xx07		**MicroChannel Side Card Size Indicator & wait states.** XX at RESET. Bits 0-5 are RW, 6-7 are RO. Only bits 0-5 are loaded by the INIT ROM.
	0-1	Bus Master timing. These bits adjust the timing parameters used to generate MicroChannel bus cycles when the 82C614 is a Bus Master.
	0	0=Default cycle is 200nS. 1=default cycle is 300nS.
	1	Reserved for future timing selections for MicroChannel Master operation. Write as a 0.
	2-3	Slave wait states. Determines the number of wait states the 82C614 adds to register accesses when it is a slave.
	2	0=0 wait states, 1=1 wait state (additional 100nS - A Synchronous Extended cycle).
	3	Reserved for future timing selections for MicroChannel slave operation. Write as a 0.
	4	1=Sample -SFDBKRTN when a bus master. 0=ignore. Normally programmed the same as bit 5 since the -SFDBKRTN signal is on the 32 bit extension. The DMA registers specify the result of -SFDBKRTN being sampled inactive.
	5	Card size bit. Tells the 82C614 what card size to assume. Software will generally copy bit 7 of this register here. 0 = 16 bit card size, 1 = 32 bit card size. Only applies to the size of the address bus (24 or 32 bit) for the current rev of the 82C614. If the DMA controller attempts to do an access over 16M while programmed for a 16 bit slot, an error condition will occur which will be indicated in the particular DMA channel's status registers. The INIT ROM should generally program as a 1 (32 bit mode).
	6	1=bit 7 is valid. 0=bit 7 is always a 0. This bit will be a 1 if either Multifunction Pin #1, #3, or #7 is programmed to be the Card Size Indicator pin, and a 0 if none are programmed for this function.
	7	Card Slot size. Indicates whether the adapter card occupies a 16 bit or 32 bit card slot. Either Multifunction Pin #1, #3, or #7 may be used for this. 1=32 bit slot, 0=16 bit slot. This bit will read the inverted version of the Multifunction pin. Always indicates 0 if the board has not implemented this (the multifunction pin is used for something else).

I/O Address	Bit	Function
xx08		**Fixed Decode Configuration.** XX at RESET. RW.
	0-1	Wait states added on the local bus when any fixed decode is active. 10 00 = 0 wait states. 01 = 1 wait state (100nS added). 10 = 2 wait states (200nS added). 11 = 3 wait states (300nS added).
	2	Data size for fixed decodes 4-7. 0=8 bit, 1=16 bit.
	3	Data size for fixed decode 8. 0=8 bit, 1=16 bit.
	4	Buffered write enable when fixed decodes are active. 1= enabled.
	5	Data size when the External MicroChannel decode is active. 1= 16 bit. 0=8 bit. If Multifunction pin #1 is programmed to provide the data size, that pin is inverted, and ORed with this register bit.
	6-7	Local Bus Minimum wait states. Sets the minimum number of wait states for ALL local bus cycles. Same encoding as bits 0-1 above.
xx09		**DMA Implicit I/O wait states.** This register supplies the number of wait states added for Implicit I/O cycles on the local bus for each DMA channel. The encoding for each pair of bits is as follows: 00 = 0 wait states. 01 = 1 wait state (100nS added). 10 = 2 wait states (200nS added). 11 = 3 wait states (300nS added). XX at reset. RW.
	0-1	DMA channel 0.
	2-3	DMA channel 1.
	4-5	DMA channel 2.
	6-7	DMA channel 3.

I/O Address	Bit	Function
xx0A		**CHCK Enable Register.** Enables the individual sources for the CHCK interrupt. 1=interrupt enabled. XX at RESET. Set by INIT ROM. RW.
	0	Data parity error when written to as a slave.
	1	-CHCKIN pin input local side during MicroChannel access to a local device.
	2-7	Not used.
xx0B		**CHCK status Register.** Gives the status of each source of the CHCK interrupt. 1=device interrupting. Bits will be active even if the interrupt is not enabled. When the 82C614 has issued a CHCK, POS6 contains a copy of this register ANDed with the enable register (Reg 0A). Writing a 1 to the bit position will clear the interrupt. Writing a 0 will leave it unchanged. Write a 1 to POS5 bit 7 will clear all bits in this register. 00 at RESET. RW. The INIT ROM should contain a 00, which will have no effect on the register.
	0	Data parity error when written to as a slave.
	1	-CHCKIN input from local side during MicroChannel access to a local device.
	2-7	Not used. Read as 0.
xx0C		**Interrupt Enable Register.** Enables the individual sources for the standard interrupt. 1=interrupt enabled. Register 0E bit 2 decides whether or not the interrupt goes to the MicroChannel. If the destination is the MicroChannel, POS5 bits 1-2 decide which IRQ pin is used. XX at RESET. RW.
	0	DMA Channel 0 interrupt enable.
	1	DMA Channel 1 interrupt enable.
	2	DMA Channel 2 interrupt enable.
	3	DMA Channel 3 interrupt enable.
	4	External Interrupt 0 input enable.
	5	External Interrupt 1 input enable.
	6	External Interrupt 2 input enable.
	7	External Interrupt 3 input enable.

I/O Address	Bit	Function
xx0D		**Interrupt status Register.** Gives the status of each source of the standard interrupt. 1=device interrupting 0=device not interrupting. Bits will be active even if interrupt not enabled. Writing a 1 to bits 0-3 will clear the interrupt. Writing a 0 will leave it unchanged. Bits 4-7 are straight from the interrupt pins, and must be cleared by clearing the external source. If an external interrupt is not provided for by the multifunction pins, that bit position will read as a 0. X0 at RESET. RW INIT ROM should set to 00.
	0	DMA 0 End of operation.
	1	DMA 1 End of operation.
	2	DMA 2 End of operation.
	3	DMA 3 End of operation.
	4	External Interrupt 0 (dedicated pin).
	5	External Interrupt 1 (Multifunction pin).
	6	External Interrupt 2 (Multifunction pin).
	7	External Interrupt 3 (Multifunction pin).
xx0E		**-INITROM pin configuration.** Bit 7 is for the -INITROM pin. 01 at RESET. The INIT ROM should program a 001 into the first 3 bits for future compatibility.
	0	Program as 1.
	1	Program as 0.
	2	Program as 0.
	3-6	Not used. Read as 0s.
	7	-INITROM status after init ROM load. 0=high, 1=tristated. See INIT ROM description for further explanation.
xx0F		**Multifunction Pin Data Port.** Each multifunction pin may be programmed as an input port bit or an output port bit. This register is the data register for the pins programmed for this. A read of this register returns the value of all 8 Multifunction Pins regardless of how they are being used. A write to this register writes to an internal latch. The individual bits of the latch are sent to the corresponding Multifunction Pin only if it is programmed as an Output Port bit. XX at RESET. RW.
	0	Multifunction Pin 0.
	7	Multifunction Pin 7.

I/O Address	Bit	Function
xx10-xx17		Not used. INIT ROM locations corresponding to these register locations should contain 0s.
xx18		Alternate addressing for POS0 for loading by INIT ROM. R/W.
xx19		Alternate addressing for POS1 for loading by INIT ROM R/W. The value of the POS Registers 0 & 1 (the adapter ID) may be read or written through these registers. The INIT ROM uses these registers to load the Adapter ID into POS 0 & 1.
xx1A-xx1B		Not used. INIT ROM locations corresponding to these register locations should contain 0s.

2.4 Multifunction Pin Registers

These registers select what internal signal is connected to each Multifunction Pin. There are 4 bits for programming each pin, giving 16 selections for each. Each multifunction pin is an input for selections 0-7, and an output for selections 8-F. See the write-up on Multifunction Pins for the details of the function each pin performs for its various programming combinations. The following shows what register bits are assigned to what Multifunction pin.

I/O Address	Bit	Function
xx1C		**Multifunction pins 0 & 1.**
	0-3	Multifunction Pin 0.
	4-7	Multifunction Pin 1.
xx1D		**Multifunction pins 2 & 3.**
	0-3	Multifunction Pin 2.
	4-7	Multifunction Pin 3.
xx1E		**Multifunction pins 4 & 5.**
	0-3	Multifunction Pin 4.
	4-7	Multifunction Pin 5.
xx1F		**Multifunction pin 6 & 7.**
	0-3	Multifunction Pin 6.
	4-7	Multifunction Pin 7.

2.5 Programmable Decode Registers

These registers program the address range and other information for each Programmable Decode. All of the registers are XX at RESET, and are set by the INIT ROM.

Address Registers specify the value to compare.

Mask registers specify whether the address line should be ignored in the decode.
1= ignore bit position.
0= compare bit position to the address register bit.

I/O Address	Function
xx20	Decode 0 System Address 0-7.
xx21	Decode 0 System Address 8-15.
xx22	Decode 0 System Address 16-23.
xx23	Decode 0 System Address 24-31.
xx24	Decode 0 Mask for System Address 0-7.
xx25	Decode 0 Mask for System Address 8-15.
xx26	Decode 0 Mask for System Address 16-23.
xx27	Decode 0 Mask for System Address 24-31.
xx28	Decode 1 System Address 0-7.
xx29	Decode 1 System Address 8-15.
xx2A	Decode 1 System Address 16-19. Bits 4-7 Reserved. Read as 0.
xx2B	Reserved Read as 0.
xx2C	Decode 1 Mask for System Address 0-7.
xx2D	Decode 1 Mask for System Address 8-15.
xx2E	Decode 1 Mask for System Address 16-19. Bits 4-7 Reserved. Read as 0.
xx2F	Reserved Read as 0.
xx30	Decode 2 System Address 0-7.
xx31	Decode 2 System Address 8-15.
xx32	Decode 2 Mask for System Address 0-7.
xx33	Decode 2 Mask for System Address 8-15.
xx34	Decode 3 System Address 0-7.
xx35	Decode 3 System Address 8-15.
xx36	Decode 3 Mask for System Address 0-7.
xx37	Decode 3 Mask for System Address 8-15.

I/O Address	Bit	Function
xx38 xx3A xx3C xx3E		Decode 0 System Commands/DMA Channel decode. Decode 1 System Commands/DMA Channel decode. Decode 2 System Commands/DMA Channel decode. Decode 3 System Commands/DMA Channel decode. Each of the 4 registers is defined as follows: XX at RESET. Set by INIT ROM. RW.
	0	Read Cycles. 1= the decode is active for Read cycles, 0=not active.
	1	Write Cycles. 1= the decode is active for Write cycles, 0=not active.
	2	Memory/I/O. 0=active for I/O cycles, 1=active for memory cycles.
	3	Decode/Strobe. 0=pin is an address decode, 1=pin is a strobe (conditioned with CMD).
	4-7	DMA Channel Decodes. A 1 will cause the Programmable decode to be active for the specified DMA channel local cycles. It will only be active for the type of cycles (memory or I/O, Read and/or Write) specified above. They are not active for Implicit I/O cycles.
	4	DMA channel 0.
	5	DMA channel 1.
	6	DMA channel 2.
	7	DMA channel 3.

I/O Address	Bit	Function
xx39 xx3B xx3D xx3F		Decode 0 Control. Decode 1 Control. Decode 2 Control. Decode 3 Control. XX at RESET. Set by INIT ROM. RW.
	0-1	Wait state generation. When the decode is active, 100nS is added to the access time on the local bus for each wait state. Added for both MicroChannel initiated and DMA initiated cycles. This is in addition to wait states required to arbitrate for the local bus. 10 00 0 wait states. 01 1 wait state. 10 2 wait states. 11 3 wait states.
	2-3	Peripheral Data Size. Data size to be used during MicroChannel accesses. There is not enough time to receive the data size from the peripheral since a DMA cycle may be taking place on the local side when the MicroChannel cycle is initiated. 32 00 8 bit. 01 16 bit. 10 32 bit (not supported on 82C614). 11 Not defined.
	4-5	Relocatable address selector. Selects what type of POS relocation is used by the decode. 54 00 No Relocation by POS. 01 Relocation on 128 byte address boundary. 10 Relocation on 8K address boundary. 11 Relocation on 128K address boundary.
	6	Reserved. Read as 0.
	7	Allow Buffered writes. 1=allow buffered writes from MicroChannel yielding 0 wait state write cycles to the MicroChannel, 0=always write through, adding wait states to MicroChannel.

2.6 Other Registers

I/O Address	Bit	Function
xx40		Buffer Testing Control Register. Bit 7=0 at RESET, rest XX.
	1-0	DMA channel's buffer to be tested.
	2	Clear ring buffer pointers for all channels. A 1 clears, Must be rewritten to a 0.
	3-6	Reserved.
	7	Test mode. 0=normal mode. 1=test mode.
xx41		Buffer Testing Data Port When test mode is enabled, writing to this port causes data to be written into the next available location in the ring buffer for the DMA channel specified by the Buffer Testing Control Register. Reading this port causes the next byte from the ring buffer of the specified DMA controller to be read. Note that the read and write pointers are separate, and increment after each access. Overflows and underflows of the ring buffer are ignored. Initial value: 00. RO. (hardwired by chip design).
xx42-xx47		POS2-7 RW. Alternate method for accessing POS registers.
xx48-xx4F		Reserved.
xx50-xx5F		Reserved For possible future 82C614 registers not requiring INIT ROM setup.
xx60-xx7F		Decode #8 I/O space. Useable by local peripherals.

2.7 DMA registers

The 82C614 has 4 sets of DMA registers, one for each channel.

0080-0096 DMA channel 0.
00A0-00B6DMA channel 1.
00C0-00D6 DMA channel 2.
00E0-00F6 DMA channel 3.

Addresses listed below are for DMA channel 0.

I/O Address	Bit	Function
xx80-xx83		**DMA CH 0 System Address Registers.** Supplies the DMA Memory or I/O address on the MicroChannel side. All 32 bits must be programmed. For I/O cycles bits 16-31 must be set to 0. For memory accesses under 16Meg bits 24-31 must be set to zero, even if only 24 bits of address are supported by the system. The address will autoincrement if a memory address, and will not increment if an I/O address. XX at RESET. RW.
xx80	0-7	MicroChannel address.
xx81	8-15	MicroChannel address.
xx82	16-23	MicroChannel address.
xx83	24-31	MicroChannel address.
xx84-xx86		**DMA CH 0 Byte Count Registers.** Contains the number of bytes to be transferred. XX at RESET. RW.
xx84	0-7	Byte Count.
xx85	8-15	Byte Count.
xx86	16-23	Byte Count.
xx87		**Reserved**
xx88-xx8A		**DMA CH 0 Local Address Registers.** Supplies the 24 bit DMA address for the local side. XX at RESET. RW.
xx88	0-7	Local Address.
xx89	8-15	Local Address.
xx8A	16-23	Local Address.

I/O Address	Bit	Function
xx8B-xx8E		**DMA CH 0 Linked List Address Pointer Registers.** 32 bit register which points to the start of the next DMA linked list. Must be located on a word boundary, so the LSB must be 0. These registers are loaded during a linked list read. XX at RESET except for 8B which is set to 00. RW.
xx8B	24-31	Linked List address 00 at RESET.
xx8C	0-7	Linked list address. Bit 0 is always a 0, forcing an even address.
xx8D	8-15	Linked list address.
xx8E	16-23	Linked list address.
xx8F		**DMA Control CH 0 Register.**
	0	Direction bit. 0=from local to system, 1=from system to local.
	1	M/-IO indicator for the system side. 0=Memory, 1=I/O.
	2-3	Local side addressing mode. 32 00 = Local Memory. 01 = Local I/O. 10 = Local Implicit I/O. 11 = Local Implicit I/O to/from Local I/O or Memory. This is a special case. DATA is not FIFOed. The DMA source and destination are both on the local side.
	4	Force DREQ. 0 = Use DREQ protocol as programmed into the secondary control register. 1 = End of Linked List operation will trigger a forced DREQ (software DREQ).
	5	Reserved. Write as 0.
	6	Local address increment. 0=increment, 1=don't.
	7	Link List chain. 0=end of link list. 1=linked list pointer points to next entry to be executed.
xx90		**Start DMA CH 0.** A write to this address starts the DMA controller using the values programmed into the registers. The data is ignored. Write only. An 8 bit output must be done to avoid hitting the next port also.
xx91		**Start DMA CH 0 Linked List Chain.** A write to this port starts the DMA controller, but instead of using the values in the DMA registers, only the Linked List Address is used, the DMA controller begins by fetching the linked list entry. The data is ignored. Write only.

I/O Address	Bit	Function
xx92		**Halt DMA CH 0.** A write to this address HALTS the DMA controller. The data is ignored. Write only.
xx93		**DMA CH 0 Command Register (writes)/Secondary Status Register (reads).** **Writes:** There is one command for each bit position. If the bit is written as a 1 the command will be performed. Multiple commands may be performed with one instruction. Bits 0 & 1 should not be activated together. Write only.
	0	Trigger FIFO fill/empty. Triggers FIFO fill if the direction is from MicroChannel to peripheral. Triggers FIFO empty if direction is from peripheral to MicroChannel.
	1	Clear FIFO pointer. Clears the channels FIFO. Any data in the FIFO is lost.
	2	Force one DREQ (local side DMA request). Causes one DMA operation on the local side regardless of the state of DREQ. If Block Mode is programmed for that channel, this command will trigger the entire block to be DMAed. Has the effect of taking the external DREQ pin active until either a DMA cycle for that channel begins, or that channel is reprogrammed.
	3	Resume DMA. Resumes DMA operation without clearing the FIFO, etc, following a HALT DMA command.
	4	Clear DMA error Conditions. Clears the errors for the DMA channel. Mainly used to reset errors before a RESUME DMA command. Clears bits 2-7 of the status register, and 0-3 of the Secondary Status Register.
	5-7	Reserved. Write as 0s.

I/O Address	Bit	Function
xx93 (continued)		**Reads:** Indicates additional error information. These bits are set to 0 with a START DMA, START LINKED LIST, or CLEAR ERRORS command. Set to one if the error condition occurs. An error condition will halt the DMA channel if the Secondary Control register (95 for CH 0) bit 3 is a 1.
	0	DMA disabled bit. Set to a 1 if DMA is disabled by Card Enabled (POS2 bit 0) inactive.
	1	Access attempt to greater than 16M when programmed for a 16 bit card slot.
	2	Error occured (any error) during a linked list read for this channel.
	3	Error occured (data parity or -CHCK detected) during a streaming data cycle.
	4	Timeout error occured as a result of CHRDYRTN being held by the slave for more than 3.5uS.
	5-6	-SFDBKRTN status. These bits record the state of the -SFDBKRTN signal if a -CHCK condition is detected during a master cycle. 0 = -SFDBKRTN active, 1 = -SFDBKRTN inactive. Bit 5 is used for DMA master cycles, bit 6 is used for Linked List master cycles. Both bits are read only.
	7	Not used. Read as 0s.

I/O Address	Bit	Function
xx94		DMA CH 0 Status Register. RO.
	0	DMA busy. Set to 1 with a START DMA, START LINKED LIST, or RESUME DMA command (assuming Card is enabled (POS2)). Reset when DMA is finished (including all linked list entries), DMA is halted by an external source, or an error condition occurs (if bit 3 of the Secondary Control Register = 1).
	1	End of Transfer. Set to 0 with START DMA or START LINKED LIST command. Set to 1 upon completion of the DMA (the final entry in the linked list table) with no errors.
	2-7	Error indicator bits. All are set to 0 by executing a START DMA, START LINKED LIST, or CLEAR ERRORS command. If an error condition occurs, the bit is set to 1. The DMA channel halts on an error of the Secondary Control Register (95 for CH 0) bit 3=1.
	2	-CHCK detected during a write cycle to the MicroChannel.
	3	-CHCK detected during a read from the MicroChannel.
	4	Data Parity error during a read from the MicroChannel
	5	DMA "no feedback" bit. The 82C614 sets it to a 1 if no SFDBKRTN is sampled during the DMA transfer on the MicroChannel. SFDBKRTN is only sampled if POS3 bit 6 is a 1 and Register 07 bit 4 is set to 1 (normally set to a 1 when the card slot size is 32 bit.
	6	Time-out bit. Goes high if ARB/GNT goes high while the 82C614 is in the process of transferring data as a bus master.
	7	-CHCKIN activated during a cycle to the local bus.

I/O Address	Bit	Function
xx95		**DMA CH 0 Secondary Control Register.** 00 at RESET.
	0-1	Trigger point for buffer fill/empty to MicroChannel. 10 00 Empty when > 1/4 full. Fill when < 3/4 full. 01 Empty when > 1/2 full. Fill when < 1/2 full (default). 10 Empty when > 3/4 full. Fill when < 1/4 full. 11 Empty when > 7/8 full. Fill when < 1/8 full.
	2	Linked list address load size. 0=do not load bits 24-31 of the linked list address when reading linked list entries. 1=load bits 24-31 of linked list address from byte 0B of the linked list table.
	3	Halt on error. When 1, the DMA channel halts on any of the error conditions indicated in the Status and Secondary Status registers. When 0, the DMA channel continues. Should normally be set to a 1.
	4-5	DREQ Mode. 54 00 Mode A — Edge triggered mode. One DMA cycle per rising edge of DREQ (falling edge if DREQ programmed for active low). 01 Mode B — Block Mode. Once DREQ is detected active, all bytes will be transferred until terminal count. 10 Mode C — Demand Mode, fast timing. DREQ sampled immediately at end of previous DMA cycle. Back to back cycles will occur if DREQ is held active. 11 Mode D — Demand Mode, slow timing. DREQ sampled 3 clocks + 12.5nS after end of previous DMA cycle. Similar to "Single Transfer" mode of 8237.
	6	Data Size of local side for Implicit I/O. 0=byte wide. 1=word.
	7	Not used.

I/O Address	Bit	Function
xx96		Flush timer length. The flush timer will cause the DMA channel's FIFO to be emptied onto the MicroChannel periodically if the data is being provided by the local side at a very slow rate. Only active for transfers from the local side to the MicroChannel side. The timer is reset every time the channel's FIFO is read by the MicroChannel Side. Unused bits are read/write, and should be written as 0s when writing this register. Times shown are rounded off. The exact time is the binary division of the 40MHz clock (the first one is actually 51.2uS). 00 at RESET.
	0	Not used. RW.
	1-3	Timer length: 321 000 Flush timer off. 001 50uS (40MHz divided by 2048)(2**11). 010 200uS (40MHz divided by 8192)(2**13). 011 800uS (40MHz divided by 32,768) (2**15). 100 3.2mS (40MHz divided by 131,072) (2**17). 101 13mS (40MHz divided by 524,288) (2**19). 110 50mS (40MHz divided by 2,097,152) (2**21). 111 200mS (40MHz divided by 8,388,608) (2**23).
	3-7	Reserved. RW. Write 0s.
xx97		Reserved.
xx98-009F		Decode #4. For use by Local Peripherals.
xxA0-xxB7		DMA Channel 1. Register definitions are the same as for channel 0.
xxB8-00BF		Decode #5. For use by Local Peripherals.
xxC0-xxD7		DMA Channel 2. Register definitions are the same as for channel 0.
xxD8-00DF		Decode #6. For use by Local Peripherals.
xxE0-xxF7		DMA channel 3. Register definitions are the same as for channel 0.
xxF8-00FF		Decode #7. For use by Local Peripherals.

3.0 BASIC OPERATION

3.1 DMA Operation

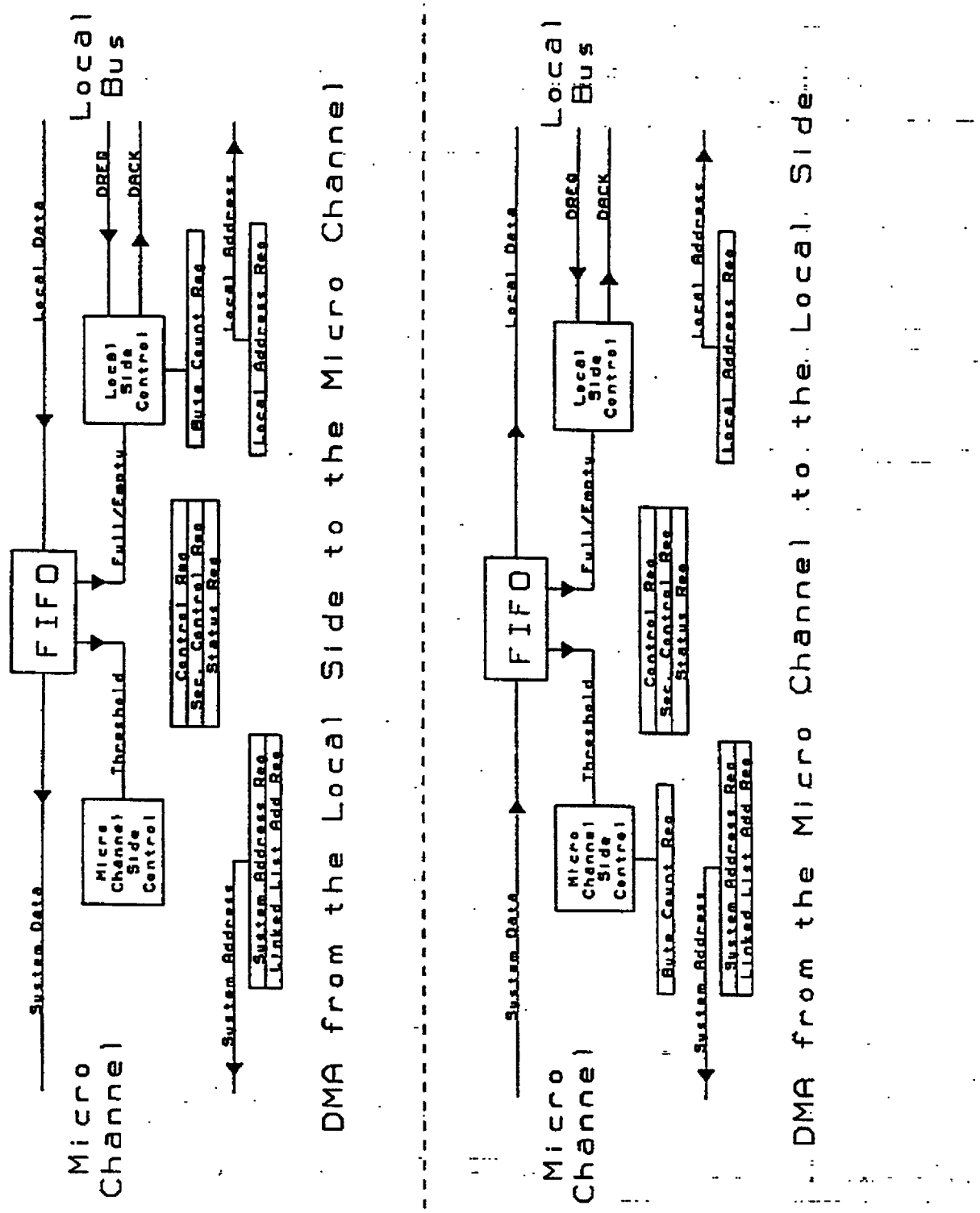
To minimize the usage of the MicroChannel, DMA operations are always done through a FIFO buffer within the 82C614. This allows blocks of data to be read or written from the MicroChannel in BURST cycles, reducing the number of arbitrations. Each of the 4 DMA channels has its own FIFO buffer. The size of each is programmable.

DMA from the MicroChannel to the local peripheral

When the DMA START is issued, the 82C614 will transfer data from the MicroChannel to the FIFO until the FIFO is full or Terminal Count is reached. The 82C614 will arbitrate for the MicroChannel and do burst mode cycles to fill the FIFO (the 82C614 may have to gain access to the bus more than once to do this if it is Preempted off the bus). If the addressed slave supports streaming data, 100nS streaming data cycles will be performed. The FIFO will be emptied a byte or word at a time to the peripheral, controlled by the DREQ pin for that channel. When the FIFO reaches the "trigger point" the 82C614 will refill it from the MicroChannel. This trigger point is programmable, and may be 1/4, 1/2, 3/4, or 7/8 empty. When the terminal count is reached on the MicroChannel side, no more data will be transferred. Nothing else will occur on the MicroChannel side until the FIFO has been emptied by the local side. When the local side empties the FIFO, the DMA process is ended. At this point, if the linked list bit in the Control Register is a 1, a new set of DMA parameters will be loaded from the MicroChannel using the Linked List Address and the new DMA operation will be executed. The 82C614 will become a bus master to read the table. If the linked list bit is a 0 the Terminal count interrupt will be issued, if enabled, and the DMA controller will be idle.

DMA from the local side to the MicroChannel

The local peripheral will begin loading the FIFO a byte or word at a time on each DREQ. When the FIFO reaches the trigger point, which is programmable, it will be emptied onto the MicroChannel using burst cycles. The FIFO will be completely emptied, even if it contains an odd number of bytes. When Terminal count is reached on the local side, it will trigger a request to empty the FIFO on the MicroChannel side. When the FIFO is empty, the linked list bit will be checked in the command register. If it is a 1, the next linked list entry will be downloaded into the DMA controller and executed. If it is a 0 a Terminal Count interrupt will be issued and the DMA controller will be idle.



DMA Registers

Each DMA controller has a block of 24 I/O ports. The first 16 of these are automatically loaded by a linked list operation. These ports include:

- A 32 bit System Address pointer.
- A 24 bit byte Count Register.
- A 24 bit Local Address Pointer.
- A 24 or 32 bit Linked List Pointer.
- A 1 byte Control Register.

Ports not loaded by the linked list include:

- 3 immediate Command Ports where the data is ignored.
- 1 immediate Command Port where the data specifies the command.
- 1 Secondary Control Register.
- 1 Status Register.
- 1 Secondary Status Register.

The table below lists the DMA registers and their addresses for each channel. When a DMA channel performs a Linked List read, 16 bytes are read from MicroChannel Memory, and loaded into the first 16 registers for that channel, in the order listed below. Note that bit 2 of the Secondary Control Register programs whether the Linked List address bits 24-31 (byte B) get reloaded during a linked list read operation.

DMA Register I/O addresses and Linked List Order

Register Addresses for each Channel Ch 0	Ch 1	Ch 2	Ch 3	Linked List Byte	Register Description
xx80	xxA0	xxC0	xxE0	0	MicroChannel address 0-7.
xx81	xxA1	xxC1	xxE1	1	MicroChannel address 8-15.
xx82	xxA2	xxC2	xxE2	2	MicroChannel address 16-23.
xx83	xxA3	xxC3	xxE3	3	MicroChannel address 24-31.
xx84	xxA4	xxC4	xxE4	4	Byte Count bits 0-7.
xx85	xxA5	xxC5	xxE5	5	Byte Count bits 8-15.
xx86	xxA6	xxC6	xxE6	6	Byte Count bits 16-23.
xx87	xxA7	xxC7	xxE7	7	Reserved.
xx88	xxA8	xxC8	xxE8	8	Local Address bits 0-7.
xx89	xxA9	xxC9	xxE9	9	Local Address bits 8-15.
xx8A	xxAA	xxCA	xxEA	A	Local Address bits 16-23.
xx8B	xxAB	xxCB	xxEB	B	Linked List address bits 24-31.
xx8C	xxAC	xxCC	xxEC	C	Linked List address bits 0-7.
xx8D	xxAD	xxCD	xxED	D	Linked List address bits 8-15.
xx8E	xxAE	xxCE	xxEE	E	Linked List address bits 16-23.
xx8F	xxAF	xxCF	xxEF	F	Control Register.

DMA Register I/O addresses and Linked List Order (continued)

Register Addresses for each Channel Ch 0	Ch 1	Ch 2	Ch 3	Linked List Byte	Register Description
xx90	xxB0	xxD0	xxF0	-	Start DMA.
xx91	xxB1	xxD1	xxF1	-	Start Linked List.
xx92	xxB2	xxD2	xxF2	-	Halt DMA.
xx93	xxB3	xxD3	xxF3	-	DMA command/ Secondary Status Register.
xx94	xxB4	xxD4	xxF4	-	DMA Status Register.
xx95	xxB5	xxD5	xxF5	-	Secondary Control Register (Chips added).
xx96	xxB6	xxD6	xxF6	-	Flush Timer setup.

DMA Register Descriptions

The MicroChannel Address Register points to either memory or I/O, as specified by the Command register. The upper 16 bits should be programmed to 0 if it is an I/O address. The address will auto increment if a memory address, but will not increment if an I/O address. The data width of the addressed slave will be determined by the DS16RTN pin on the MicroChannel. The 82C614 will generally do word transfers on the MicroChannel, which will be divided into two byte transfers if the slave is 8 bit. The 82C614 will do byte transfers only under the following conditions:

1. The transfer count is programmed with an odd number (the last transfer will be a byte).

2. The FIFO is being emptied onto the MicroChannel and there is an odd number of bytes in the FIFO (the last transfer of the flush will be a byte operation, and the first transfer of the next FIFO empty will be a byte).

3. The initial value of the address register is an odd number. This will force all transfers to be byte transfers due to the misalignment of data.

Local Address Register

The Local Address Register may also contain a memory or IO address, as programmed by the Command Register. In addition, Implicit addressing may be used. For implicit addressing, the DACK pin for the respective DMA channel is used as a chip select for the peripheral and no address need be produced. Many peripherals have a DACK input for this purpose, which is independent of the normal Chip Select. The 82C614 will place the contents of the Local Address Register on the local address bus during implicit I/O cycles also, but it will normally not be used. The Local Address Register will be incremented after each local bus DMA operation by the DMA channel if specified by the Control Register.

Byte Count Register

Since there is a FIFO between the MicroChannel and local sides, the current byte counts will actually be different on the two sides much of the time. Because of this, the byte count register will be associated with whichever side is the source of the data. The total number of bytes transferred will be equal to the value loaded into the byte count register plus 1. The two directions will be specified separately here.

- **MicroChannel to Peripheral Transfer.** When the Byte Count underflows past 0 the FIFO will no longer be filled from the MicroChannel side. The Terminal count interrupt will not be issued yet, however. When the FIFO is emptied on the local side, the final cycle will produce a TC output signal (a multifunction pin) on the last transfer. The Terminal count bit will then be set internally. If a linked list transfer is programmed, it will take place at this point, otherwise an interrupt will be sent to the MicroChannel, if enabled.

- **Peripheral to MicroChannel Transfer.** When the Byte Count underflows past 0 the TC output will be activated with the last cycle (the TC is for the local side. TC on the MicroChannel is not used by the 82C614). Any further DREQs will be ignored until the DMA channel is reprogrammed. A request will be given to the MicroChannel arbiter to empty the FIFO to the MicroChannel. When the FIFO is empty the internal TC will occur which will trigger the next linked list fill or cause the terminal count interrupt.

Linked List Address Register

The Linked List Address Register contains the address of the next 16 byte block of DMA parameters to be loaded. The parameters are loaded from MicroChannel memory. The parameters will be loaded when a Linked List Start command is issued from the MicroChannel, or when a DMA operation successfully finishes and bit 7 of the control register is set to a 1. The Linked List address is 32 bits. Bit 0 must be programmed to a 0, making all Linked List entries start on a word boundary. The Linked List Address register is one of the registers loaded by the linked list read operation. The 82C614 may be programmed to load all 32 bits or only the lower 24 bits of this register during a linked list operation. The 24 bit mode is provided to be compatible with an existing format. When programmed to 24 bit mode, the upper bits of the linked list register will still be used, but they will not be reloaded during linked list operations. They will power up to 00, and can be changed by direct programming from the MicroChannel.

Control Register

The Control Register specifies the data direction, whether the MicroChannel address is a memory or I/O address, whether the local address increments, whether a linked list operation should be done when the current DMA is finished, and the addressing of the local side. The addressing on the local side can be as follows:

Mode	Local Address Mode
0	A memory address.
1	An I/O address.
2	An Implicit I/O port.
3	An Implicit I/O port to/from Local memory or I/O.

When Mode 0 or 1 is used, one of the 82C614's chip select outputs will normally be programmed to be active to select the peripheral. The Chip select programming also provides the DMA channel with the data size of the peripheral.

An "Implicit I/O Port" is a port for which there is no address required. The DACK signal for the respective channel is used to enable the port, and is usually connected to the DACK pin of the peripheral chip. Any I/O which is decoding the address should be disabled during an implicit I/O DMA operation (as on the AT bus). This can be done using the individual DACK lines or the AEN signal, which is available as a multifunction pin. Generally a peripheral on the local side will be using one of the Programmable or Fixed decodes as their chip select. These will NOT be active during an implicit I/O port access (even if programmed to be active for that DMA channel), so no further gating is needed.

Mode 3 is a special case. The entire DMA operation occurs on the local side. Instead of reading data from the local side, placing it in the FIFO, and then bursting it onto the MicroChannel, the data is read from the local side, and written back out to another device or memory on the local side (or vice versa). A temporary holding register is used to store the data instead of the FIFO.

In Mode 3 one device is an Implicitly Addressed I/O port, and can be thought of as the normal "local side" port. It is the one controlling the DREQ. The second device is addressed using the local address register (which is not needed by the implicitly addressed device). The System side M/ I/O bit is used to select whether the local address is a memory or I/O address. The direction b.t=0 to DMA from the implicit port to the addressed port, =1 to DMA from the addressed port to the implicit port.

Normally the DACK signal is active for any access to the local side by the respective DMA controller. This is true for Modes 0, 1, & 2, as well as the Implicit I/O access of mode 3. The DACK will NOT be active during accesses to the "secondary" (addressed) device in mode 3.

START DMA, HALT DMA, and START LINKED LIST Ports

The START DMA, HALT DMA, and START LINKED LIST ports are write only ports which execute the specified function. The data is ignored for all three commands.

- START DMA enables the DMA controller, using the values which are programmed into the DMA registers. The FIFO pointers and flush timer are cleared with this command.

- START LINKED LIST causes the DMA controller to immediately load its registers from the linked list entry addressed by the linked list address register. The DMA will be started as soon as the linked list loading is complete (The DMA will actually start after the 82C614 has released and regained the MicroChannel, or another 82C614 DMA channel has completed a DMA cycle). This command also clears the FIFO pointers and flush timer.

- HALT DMA stops DMA activity. To resume after a HALT DMA, a RESUME DMA command should be issued. The RESUME DMA does not have its own I/O port, but is issued by using the DMA COMMAND register below. Issuing a START DMA after a HALT DMA command would clear the FIFO, causing a possible loss of data.

DMA COMMAND

The DMA COMMAND port allows additional commands to be immediately executed. Setting the respective bit to a 1 will perform that command. More than one bit may be set to a one. This is a write only register. Bits 0 and 1 should not be set to 1 at the same time.

Bit	Function
0	Triggers a FIFO fill or empty from the MicroChannel.
1	Clears the FIFO pointers, which in effect resets the FIFO. This should not be done when a DMA controller is operating since it will cause data loss.
2	Forces a DREQ on the local side. This is most useful when the DMA channel is in DREQ Mode B (Block Mode) and no external hardware is controlling the DREQ. This command would cause the entire DMA block to be performed, until Terminal Count. In DREQ modes A, C, and D this will cause one DMA cycle on the local bus. If there is no room (or data) in the FIFO, the cycle will be delayed until there is.
3	Issues a RESUME DMA command, to continue after the DMA channel is halted from an error or a HALT DMA command.
4	Clears the errors from the status registers. This might be done before a RESUME DMA commmand after an error has halted the DMA channel.

Secondary Command

The Secondary Command register contains configuration information about the DMA channel. It is not reloaded by the linked list. It contains the following:

- Trigger point for the FIFO on the system side. Specifies how full or empty the FIFO should be before a MicroChannel arbitration is requested.
- The size of the linked list address. The full 32 bits of the linked list address is always used, but if this bit is set to a 0, only 24 bits will be reloaded during a linked list operation. The upper 8 bits are set to 0 at powerup, but may be changed by the processor. If this bit is a 1, all 32 bits will be updated on a linked list fill.
- Whether the DMA channel should be halted on an error.
- DMA Request mode. The four modes are:
- Mode A: Edge triggered mode. One DMA cycle per rising edge of DREQ (falling edge if DREQ programmed for active low). It must go low, then high again (or vice-versa) to cause another DMA cycle.
- Mode B: Block Mode. After the DREQ is sampled active once, the entire DMA will be performed without sampling the DREQ again, until terminal count.
- Mode C: Demand Mode, fast timing. DREQ sampled immediately at end of previous DMA cycle. Back to back cycles will occur if it is still active.
- Mode D: Demand Mode, slow timing. DREQ sampled 3 clocks + 12.5nS after end of previous DMA cycle. Similar to "Single Transfer" mode of 8237.
- Data size (8 or 16 bit) when Implicit I/O is used.

Flush Timer

The Flush Timer is used to empty the FIFO for the DMA channel onto the MicroChannel in the event that no data has been received from the local side peripheral for a while. This prevents data from sitting in the FIFO for an extended period of time. The timer is reset each time data is transferred from the channel's FIFO to the MicroChannel. If it times out, a FIFO empty request is triggered. The flush timer only operates for DMA operations from the local side to the MicroChannel. No flush timer is needed when transferring the other way. Registers xx96, xxB6, xxD6, and xxF6 program the Flush timers for the respective channels. It may be set to 50uS, 200uS, 800uS, 3.2mS, 13mS, 50mS, 200mS, or turned off (these numbers are rounded off - the first one is actually 51.2uS, etc.). The register selects a prescaler which clocks a divide by 8 counter, so the maximum time from a previous FIFO empty to a flush time-out is the specified value, and the minimum is 87% of the timer value.

Status Register and Secondary Status Register

The Status Register and Secondary Status Register provide the BUSY and error indications. Bit 0 of the Status register is the BUSY bit. It is a 1 whenever the DMA channel is operating. It is set to a 1 with the START DMA, START LINKED LIST, or RESUME DMA commands, and reset to a 0 when the terminal count has been reached, the FIFO is empty, and the linked list bit in the command register is a 0. The busy bit will also be set to a 0 when any of the following conditions occurs: a HALT DMA command is executed, the 82C614 is disabled by POS2 bit 0, or if an error occurs relating to the DMA channel and bit 3 of the secondary control register is a 1.

Bit 1 of the Status register is set to a one when a DMA operation is ended, including all linked list entires, with no errors.

The remaining bits in the Status Register and all of the bits in the Secondary Status register are error indicators. The errors are cleared when a START DMA, START LINKED LIST, or CLEAR ERRORS command is executed. A RESUME DMA command does not clear the errors. These errors, and the conditions which cause them are listed below:

- -CHCK detected during a write cycle when a MicroChannel Master was servicing this DMA channel.
- -CHCK detected during a read cycle when a MicroChannel Master was servicing this DMA channel.
- Read Parity error. Set to a one if incorrect parity is received when the 82C614 is a MicroChannel Master servicing this DMA channel. This error will only occur when POS3 bit 5 is a 1 and -DPAREN is active for the cycle. Data parity is only checked on the data busses actually being used to transfer data as determined by A0, -SBHE, and -DS16RTN.
- No SFDBKRTN sampled when the 82C614 is a MicroChannel Master servicing this DMA channel. This error will only occur if POS3 bit 6 is a 1 and register 07 bit 4 is a 1.
- Time out. Will occur if the ARB/-GNT signal goes high while the 82C614 is a MicroChannel Master servicing this DMA channel.
- -CHCKIN detected. Set to a 1 if -CHCKIN is detected active while performing a LOCAL bus cycle for this DMA channel.
- DMA Disabled. It will occur if a START DMA, START LINKED LIST, or RESUME DMA command is done when the POS2 bit 0 = 0 (card disabled) or DMA is disabled by the SCB (Subsystem Control Block).
- Address boundary error. Set to a 1 if while a MicroChannel Master servicing this DMA channel, an attempt is made to access memory greater than 16Mbytes when the 82C614 is programmed to be connected to a 16 bit slot. Register 07 bit 5 determines whether the card slot is 16 or 32 bit.

The next 3 are set with other error bits, to indicate additional information:

- Error occured (any error) during a linked list read for this channel.
- Error occured (data parity or -CHCK detected) during a streaming data cycle.
- Timeout error occured as a result of IOCHRDY being held by the slave for more than 3.5uS.

3.2 MICROCHANNEL TRANSFERS

The 82C614 is both a slave and a master on the MicroChannel, at different times. It is a slave when the CPU or other MASTER accesses one of the 82C614 registers, or accesses memory or I/O devices on the 82C614's local side. It is a master when transferring data to or from the buffer (under control of one of the DMA channels), or when filling a LINKed LIST entry.

MicroChannel Slave

As a MicroChannel Slave the 82C614 will respond to three types of accesses:

- POS register accesses.
- Internal register accesses.
- Accesses to peripherals on the local side (memory or I/O).

POS and register accesses differ only in the way they are addressed. The POS registers are accessed by taking the -CDSETUP pin low, and providing an address on A0-A2. POS registers are accessible regardless of the state of the Card Enable bit (in POS2). CDSFDBK is not driven during POS register accesses. The rest of the registers are accessed with normal I/O cycles. The I/O address of the register set is determined by Register 06 (which is loaded by the INIT ROM) and POS register 2. These registers are accessible only when the Card Enable bit is a 1. CDSFDBK is driven for these register access cycles.

POS and register accesses may be programmed to be either 0 or 1 wait states on the MicroChannel. Since a register access uses only the MicroChannel side of the chip, it may occur concurrently with DMA activity on the local side.

The registers in the 82C614 are addressed in a 256 address block. About 150 of these addresses are used for actual registers in the 82C614. The registers are somewhat scattered through the 256 address block to allow sections to be grouped together (each DMA controller's registers start on a 32 port boundary). Some of the remaining addresses are reserved for possible future use by the 82C614, while the rest may be used by peripherals on the local bus.

The 82C614 will respond to all 256 I/O ports. Accesses to reserved registers, writes to Read Only registers, or reads from write only registers will be treated as "no operation." There are 5 blocks of I/O ports within the 256 port register area which are set aside for use by the local peripherals. These are referred to as Fixed Decodes since they are fixed within specific area of the 82C614 register set I/O. When one of these blocks is accessed it will either cause a local bus access, if a local bus peripheral is using the block, or a "no operation" if the block is unused on the local side. See the next section for more details.

The 82C614 will appear as a 16 bit slave for all I/O to the register area, except for the Fixed Decode areas. Fixed Decodes use the data size programmed into register 08 (the Fixed Decode Configuration Register). The 82C614 registers may be read from or written to with 8 or 16 bit I/O instructions. Back to back I/O accesses to the 82C614 registers, or any 82C614 access are permissible.

Accesses to Local Peripherals

MicroChannel accesses to the local peripherals are done through the 82C614. The 82C614 performs the MicroChannel I/O and/or memory decode for the devices on the local bus. The 82C614 appears as the slave for these accesses, and generates the address, chip select, and timing on the local bus to access the peripheral. The 82C614 also passes the data between the MicroChannel and local peripheral, performing any byte swapping that is necessary.

The 82C614 is programmed with the MicroChannel address range, the data size (8 or 16 bit device), and the access time of each peripheral on the local bus. The address is used to determine when the 82C614 should respond as a MicroChannel slave and which chip select to activate. The data size is passed onto the MicroChannel through the -CDDS16 pin. The access time is used to add wait states on the local bus, which in turn adds wait states to the MicroChannel. The peripheral may also add wait states in hardware by using the READY input on the local side.

When the 82C614 detects an access to a local peripheral, it pulls CDCHRDY low, and arbitrates for the local bus. MicroChannel accesses have the highest priority on the local bus, so the longest that this arbitration will take is the time it takes to complete a bus cycle in progress. When the local bus is available, the bus cycle is performed and the data is passed from the local side to the MicroChannel side or vice-versa.

The 82C614 detects a MicroChannel access to a local peripheral in one of three ways:

- Programmable Decodes.
- Fixed Decodes.
- External decode.

There are 4 Programmable Decodes which allow local peripherals to use memory or I/O spaces anywhere in the MicroChannel address range. See the separate section on Programmable decodes for details of the addressing. These are referred to interchangeably as Programmable Decode 0 to 3 and Decode 0 to 3. The pins on the 82C614 which are activated by these decodes are called -CS0-3.

The Fixed Decodes allow peripherals to use 5 areas of the 82C614 register map which are not used by internal registers. Four of them (Decodes 4-7) each decode a range of 8 I/O ports, while the other one (Decode 8) decodes a 32 port range. See the section on Fixed Decodes for more details. The fixed decode chip selects are provided to the local side through multifunction pins. They are called -CS4-8.

If a MicroChannel decode is required which cannot be done with the Programmable or Fixed decodes, an external decoder may be used. Multifunction Pin #0 may be programmed to be a decode input. When this input is low, the 82C614 will respond to the MicroChannel cycle and perform a local bus cycle. The decode may be unlatched, and consist of Address lines, M/ -I/O, -S0, and -S1 decoding.

Buffered Writes

Accesses to devices on the MicroChannel, particularly I/O devices, will have several wait states added, due to the speed of most peripherals. The 82C614 incorporates a buffered write scheme to reduce the average number of wait states during accesses to its peripherals. When Buffered Writes are enabled, a write cycle to a device on the local bus will be 0 wait states as far as the MicroChannel is concerned. The 82C614 will latch the address and data, and perform the local bus cycle as soon as the local bus becomes available. Only one write cycle will be buffered at a time. If the MicroChannel attempts to access a device on the local side before the write buffer has been cleared out, wait states will be added on the MicroChannel until the previous write is finished. If the second access is a write, it will then be buffered, and CDCHRDY will be returned to the MicroChannel. If the second access is a read, a normal read cycle will be done on the local bus, and CDCHRDY will be returned high to the MicroChannel when the data is available.

Note that while buffered writes will always decrease the average number of wait states for accesses to the local peripherals, it may increase the number of MicroChannel wait states for a particular access. When a write cycle to a local device is immediatly followed by a read cycle from a local device, the read cycle will have more wait states on the MicroChannel than it would have had if buffered writes were turned off. If devices with very long access times are present on the local bus, care must be taken to avoid exceeding the 3.5uS limit on holding CDCHRDY inactive on the MicroChannel. Buffered writes may have to be turned off in this case. The longest time CDCHRDY will be held low is as follows:

- A DMA cycle on the local bus has just started.
- A MicroChannel write to a local device begins. The write is buffered by the 82C614 yielding a 0 wait state cycle on the MicroChannel.
- A MicroChannel read cycle to a local device immediately follows the write.

The read cycle will have wait states added until the DMA cycle is finished, the buffered write is done on the local bus, and the read cycle is completed on the local bus. Peripherals with access times above approximately 1uS will begin to have problems. The exact access time at which buffered writes must be disabled will appear in a future revision of this data sheet.

Note that read and write cycles to the 614s internal registers are 0 wait state, and are not affected by buffered writes.

During accesses to local peripherals, the 82C614 will appear as either an 8 or 16 bit slave depending on the data size of the local side device. See the section on data sizes for how this is determined.

During a read from the local bus, several things control the number of wait states:

- The 82C614 will have to arbitrate for use of the local bus (A DMA channel may be using the bus). MicroChannel slave accesses have the highest priority in the local bus arbiter.
- If a buffered write is pending from a previous MicroChannel access, it will be performed first.
- Once the bus cycle is initiated on the local side, the programmed wait states will be added.
- Local READY will be sampled until it is active. At this point CDCHRDY will be returned to the MicroChannel.

Write cycles are handled the same was as read cycles unless Buffered Writes are enabled. With buffered writes, if the write queue is empty, the access will be stored in the write queue, yielding a 0 wait state cycle on the MicroChannel. If the write queue is not empty, wait states will be added to the MicroChannel cycle until the write queue is empty. The write will be performed on the local side as soon as it becomes available. No other cycles will occur on the local side before the buffered write is performed except cycles which were in progress when the actual MicroChannel write occurred.

MicroChannel MASTER

The 82C614 will become a bus master for DMA data transfers and for Linked List reads. The MicroChannel side contains two different arbiters for bus master activity.

The MicroChannel Arbiter is used to gain access to the MicroChannel itself. The arbitration level used by the 82C614 is programmed into POS register 3. The 82C614 follows the MicroChannel Specification for this arbiter.

The Burst Arbiter receives requests from the DMA channels for data or linked list transfers. Data transfers fill or empty a FIFO while Linked List transfers load the DMA registers. Linked list transfers have a higher priority than data transfers. Within the linked list requests, the priority is fixed, with channel 0 having the highest priority. Within the data transfer requests, priority is either fixed (channel 0 highest) or rotating. An arbitration will be done between each bus cycle. A complete streaming data transfer is considered to be one bus cycle, and will not be interrupted by an arbitration.

The 82C614 will do as many transfers as it can once it gains control of the MicroChannel bus. This may involve several Linked List or DMA data transfer operations. When one operation is complete, the Burst Arbiter gives control to the highest priority requesting device and transfers continue without giving up the bus. Note that this will cause non-contiguous addresses, mixed reading and writing, and mixed memory and I/O cycles on one MicroChannel Arbitration. When PREEMPT goes active while the 82C614 has the bus, it will do as many more bus cycles as it can without violating the MicroChannel specs before giving up the bus.

3.3 Local Bus

The adapter card containing an 82C614 will usually contain one or more I/O mapped peripherals. Many adapter cards will also contain a BIOS ROM, and some will contain a RAM buffer. All peripherals and memory on the adapter card will normally be connected to the Local Bus of the 82C614. This bus provides address, data, chip selects, command signals, and interrupt inputs for the peripherals and memory.

Address: 16 address bits are muxed with the data lines. External latches must be provided to latch the address bits which will be used. If only an 8 bit data bus is needed, 8 latched bits may be provided by the 82C614 directly. 8 high order address bits (A16-23) are available on the multifunction pins. -BHE is provided for 16 bit peripherals or memory.

Data: The peripheral's and memory's data busses may be connected directly to the 82C614's muxed address/data pins. Each peripheral or memory may use either an 8 bit or 16 bit data bus.

Chip selects: 9 chip select lines are provided plus the INIT ROM chip select. 4 are programmable, and may provide a chip select for any I/O address range produced from the MicroChannel. One of these programmable decodes may by used by a memory device instead, decoding any memory range on the MicroChannel. Another may be used by a BIOS ROM, and will decode any BIOS ROM area on the MicroChannel. 4 of them decode an 8 port I/O range which falls within the 256 port I/O range used by the 82C614. 1 of them decodes a 32 port I/O range which falls within the 256 port I/O range used by the 82C614.

Commands: Separate I/O READ, I/O WRITE, MEMORY READ, and MEMORY WRITE pins are provided.

Wait states: A READY pin is provided to add wait states to the bus cycles. The 82C614 may also be programmed to provide automatic wait states for the devices.

DMA signals: A DMA REQuest and DMA ACKnowledge pin is provided for each of the 4 DMA channels. Any of the chip select pins may also be activated for DMA cycles. Additional DMA signals such as Terminal Count may be provided by multifunction pins.

Interrupts: 1 interrupt input is provided as a dedicated pin. 3 more are available through the multifunction pins. In addition there is a dedicated pin for a CHCK interrupt input which will activate the CHCK pin on the MicroChannel.

By using the chip select lines provided by the 82C614, the local peripherals will generally not need to do any address decoding. Most peripherals will require a chip select from the 82C614 and a few address bits only. Memory devices will generally require more address bits. Only those address bits which are needed by the local devices need be latched externally. Two 373 latches are all that is needed to latch all 16 address bits. If more than 16 address lines are needed, one or more of the multifunction pins may be programmed to provide additional bits. These do not need to be externally latched.

Many adapter cards will not require a 16 bit data bus on the local side. If this is the case, the 82C614 may be programmed to only provide 8 data bits, allowing the other 8 pins to be dedicated address lines. This will eliminate the need to latch these lines. The latched addresses on AD8-16 may be programmed to be either A8-16 or A0-7. A0-7 would be selected in cases where only 8 bits of data and 8 bits of address are required. In all cases, A0-7 will be muxed on pins AD0-7.

There are two timing modes for the local bus: Normal mode and Compressed mode. Compressed timing provides setup and hold times and peripheral requirements similar to that of the MicroChannel. In Normal mode the setup and hold times have been increased, as well as more relaxed peripheral requirements, such as data bus float delay. Many peripheral chips require these relaxed parameters. Compressed mode has a cycle time of 200nS and a nominal command active time of 100nS. In Normal mode these are increased to 300 and 150 respectively. In general, normal mode should be used unless the higher throughput of compressed mode is required. The local bus timing diagrams, as well as the timing specs for both compressed and normal modes are at the end of this document.

Two types of bus cycles are performed on the local bus: DMA accesses and MicroChannel requested accesses. DMA accesses are initiated by the 82C614, usually in response to a device on the local bus activating a DREQ line. Data is moved from a device on the local bus to the 82C614's internal FIFO or vise-versa. A MicroChannel requested access is a normal memory or I/O access by the MicroChannel (usually from the system microprocessor) to a device on the adapter card. The same local bus timing is used for both types of cycles.

The Local Arbiter controls access to the local side. MicroChannel accesses have a higher priority than the DMA accesses. Within the DMA channels, priority may be either fixed or rotating. The order of priority may be either 0-1-2-3 or 3-2-1-0 for fixed priority. When programmed to DREQ modes B or C, once the channel wins the arbitration, it may perform several bus cycles if the peripheral continues to request data. A time-out may be programmed to force an arbitration after a channel has the local bus for 4uS. A MicroChannel access request will always force an arbitration after the current bus cycle.

A MicroChannel requested access will be caused by a device on the MicroChannel (generally the System Board CPU) doing an I/O or memory cycle to an area decoded by a Programmable, Fixed, or External Decode. During the bus cycle, the address placed on the local bus will be directly copied from the MicroChannel. The appropriate chip select line will also be activated. Generally a peripheral need only use a chip select signal from the 82C614 and several of the lower address lines. If multiple decodes are programmed to the same I/O or memory area, all of them will be activated.

DMA accesses are requested by the DREQ lines. If the DMA channel is not enabled or has reached terminal count on the local side the DREQ will be ignored. If there is no room in the FIFO (or no data available) the DREQ will be delayed until the DMA cycle can be performed.

Addressing for DMA cycles is done several ways. The appropriate DACK line will be active during "Implicit I/O" cycles. If the DMA channel is programmed for Addressed Memory or I/O, one of the chip select outputs may be programmed to be active for the DMA operation. Note that the chip select is programmed to be active for bus cycles for a particular DMA channel(s). This is NOT done by decoding the DMA address. The address compare registers of the Programmable Decodes are used to compare the MicroChannel address only. The memory or I/O address from the Local Address Register for the channel is placed on the local bus during the bus cycle.

Local Bus DMA Cycles

DMA Mode	DACK Generated	CSN Generated	Address Produced
Mode 0 Addressed memory	No	Yes	Yes
Mode 1 Addressed I/O	No	Yes	Yes
Mode 2 Implicit I/O	Yes	No	Yes
Mode 3 Implicit I/O cycle	Yes	No	No
Addressed I/O or mem cycle	No	Yes	Yes

3.4 Data Sizes and Wait States

As a Bus Master

As a bus master, the 82C614 determines the data size of the addressed MicroChannel slave by sampling the -DS16RTN signal. The 82C614 is a 16 bit master. 16 bit cycles to 8 bit devices will be done in two transfers. 32 bit devices are seen by the 82C614 as 16 bit slaves. The system board takes care of the data bus and byte select translations for 32 bit slaves.

As a bus master the 82C614 will be able to perform 200nS default cycles on the MicroChannel and 100nS streaming data cycles. Bits 0 & 1 of register 07 allow the timing to be relaxed, changing the default cycle to 300nS. Exactly which parameters are relaxed will be in a future revision of the data sheet.

As a MicroChannel Slave

The 82C614 is a 16 bit slave when its internal registers are accessed. When accessing a peripheral on the local bus the 82C614 will respond as either an 8 or 16 bit slave, depending on the data size of the local peripheral (see the section below on the local bus to see how this is determined).

When accessing internal registers the 82C614 can be accessed in either 0 or 1 wait states (it is programmable). When accessing a peripheral on the local bus, the number of MicroChannel wait states will be determined by the timing on the local bus. This will include the time to arbitrate for the local bus, and the time to perform the actual local bus cycle. See the section below on local bus accesses. If buffered writes are being used, most write cycles to the local bus can be done in 0 wait states. A previous section on MicroChannel transfers discusses this further.

On the Local Bus

On the local bus the 82C614 must know the data size and timing requirements of each peripheral. These are programmed into the 82C614 registers. A device can be programmed as 8 or 16 bits (a 32 bit migration path is provided in the register definitions at some places, but is ignored in the 82C614). A device can also be programmed for 0, 1, 2, or 3 wait states. In addition, any device may pull the READY line low to add additional wait states.

The data size and wait states for a peripheral are determined by how it is selected. Each peripheral is selected with one of the following (the signal names are in parenthesis):

- A programmable Decode (CS 0-3).
- A fixed Decode (CS 4-8) (Multifunction pins).
- A DMA Acknowledge (DACK 0-3).
- External MicroChannel Address Decoding.
- External Local Bus address decoding.

These are discussed in the following paragraphs:

Programmable Decodes

The Programmable Decodes are individually programmed with a data size and number of wait states through their Control Registers (39, 3B, 3D, & 3F).

Fixed Decodes

The Fixed Decodes use Register 08 for the data size and wait states. Two bits control the data size, one for Decodes 4-7 and one for Decode 8. The number of wait states is programmed the same for all 5 fixed decodes.

Implicit I/O

If Implicit I/O is used by a DMA controller (using a DACK pin), that DMA controller's Control register contains the data size. The number of wait states is programmed by register 09. There are two bits in that register for each DMA channel.

External MicroChannel Address Decoding

If External MicroChannel Address Decoding is used, the data size may come from two different places. A multifunction pin may be programmed to provide the data size dynamically. This is useful if more than one device is using external decode, and they are different data sizes. The pin is pulled low to indicate 16 bit. If only one device or multiple devices which all have the same data size are using external MicroChannel decode, the data size may be programmed into Register 08 bit 5, allowing the multifunction pin to be used for something else. If the data size is provided externally by the multifunction pin, that pin will only be sampled for externally decoded cycles, so it's state does not matter when the decode pin is inactive. Note that the register bit should be set to a 0 if the multifunction pin is used, since it is an OR function internally. Bus cycles decoded using external MicroChannel decoding will be 0 wait states on the local side unless the 82C614 is programmed to add wait states to ALL local cycles. The device may pull the local side READY pin low to extend the cycle. The 82C614's DMA channels cannot access peripherals through this decoding method.

External Local Bus Address Decoding

External Local Bus Address Decoding without using a Decode pin is possible, but not recommended. A device using only external local bus address decoding can only be accessed through the DMA controllers, using a programmed address. Since no Decode pins are active, it will default to 8 bit 0 wait state.

Note that it is possible that more than one decode may be active at the same time. If this happens, the data size and wait state information for all active chip selects will be used. If any active chip select is programmed for 16 bit, the cycle will be 16 bit. The highest number of programmed wait states will be used.

Register 08 bits 6&7 may be programmed for the minimum number of wait states for the local bus. This will add 0, 1, 2, or 3 wait states to all cycles. These wait states are not added to the wait states programmed elsewhere, it simply sets the minimum.

The following summary shows where the data size and wait state information is obtained for each decode.

Decode	Data Size	Wait States
Decode 0	Reg 39 Bit 2	Reg 39 Bits 0-1
Decode 1	Reg 3B Bit 2	Reg 3B Bits 0-1
Decode 2	Reg 3D Bit 2	Reg 3D Bits 0-1
Decode 3	Reg 3F Bit 2	Reg 3F Bits 0-1
Decode 4	Reg 08 Bit 2	Reg 08 Bits 0-1
Decode 5	Reg 08 Bit 2	Reg 08 Bits 0-1
Decode 6	Reg 08 Bit 2	Reg 08 Bits 0-1
Decode 7	Reg 08 Bit 2	Reg 08 Bits 0-1
Decode 8	Reg 08 Bit 3	Reg 08 Bits 0-1

Decode	Data Size	Wait States
DMA 0 Implicit I/O	Reg 95 Bit 6	Reg 09 Bits 0-1
DMA 1 Implicit I/O	Reg B5 Bit 6	Reg 09 Bits 2-3
DMA 2 Implicit I/O	Reg D5 Bit 6	Reg 09 Bits 4-5
DMA 3 Implicit I/O	Reg F5 Bit 6	Reg 09 Bits 6-7
Ext uChan Dec.	Reg 8 Bit 5[1]	None
Ext Loc Dec.	8 Bit only	None
Minimum wait states for all	-	Reg 08 bits 6-7

Note 1: Multifunction pin #1 may be programmed to provide the External Micro Channel data size dynamically. If it is, that pin is inverted, and ORed with Register 8 bit 5.

Local Bus Accesses from the MicroChannel

When the MicroChannel accesses a local peripheral it will be caused by the address decode sections of either a programmable decode, a fixed decode, or an external decode being activated. The data size and wait state information from the decode which is activated will be used. The data size information must be sent to the MicroChannel as soon as the address is decoded. Because of the programmability of the decodes, it is possible for more than one to be active at one time. The data sizes from all decodes which are activated will be ORed together, so that if any of them indicate a data size of 16 bit, the access will be 16 bit. Likewise, the programmed wait state information will decode separate 1, 2, and 3 wait state signals. These will be ORed from all active decodes to produce the highest number of wait states programmed into any activated decode.

Example:

The 82C614 register set occupies the I/O addresses 0800-08FF.
This places Decode 8 at address 0860-087F.
Programmable Decode number 2 decodes I/O address 0860-086F.
The system processor reads I/O port 0862.
Decode #8 (a fixed decode) and Decode 2 (a Programmable decode) both are activated.

Decode 8 is programmed to 8 bit 2 wait states.
Decode 2 is programmed to 16 bit 1 wait state.
The access will be 16 bit 2 wait state.

Local Bus Accesses by a 82C614 DMA Controller

Each Programmable decode has bits to activate the decode for any of the DMA channels (or multiple DMA channels). The fixed decodes may also be activated for DMA channels, but not as universally. Each fixed decode has one DMA channel assigned which it may be programmed to be activated for. This is done by programming the multifunction pin which contains that decode.

For Local Bus DMA cycles, the data size and wait state information comes from EITHER the Decode Programming OR the Implicit I/O programming. Where the information comes from is determined by the following table, showing the DMA modes:

Local Bus DMA data size & wait state source

DMA Mode	Data Size & Wait State Info Source
Mode 0 Addressed memory	Decode Programming
Mode 1 Addressed I/O	Decode Programming
Mode 2 Implicit I/O	Implicit Registers
Mode 3 Implicit I/O cycle	Implicit Registers
Addressed I/O or mem cycle	Decode Programming

When the Decode Programming is used, whichever decode is programmed to be activated for the particular DMA channel will provide the information. If more than one is activated, the same ORing occurs as mentioned above. When the Implicit registers are used, they provide the information, and any decodes programmed to be activated for that channel are NOT used.

As always, all types of local bus DMA cycles use Register 08 bits 6-7 to set the minimum number of wait states, and any cycle may be extended if the local peripheral pulls READY low.

INIT ROM data size and wait states

INIT ROM cycles are always 8 bit. Data is taken from AD0-7. The address is incremented by two, however, so that if a 16 bit BIOS ROM is used for the data, consecutive bytes of the even word will be read. 3 wait states are always added for INIT ROM accesses.

3.5 CHCK Interrupt

In keeping with the MicroChannel specification, the 82C614 drives the -CHCK interrupt only when it is a slave. The 82C614 may drive CHCK low when it detects a data parity error when being written to, or if the -CHCKIN pin is driven active from the local bus during a MicroChannel access to the local bus.

A write data parity error will be detected only when POS3 bit 5 =1 (enabling parity) and -DPAREN is low for the bus cycle. The Parity error will be latched, causing register 0B bit 0 to be a 1. Register 0A bit 0 is a mask bit for the write data parity error CHCK generation. The parity error is ANDed with this bit before being sent to the CHCK logic. Data parity will only be checked on the data busses being used to transfer data. This is determined by A0, -BHE, -CDDS16 (driven by the 82C614 with the data size of the local bus slave, or 16 bit for internal registers).

When the MicroChannel is performing a bus cycle to a device on the 82C614's local bus, that device, or other logic on the local bus may activate the -CHCKIN line. This will set register 0B bit 1 to a one, and if enabled by register 0A bit 1, will cause a CHCK on the MicroChannel. This will cause -CHCK on the MicroChannel to go active in the middle of the bus cycle. In order to satisfy the MicroChannel timing specs for synchronous -CHCK, the 82C614 will begin sampling the -CHCKIN pin at the start of the local bus command, and end sampling 25nS before the end of the command (sampling actually ends when CDCHRDYRTN is returned active on the MicroChannel). If -CHCKIN is low at any time during sampling period, it will be latched and sent to the MicroChannel (if enabled). The -CHCKIN pin will not cause a -CHCK on the MicroChannel if it occurs during a buffered write, since the MicroChannel bus cycle has already been completed before the CHCK can be indicated.

When the 82C614 generates a CHCK, POS5 bits 6 & 7 will both be set to 0s. Bit 7 indicates that the 82C614 has generated CHCK, while bit 6 indicates that CHCK information is contained in POS6 & 7 (POS6 in the case of the 82C614). POS6 will contain the AND of registers 0A and 0B while POS5 bit 6=0. Writing a 1 to POS5 bit 7 will reset the error condition by setting POS5 bits 6 & 7 back to 1s, and clearing register 0B. The individual interrupts in register 0B may also be cleared by writing 1s to the respective bits. Writing 0 to a bit will leave it unchanged.

-CHCK is generated synchronously, and for the duration of the bus cycle only.

As a bus master, the 82C614 samples -CHCK during bus cycles it initiates. If -CHCK is active during a bus cycle, the 82C614 will set error bit(s) in the status register of the DMA channel being serviced by the bus cycle. The DMA channel may be programmed to either halt or continue after an error has been detected. Detection of a -CHCK will set one or more of the following DMA error bits.

Status Register (xx94, xxB4, xxD4, xxF4)

Bit	Error Detected
2	-CHCK detected during a write cycle to the MicroChannel.
3	-CHCK detected during a read cycle from the MicroChannel.

Secondary Status Register (xx93, xxB3, xxD3, xxF3)

Bit	Error Detected
2	Error occured during a linked list read for this channel.
3	Error occured during a streaming data cycle.

3.6 IRQ Interrupts

There are 8 sources for the standard interrupt: the End of Operation status for each of the DMA controllers, and 4 external interrupt pins. One of the external interrupts is a dedicated pin while the other 3 are multifunction pins. Register 0C individually enables the interrupts. Register 0D indicates which devices are interrupting. Register 0D will indicate an interrupting condition even if that interrupt is not enabled. The DMA End of Operation interrupts may be cleared by writing a 1 to the corresponding bit of register 0D. The external interrupts must be cleared by clearing the external interrupting source.

The destination of the interrupt is also programmable. Register 4 indicates whether or not the interrupt goes to the MicroChannel. POS5 bits 0 & 1 indicate which MicroChannel interrupt pin will be used. There are two dedicated pins and 2 multifunction pins which may be used as MicroChannel interrupts. This allows the POS to select which interrupt level on the bus to use. Only one will be used at a time. The dedicated pins may be connected directly to the MicroChannel. Any multifunction pins used as MicroChannel interrupts must be buffered with open collector non-inverting buffers.

3.7 INIT ROM

The INIT ROM is an 8 bit wide 64 location PROM. Following RESET, the PROM is downloaded into the 82C614. The 82C614 register address, the Programmable decode address programming, the multifunction pin assignments, and other configuration information is stored here. Locations 00-3F of the INIT ROM are loaded into 82C614 registers 00-3F respectively. Note that some of the registers or bits within registers are Read Only, and are not written by the INIT ROM. The 82C614 will read all 64 bytes from the INIT ROM, even if the byte is not used. Read only or unused bits should be programmed to 0 in the INIT ROM for compatibility with any future changes to the chip. The first two locations of the init ROM are not used, since these are read only registers, and will be in all future revs. These two locations do not need to be set to 0, and may contain revision or check sum information, or whatever the board designer wants.

Until the 82C614 is finished loading the INIT ROM, POS0 & 1 return 00 when read, regardless of the value in the registers, & all I/O is disabled from the MicroChannel side, except the POS registers.

The INIT ROM can either be a fuse link PROM , or a section of the BIOS ROM. Each INIT ROM read cycle has the same timing as a memory read cycle, with a few exceptions. The address which is issued with ALE has the INIT ROM address on LAD1-6, and 1s for LAD7-15. After ALE goes low, LAD0-7 become inputs for the data, and LAD8-15 remain outputs, and contain the INIT ROM address. -MEMR and -INITROM go low at the same time. -BHE will be a 1 and A0 will be a 0.

If a fuse link prom is used, LAD8-13 are hooked to its address lines, LAD0-7 are hooked to its data lines, and -INITROM is hooked to the output enable. If a section of the BIOS ROM is used, the addresses are such that the INITROM cycles read the last 64 locations of the ROM. If an 8 bit BIOS ROM is used, every other location at the end of the ROM is read. If a 16 bit ROM is used, consecutive locations of the low byte will be used. If it is desirable to use locations other than at the end of the ROM, the -INITROM signal can be ANDed with an address line.

During RESET the -INITROM pin is tristated, and is an input. There is a weak pullup resistor to VCC inside the chip. At the end of RESET, the 82C614 samples the -INITROM pin.

- If it is high, the -INITROM pin has the same timing as -MEMR for the init ROM cycles. All -CS pins will be high. The addresses are driven as described above.

- If it is low, the -INITROM pin is driven low for the entire time the INIT ROM is being read, the -CS1 pin is driven low for each INITROM cycle, with the same timing as the -MEMR pin. AD8-15 will be driven with 1s the entire time if -INITROM is sampled low at the end of RESET. A BIOS ROM would normally be connected to -CS1.

  At the end if the INIT ROM sequence, the -INITROM pin is either tristated, or driven high, depending on the value of register xx0E bit 7 (the register has now been loaded by the INIT ROM). This allows an absolute minimum of external logic for several configurations. The following are some of the ways the INIT ROM can be hooked up:

- Separate Fuse Link PROM. Address lines hooked to AD8-13, output enable hooked to -INITROM. Data lines hooked to AD0-7. No external logic.

- Part of BIOS ROM (last 64 even numbered bytes). Tie -INITROM to ground. Connect -CS1 to the output enable of the EPROM(s). Connect the latched address lines to the EPROM (If the 82C614 local side will be programmed for 8 bit mode, AD8-15 may be connected directly to the EPROM upper address lines). Program Register 0E bit 7 to a 1 so that the 82C614 tristates the -INITROM signal after loading. No external logic.

- Same as above, except INIT ROM data is located somewhere other than the end of the BIOS ROM. Connect the same as the previous example, except pull -INITROM low with a pulldown resistor. Use the -INITROM signal to modify an address bit to the BIOS ROM to have it read the desired locations. The -INITROM signal will be driven low until the init data is loaded. Program Register 0E bit 7 to a 0 so that the 82C614 drives -INITROM high after loading. An open collector inverter from RESET may be used instead of the pull down resistor if there is too much TTL loading for a pulldown to work properly.

The read strobe for the INIT ROM will be equivalent to the 3 wait state cycle timing.

3.8 Programmable Decodes

Four programmable decodes are provided which provide chip selects for memory or I/O cycles. One is completely programmable, with a 32 bit address compare, decoding a memory or I/O block anywhere in the address space. Another has a 20 bit address, and may decode any I/O address, or a memory address in the bottom 1M. The other two are I/O only.

There are two ways which a peripheral or memory on the local side may be accessed:

1. From the MicroChannel (usually by the system processor, but potentially by any MicroChannel master). This includes register accessing of peripherals, BIOS ROM accesses, and RAM buffer accesses.

2. By an 82C614 DMA channel. Normally the DACK signals are used as DMA chip selects, but providing a programmable chip select decode for DMA will save gates in some implementations.

The decoding on the MicroChannel bus not only provides a chip select for a memory or peripheral device, it also provides the indicator to the 82C614 of what address ranges it should respond to as a MicroChannel slave. When the MicroChannel produces address and status information which triggers one of the programmable decodes, the 82C614 pulls the CDCHRDY line low and immediately begins arbitrating for use of the local bus. When the local bus is free, the appropriate decode line is activated and the cycle is performed.

Decoding for the MicroChannel is as follows:

- Each of the address lines may be compared to a 0, 1, or don't care. This is implemented with an address compare register, and a 32 bit address mask. A 1 in a mask bit indicates a don't care for that bit. (Decode 0 compares 32 address bits, decode 1 compares 20 address bits, and decodes 2 & 3 compare 16 address bits).

- POS bits may be used for address compare instead of some of the bits in the 32 bit registers, as explained later.

- A programmable bit decides whether the decode is active for Memory cycles or I/O cycles. Two bits decide whether the decode is active for Reads and/or Writes.

- The decode pin (-CSn) will not become active until the local bus is arbitrated for, and the bus cycle is initiated.

- A programmable bit decides whether the decode is a Chip Select or a Strobe. A Decode is valid with some setup and hold time to the command strobe. A Strobe has the same timing as the command strobe. A decode may glitch at address transition times. A strobe will not glitch, and may be connected to the clock or clear inputs of a flip flop. The following page shows a functional block diagram of the MicroChannel decoding section of Decode 0.

Decoding for the DMA channel is far simpler. There is a bit for each DMA channel. If the bit is a 1, the programmable decode is active during accesses by that DMA channel. The same command type decoding (memory or I/O, read and/or writes) which is used for the MicroChannel will be used for DMA cycles. The decode will NOT be active for DMA operations to or from Implicit I/O ports (ports addressed with only a DACK signal, and no address lines).

The programmable decode pin is the OR of the MicroChannel decode and the DMA decode.

POS relocation for Programmable Decodes:

In order to allow multiple identical adapter boards, with identical INIT ROMs to reside in the same system, it is necessary to allow POS information to relocate the local peripherals. The 82C614 has three levels of POS relocation. One is optimized for relocating an I/O device, one for relocating a ROM BIOS, and one for relocating a RAM buffer. Each decode may be programmed to use one of these relocation methods, or no relocation at all. Each relocation method is described below:

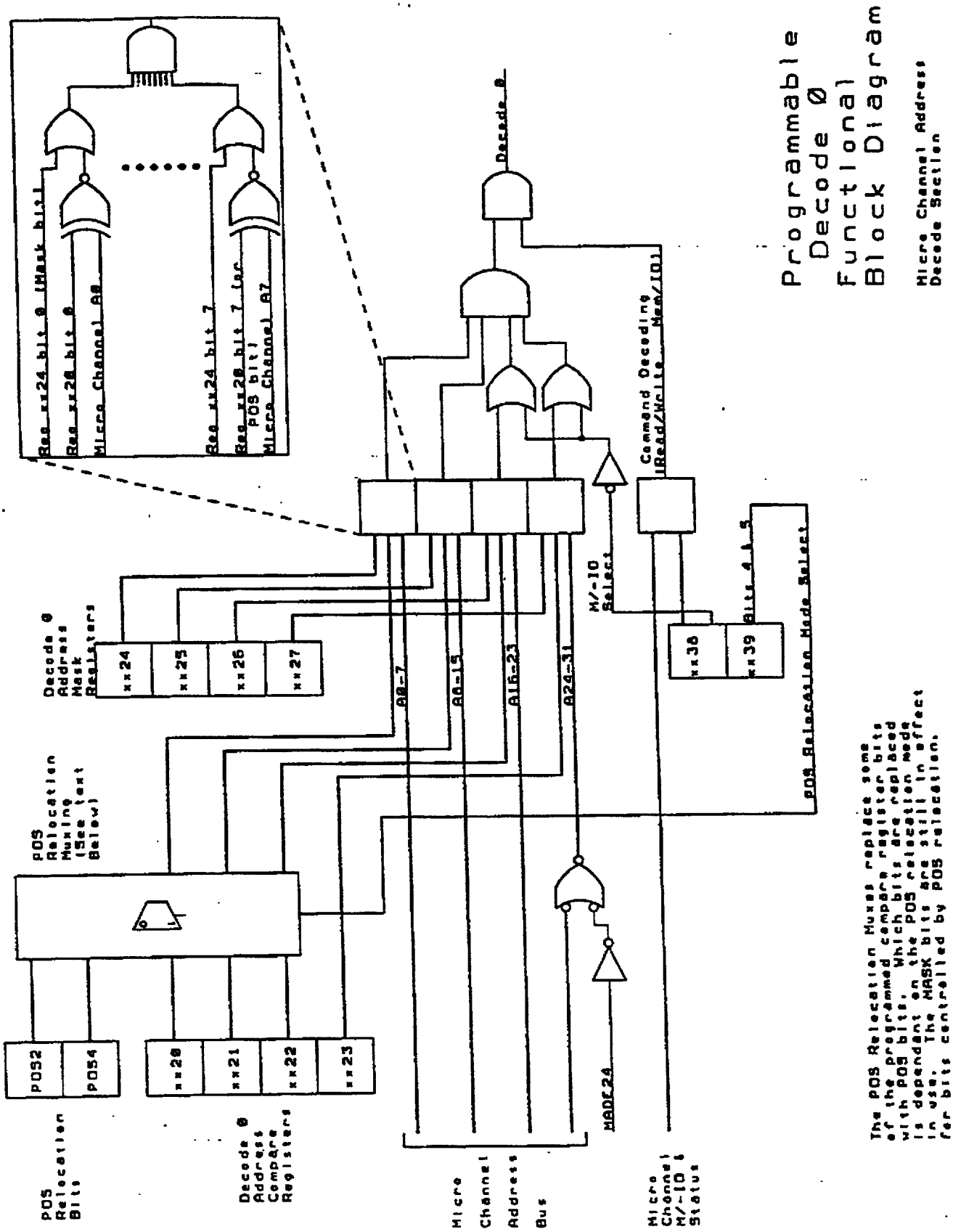
- **128 byte relocation.** This is optimized for I/O devices. There are two modes for 128 byte relocation. The mode is set on a chip wide basis, and cannot be set individually for each decode.

  Mode 0: POS4 bits 4-7 specify address bits 7-10 of each decode programmed for 128 byte relocation. This provides 16 different I/O locations available for 128 byte relocation.

  Mode 1: POS4 contains 2 bits for each programmable decode. These bits specify address bits 7-8 of the respective decode. This mode is useful when peripherals on the local bus already have specific commonly used addresses on the MicroChannel, such as serial ports, parallel ports, or disk controllers, and the 82C614 is providing a superset of the normal peripheral. In this case it may be necessary to relocate decodes individually. The bit assignments are: 0-1 Decode 0, 2-3 Decode 1, 4-5 Decode 2, 6-7 Decode 3.

- **8K byte relocation.** This is optimized for ROM BIOSes, which normally reside in the C0000-DFFFF range. POS2 bits 4-7 specify address bits 13-16 for each decode which is programmed for 8K relocation. This allows all 16 ROM areas to be programmed.

- **128K relocation.** This is optimized for a RAM buffer. POS4 bits 0-3 specify address bits 17-20 for any decode programmed for 128K relocation. Note that this uses some of the same bits as 128 byte relocation in mode 1. If 128k relocation is used at the same time as Mode 1 of 128 byte relocation, decodes 0 & 1 should generally not be programmed to use 128 byte relocation, although doing so will not cause improper operation.



Subset implementation of Programmable Decodes:

The full implementation of the programmable decodes takes a considerable number of registers. It is doubtful that all 4 decodes will require the full implementation. To reduce complexity, 3 levels of support are specified:

- Level A — Full implementation (32 bit address compare and mask).
- Level B — I/O or BIOS ROM only. Address bits 20-31 read as 0s, mask bits 20-31 read as 0s, memory cycles are always decoded with A20-31 low (actually, A20-23 low and MADE24 high). 128 byte and 8K relocation are allowed, but not 128K relocation.
- Level C — I/O only. Address bits 16-31 read as 0s, mask bits 16-31 read as 1s, Memory read and memory write select bits read as 0s. Only 128 byte relocation allowed.

The implementation of the 82C614 is as follows:

Decode 0	Level A
Decode 1	Level B
Decode 2	Level C
Decode 3	Level C

3.9 Fixed Decodes

Five of the multifunction pins may be programmed as fixed decodes. The fixed decodes are for I/O only. They decode the 5 "holes" in the 82C614 register area, and therefore are relocated by POS2 bits 1-3 along with the 82C614 registers. They are active for I/O reads and writes. They may each be optionally active for a DMA channel (selected by multifunction pin programming). Each is decoded as follows, where xx is the assigned area for the 82C614 registers, as determined by the init ROM and the POS:

Decode #	I/O Range	# of Ports	DMA CH
4	xx98-xx9F	8	0
5	xxB8-xxBF	8	1
6	xxD8-xxDF	8	2
7	xxF8-xxFF	8	3
8	xx60-xx7F	32	0

Register xx08 selects the number of wait states, the data size, and whether buffered writes are allowed for the fixed decodes.

3.10 Data Parity

The 82C614 supports data parity on the MicroChannel bus. POS3 bit 5 determines whether data parity is enabled or disabled. If this bit is a 0, -DPAREN and DPAR0-1 will not be driven and will be ignored as inputs.

As a slave, the 82C614 will generate parity during read cycles by driving the DPAR0-1 pins along with the data, and activating -DPAREN when -CMD is low. For write cycles, when -DPAREN is active, the 82C614 will check data parity and indicate an error on the -CHCK pin if enabled.

As a Bus Master, for write cycles the 82C614 will produce parity information on DPAR0-1 and drive -DPAREN active. For read cycles, the 82C614 will check parity errors if -DPAREN is active, and indicate a parity error in the status register of the DMA channel being serviced.

3.11 Streaming Data

The 82C614 supports streaming data cycles of 100nS when a Bus Master. This allows the 82C614 to fill or empty its FIFOs at a much higher rate than the basic cycle. POS3 bit 7 determines whether streaming data cycles may be used. Streaming data cycles will only be performed when the addressed slave also supports streaming data.

When a Bus Master, the 82C614 will monitor -SDR0 and -SDR1 to determine if the addressed slave is capable of supporting streaming data. If -SDR0 or -SDR1 is active at the specified time (for the standard or deferred timing) and the address is on a double word boundary (A1-0 = 00) the 82C614 will pull -SDSTROBE low, and perform streaming data cycles until either the FIFO is empty (or one byte from empty), the 82C614 is preempted off the bus, or the slave terminates the streaming transfer.

When the 82C614 begins a bus cycle, if the address is not double word aligned, it will perform basic cycles until the address becomes double word aligned before it begins a streaming data cycle. This may include one byte and one word transfer. If the 82C614 detects one byte remaining in the FIFO while performing a streaming data transfer, the transfer will be terminated, and the byte will remain in the FIFO until the FIFO trigger point is reached again. This avoids performing two byte transfers instead of one word transfer, which may be a streaming data transfer. If the particular DMA channel has reached terminal count, the final byte will be transferred using a basic cycle.

The 82C614 may use streaming data transfers to empty or fill a FIFO, or to read a linked list entry into a DMA controller. Linked list entries should be on a double word boundary to provide the fastest transfers. Note that linked list entries MUST be on a word boundary for proper operation. DMA addresses should also be on a double word boundary to support the fastest transfers. DMA addresses may be on a word or byte boundary if required, however. No streaming data cycles will be done if the starting address is on an odd byte boundary (all transfers will be byte transfers).

Streaming data cycles to or from memory on the MicroChannel cause the data to go to incrementing addresses. The 82C614 will increment the address by two (one word) on each data transfer, and the memory slave will do the same. Streaming data cycles to or from I/O ports on the MicroChannel will access the same address cycle after cycle. Streaming data on the MicroChannel does not support non-incrementing memory accesses or incrementing I/O addresses. The DMA channel also does not support either of these since they are not very useful.

If the slave indicates that it is an 8 bit streaming data device (-DS16RTN is not active and -SDR0 is active) the 82C614 will do standard, non streaming cycles.

When the MicroChannel side of the 82C614 becomes a bus master, it reprioritizes the FIFO requests and linked list transfer requests after each bus cycle (linked list reads are always done consecutively, however). A streaming data transfer is considered one bus cycle in this priority scheme, and will not be interrupted by a reprioritization.

3.12 Extended POS

Extended POS is a way for the system to access additional registers or data blocks through the POS. The 82C614 allows the 256 byte register set to be accessed through Extended POS.

Extended POS uses POS6 and POS7 as a pointer, POS3 as the data window for odd register accesses, and POS4 as the data window for even register accesses. When POS7 is 00, extended POS is disabled, and POS3 and POS4 act as regular POS registers. POS6 & 7 power up to 0000, so that POS3 and POS4 are immediately available for systems which do not use the extended POS. Any value other than 00 in POS7 changes POS3 and POS4 to data windows. The 82C614's register set is mapped into these windows when POS7 = 01. All other combinations are reserved at this time. Note that 5 areas of the 82C614 register set may be mapped to peripherals on the local bus. Accesses to these addresses will cause a bus cycle on the local bus, just as if it was accessed through a normal I/O cycle.

POS7	POS6	POS4 accesses go to:
00	XX	Regular POS3 and POS4 (Extended POS disabled).
01	00-FF	82C614 Registers 00-FF.
02-FF	XX	No Operation. Reserved.

Register xx04 bit 2 must be a 1 for extended POS to be enabled. This bit is determined by the INIT ROM. If Extended POS is disabled, all accesses to POS3 and POS4 access the normal POS3 and POS4 registers, regardless of the value of POS6 & POS7.

Note that after the 82C614 has generated a -CHCK, POS6 and POS7 switch functions, and provide -CHCK status information, until the -CHCK status is reset through POS5. Extended POS continues to function during this time, the pointer registers are just not available for reading or writing.

Extended POS accesses are performed even if the Card Enable bit in POS2 is 0.

3.13 Multifunction Pins

In addition to the standard local bus signals, there are many signals which some local peripherals may require, or that may reduce the chip count of the adapter board if they were provided. There are not enough pins on the 82C614 to provide all of these signals. For any given design, a subset of these signals may be provided by using the 8 Multifunction pins. Each multifunction pin may be programmed to one of 16 different functions, 8 of which are inputs and 8 are outputs. Not all combinations of each Multifunction pin has been assigned, allowing future expansion. The INIT ROM programs the registers which select what signal is present at each Multifunction Pin. These initial setting, selected by the board designer, may be overridden by writing to the registers controlling the Multifunction pins.

If a Multifunction pin is to be not used, it should be programmed to selection 0, making it an input bit. Many of the signals are available on more than one Multifunction pin. This is done to allow as many combinations of signals as possible to be used by one adapter card. The same output signal may be programmed to more than one Multifunction pin with no problems resulting. Programming more than one Multifunction pin to the same input signal may cause unpredictable results. The Inputs will probably be ORed inside the 82C614, but this cannot be counted on, and may change from Rev to Rev, unless specifically included in the spec. Any combination of Multifunction Pins may be programmed as Input Ports, since each has its own bit in the input register.

The following is a "pin description" of each signal which may be provided on a Multifunction Pin. The Multifunction pins which may be programmed to provide the signal are listed in the MFP# column. All outputs are 4mA Totem Pole.

Multifunction Pin Definitions

Inputs:

Signal	Type	MFP#	Description
Input Port	I	0-7	This is the default state. Unused Multifunction pins should be programmed to this. It is selection 0 for all 8 pins. When programmed as an input bit, the state of the pin can be read through register 0F. MFP0 is bit 0, MFP1 is bit 1, etc. Actually, Register 0F will read the state of each pin regardless of its programming (even if an output), but programming it as an Input Port guarantees that the pin will not be used for any other function within the 82C614.

Local Side Input Signals

Signal	Type	MFP#	Description
-Local Int 1 -Local Int 2 -Local Int 3	I I I	1,5 2,6 3,7	Additional local interrupt inputs. Active Low. Local Int 0 is a dedicated pin. Three more interrupt inputs may be programmed so that multiple peripherals may each have an interrupt line. If any of these interrupt inputs are not programmed to appear on a pin, they are forced to a 1 (inactive) internally.

MicroChannel Side Input Signals

Signal	Type	MFP#	Description
-Ext Decode	I	0,2	Active low MicroChannel decode. Used if the programmable and fixed decodes are not sufficient for a complex decode. Should be an unlatched decode of the status and address lines only. When this signal is low at the beginning of a MicroChannel cycle, the 82C614 will be the addressed slave for that cycle, and arbitrate for the local bus. If neither pin is programmed to this, the external decode will always be inactive. External logic should decode M/-I/O and the address lines (including MADE24 if a memory decode). This decode must be done in 35nS or less in order to allow the 82C614 to respond with -CDDS16, CDCHRDY and -CDSFDBK in time (-CDDS16 is the critical path).
Ext Data Size	I	1,7	Data size for the external decode. 0=16 bit, 1=8 bit. Internally inverted, then ORed with Register 08 bit 5. Sampled only when Ext Decode is active. This pin is only useful if there is more than one device using External MicroChannel Decoding, and the data sizes of the devices are different. The programmable bit (register 8 bit 5) may be used in all other cases. This pin must be stable within 35nS of the MicroChannel address and M/-I/O becoming valid. If no pin is programmed to provide this function, it defaults to a 1.

MicroChannel Side Input Signals (continued)

Signal	Type	MFP#	Description
Slot Size	I	1,3,7	Indicates whether the adapter card is plugged into a 16 or 32 bit slot. Should be tied to one of the GND pins of the 32 bit section of the connector and a pullup resistor. 0=32 bit slot, 1=16 bit slot. This pin performs no 16 or 32 bit switching directly. Software may read register 07 to read this information, and program the 82C614 logic for either a 16 or 32 bit slot.
-REFRESH	I	2,4	When low, disables the address decoders for the Programmable Decodes. This prevents the 82C614 from responding as a slave (and adding wait states) during refresh cycles. *It is not* expected to be required on most systems. During a refresh cycle the upper address lines will be either driven low, or floating high. In both cases the 82C614 is not likely to be a memory slave at that address.

Outputs:

Signal	Type	MFP#	Description
Output Port	O	0-7	Any pin programmed as on Output Port will be an output controlled by software. The system processor may write to the bit through register 0F. MFP0 uses bit 0, MFP1 uses bit 1, etc.

Local Side Output Signals

Signal	Type	MFP#	Description
A0 A1 A2 A3	O O O O	0, 4 1, 5 2, 6 3, 7	Latched Local address bits 0-3. These pins may provide the latched address bits, to avoid putting an external latch on the board. Note that if only 8 bits of data are needed, AD8-15 may be configured as latched address lines also. See the section on the local bus for details.
A16 A17 A18 A19 A20 A21 A22 A23	O O O O O O O O	0, 5 1, 7 2 3 4 5 6 7	Local address bits 16-23. These address bits allow memory greater than 64K to be on the local bus. During MicroChannel accesses to the local bus, the MicroChannel addresses 16-23 will be latched and copied onto these lines. During DMA cycles, the register for local address 16-23 will be placed on these lines.
-CS4 -CS5 -CS6 -CS7 -CS8	O O O O O	0 1 2 3 4	Chip selects 4-8. Active Low. These are the Fixed Decodes, which decode the unused I/O areas within the 82C614 register set. -CS4-7 decodes an 8 I/O port range while-CS8 decodes a 32 I/O port range. The decodes may be programmed to be active only for MicroChannel accesses, or both MicroChannel accesses and DMA accesses to one channel. Each of these chip selects has one particular DMA channel which it may be activated for. If a decode must be active for more than one DMA channel, a Programmable Decode (-CS0-3) should be used instead, or external logic may be used to gate the DACK lines.
-Terminal Count	O	1, 5	DMA Terminal Count. Active during the last local bus cycle of a DMA channel. If the cycle is Local to Local, it will be active for both cycles.

Local Side Output Signals (continued)

Signal	Type	MFP#	Description
AEN	O	2, 6	Address enable. Similar to the signal of the same name on the AT bus. This signal will be high for DMA cycles to Implicit I/O ports. It will be low for all MicroChannel Accesses to the local bus, and DMA cycles to addressed Memory or I/O.
-EXT Cycle	O	2	This signal goes low to indicate that the bus cycle being performed on the local side was initiated by the External Decode from the MicroChannel. It has the same timing as a Chip Select line.
-LS0 -LS1 LM/-I/O	O O O	5 6 7	Local -S0, -S1, and M/ -I/O. These signals may be used if the peripheral being attached to the local bus has an interface which looks more like the MicroChannel than the AT bus. They have the same definition as the same signals on the MicroChannel bus. They are all activated with ALE.
POS5 Bit 3 POS5 Bit 4	O O	6 7	POS register 5 bits 3 and 4. Allows two bits of POS information to be passed to the peripherals.

MicroChannel Side Output Signals

Signal	Type	MFP#	Description
-IRQC -IRQD	O O	1, 5 2, 6	Additional MicroChannel interrupts. These pins allow additional MicroChannel interrupts to be hooked to the 82C614, allowing the system to choose which interrupt is used by programming the POS. Only one interrupt will ever be activated at any one time. The rest will be high. The Multifunction pins do not have the drive capability to drive the MicroChannel directly, so an open collector buffer should be used, and pullup resistors placed on the input, so none of the pins are driven before the 82C614 is configured. -IRQA and -IRQB are dedicated pins, and are capable of driving the MicroChannel directly.

3.14 Multifunction Pin Programming

This table lists what signal will be provided on each Multifunction Pin when programmed as shown. Blank entries are reserved, and should not be programmed.

MFP0
Reg 1C Bits 3-0

Inputs		Outputs	
0	Input Port D0	8	Output Port D0
1		9	A0
2		A	-CS4 no DMA
3		B	-CS4 w/DMA0
4		C	
5		D	
6	-Ext Decode	E	
7		F	A16

MFP1
Reg 1C Bits 7-4

Inputs		Outputs	
0	Input Port D1	8	Output Port D1
1		9	A1
2	-Local Int 1	A	-CS5 no DMA
3		B	-CS5 w/DMA 1
4		C	-IRQC (to uC)
5		D	-Terminal Count
6	Ext Data Size	E	
7	Slot Size	F	A17

MFP2
Reg 1D Bits 3-0

Inputs		Outputs	
0	Input Port D2	8	Output Port D2
1		9	A2
2	-Local Int 2	A	-CS6 no DMA
3		B	-CS6 w/DMA3
4		C	-IRQD (to uC)
5		D	AEN
6	-Ext Decode	E	
7	-Refresh	F	A18

MFP3
Reg 1D Bits 7-4

Inputs		Outputs	
0	Input Port D3	8	Output Port D3
1		9	A3
2	-Local Int 3	A	-CS7 no DMA
3		B	-CS7 w/DMA 3
4		C	
5		D	
6		E	
7	Slot Size	F	A19

MFP4
Reg 1E Bits 3-0

Inputs		Outputs	
0	Input Port D4	8	Output Port D4
1		9	A0
2		A	-CS8 no DMA
3		B	-CS8 w/DMA0
4		C	
5		D	HOLD
6		E	Ext Cycle
7	-Refresh	F	A20

MFP5
Reg 1E Bits 7-4

Inputs		Outputs	
0	Input Port D5	8	Output Port D5
1		9	A1
2	-Local Int 1	A	A16
3		B	
4		C	-IRQC (to uC)
5	HLDA	D	-Terminal Count
6		E	-LSO
7		F	A21

MFP6
Reg 1D Bits 3-0

Inputs		Outputs	
0	Input Port D6	8	Output Port D6
1		9	A2
2	-Local Int 2	A	POS5 bit 4
3		B	
4		C	-IRQD (to uC)
5		D	AEN
6	-CS614	E	-LS1
7		F	A22

MFP7
Reg 1D Bits 7-4

Inputs		Outputs	
0	Input Port D7	8	Output Port D7
1		9	A3
2	-Local Int 3	A	POS5 bit 5
3		B	A17
4		C	
5		D	-LocInt Out
6	Ext Data Size	E	LM/-I/O
7	Slot Size	F	A23

4.0 PIN SUMMARY

4.1 MICROCHANNEL PINS

	QTY
A0-31	32
MADE24	1
D0-15	16
DPAR0-1	2
-DPAREN	1
ARB0-3	4
ARB/-GNT	1
-PREEMPT	1
-BURST	1
-SDSTROBE	1
-SDR0-1	2
-ADL	1
-CMD	1
-S0/-S1	2
M/-I/O	1
-BHE	1
TTL DIRECTION	1
CHRESET	1
-IRQA, -IRQB	2
-CDDS16 / -DS16RTN	2
-CDSFDBK/ -SFDBKRTN	2
CDCHRDY/ CHRDYRTN	2
-CHCK	1
-CDSETUP	1

4.2 ADAPTER SIDE PINS

	QTY
AD0-15	16
-LBHE	1
ALE	1
DREQ	4
-DACK	4
-IOR/-IOW/-MEMR/-MEMW	4
READY	1
-CS0-3	4
LOCALINT0	1
-INITROM	1
CLK	1
-CHCKIN	1
MULTI FUNCTION PINS	8
SIGNAL PINS TOTAL	127
SPARE PINS	1
GROUND PINS	24
VCC PINS	8
TOTAL PINS	160

4.3 Pinout List (by pin number)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	41	GND	81	GND	121	GND
2	GND	42	-LBHE	82	CHRDYRTN	122	GND
3	A20	43	READY	83	-SFDBKRTN	123	A14
4	A8	44	-CHCKIN	84	-SDR0	124	A2
5	ARB/-GNT	45	MFP0	85	-SDR1	125	ARB3
6	D0	46	MFP1	86	-DS16RTN	126	D12
7	DPAR0	47	MFP2	87	TTLDIR	127	D11
8	GND	48	MFP3	88	-S0	128	GND
9	A21	49	MFP4	89	-S1	129	A15
10	A9	50	MFP5	90	M/-IO	130	A3
11	DPAR1	51	GND	91	-ADL	131	ARB2
12	-DPAREN	52	MFP6	92	-CMD	132	D10
13	GND	53	MFP7	93	-SDSTROBE	133	D9
14	A22	54	GND	94	MADE24	134	GND
15	A10	55	CLK	95	GND	135	A16
16	GND	56	CHRESET	96	A31	136	A4
17	A23	57	AD0	97	A30	137	ARB1
18	A11	58	AD1	98	GND	138	NC
19	GND	59	AD2	99	A29	139	VCC
20	CDCHRDY	60	VCC	100	A28	140	D8
21	VCC	61	AD3	101	VCC	141	D7
22	-IOR	62	GND	102	A27	142	GND
23	-IOW	63	AD4	103	A26	143	A17
24	-MEMR	64	AD5	104	GND	144	A5
25	-MEMW	65	AD6	105	A25	145	ARB0
26	-INITROM	66	AD7	106	A24	146	D6
27	ALE	67	AD8	107	-IRQA	147	D5
28	-DACK0	68	AD9	108	-IRQB	148	GND
29	-DACK1	69	GND	109	GND	149	A18
30	-DACK2	70	AD10	110	A12	150	A6
31	-DACK3	71	AD11	111	A0	151	-BURST
32	DREQ0	72	AD12	112	-CHCK	152	D4
33	DREQ1	73	AD13	113	D15	153	D3
34	DREQ2	74	AD14	114	GND	154	GND
35	DREQ3	75	AD15	115	A13	155	A19
36	-CS0	76	LOCALINT0	116	A1	156	A7
37	-CS1	77	-CDSFDBK	117	-BHE	157	-PREEMPT
38	-CS2	78	-CDDS16	118	D14	158	D2
39	-CS3	79	-CDSETUP	119	D13	159	D1
40	VCC	80	VCC	120	VCC	160	VCC

4.4 Pinout List (by pin name)

Name	Pin	Name	Pin	Name	Pin	Name	Pin
-ADL	91	A14	123	AD8	67	GND	41
-BHE	117	A15	129	AD9	68	GND	51
-BURST	151	A16	135	ALE	27	GND	54
-CDDS16	78	A17	143	ARB/-GNT	5	GND	62
-CDSETUP	79	A18	149	ARB0	145	GND	69
-CDSFDBK	77	A19	155	ARB1	137	GND	81
-CHCK	112	A2	124	ARB2	131	GND	95
-CHCKIN	44	A20	3	ARB3	125	GND	98
-CMD	92	A21	9	CDCHRDY	20	GND	104
-CS0	36	A22	14	CHRDYRTN	82	GND	109
-CS1	37	A23	17	CHRESET	56	GND	114
-CS2	38	A24	106	CLK	55	GND	121
-CS3	39	A25	105	D0	6	GND	122
-DACK0	28	A26	103	D1	159	GND	128
-DACK1	29	A27	102	D10	132	GND	134
-DACK2	30	A28	100	D11	127	GND	142
-DACK3	31	A29	99	D12	126	GND	148
-DPAREN	12	A3	130	D13	119	GND	154
-DS16RTN	86	A30	97	D14	118	LOCALINT0	76
-INITROM	26	A31	96	D15	113	M/-IO	90
-IOR	22	A4	136	D2	158	MADE24	94
-IOW	23	A5	144	D3	153	MFP0	45
-IRQA	107	A6	150	D4	152	MFP1	46
-IRQB	108	A7	156	D5	147	MFP2	47
-LBHE	42	A8	4	D6	146	MFP3	48
-MEMR	24	A9	10	D7	141	MFP4	49
-MEMW	25	AD0	57	D8	140	MFP5	50
-PREEMPT	157	AD1	58	D9	133	MFP6	52
-S0	88	AD10	70	DPAR0	7	MFP7	53
-S1	89	AD11	71	DPAR1	11	NC	138
-SDR0	84	AD12	72	DREQ0	32	READY	43
-SDR1	85	AD13	73	DREQ1	33	TTLDIR	87
-SDSTROBE	93	AD14	74	DREQ2	34	VCC	21
-SFDBKRTN	83	AD15	75	DREQ3	35	VCC	40
A0	111	AD2	59	GND	1	VCC	60
A1	116	AD3	61	GND	2	VCC	80
A10	15	AD4	63	GND	8	VCC	101
A11	18	AD5	64	GND	13	VCC	120
A12	110	AD6	65	GND	16	VCC	139
A13	115	AD7	66	GND	19	VCC	160

5.0 PIN DESCRIPTIONS

The following section describes the function of the 82C614 signal pins. All signals that connect directly to the MicroChannel have the proper structure (open collector, totem pole, tri-state) and proper current drive as specified in the MicroChannel specification.

TP = Totem Pole
TS = TriState
OC = Open Collector

MicroChannel PINS

Signal	Type	Description
A0-31	I/O	**Address Lines 0-31.** These pins transfer the 32 bits of address to and from the MicroChannel. The 82C614 drives these lines when it is the master and receives these lines when it is a slave. These pins connect directly to the MicroChannel. 24mA TS.
MADE24	I/O	**Memory Address Enable 24.** The 82C614 drives this line when it is the master and receives this line when it is a slave. As a bus slave, when this line is high the 82C614 ignores the A24-31 inputs and assumes they are all low. As a bus master, the 82C614 drives MADE24 high for addresses below 16M (A24-31 low) and low for addresses of 16M and above (A24-31 non zero). 24mA TS.
D0-15	I/O	**Data Bits 0-15.** These lines are used to transfer the low order 16 bits of the MicroChannel data bus. These lines connect directly to the MicroChannel. 24mA TS.
DPAR0-1	I/O	**Data Parity Bits 0-1.** These signals represent the odd parity of the lower 16 data bits on the MicroChannel for both read and write cycles. The direction is the same as that of the data bits. These lines are connected directly to the MicroChannel. 24mA TS.
-DPAREN	I/O	**Data Parity Enable.** This signal is driven low to indicate that parity information on the bus is valid. The 82C614 drives this signal low during write cycles when a Master and Reads when a slave. During reads as a Master and Writes as a slave it uses this line to determine whether parity should be checked. The direction of the line is the same as that of the data. This line is connected directly to the MicroChannel. 24mA TS.

MicroChannel PINS (continued)

Signal	Type	Description
ARB0-3	I/O	Arbitration Level 0-3. These lines are used by devices arbitrating for control of the bus. The 82C614 drives and receives these lines when it requests the bus. These lines may be connected directly to the MicroChannel. 24mA OC.
ARB/-GNT	I	Arbitrate/Grant. When high, this line indicates that an arbitration cycle is in progress. When low, the winning device is granted the bus. This line may be connected directly to the MicroChannel.
-PREEMPT	I/O	Preempt. This line is driven low by devices requesting the bus. The 82C614 drives and monitors this line in accordance with the MicroChannel specification. The 82C614 will relinquish control of the bus within 7.8 microseconds after PREEMPT is driven low by another device. This line may be connected directly to the MicroChannel. 24mA OC.
-BURST	O	Burst. This line is driven low by the 82C614 when a burst transfer on the bus is required, which is pretty much anytime it becomes a bus master. This line may be connected directly to the MicroChannel. 24mA OC.
-SDSTROBE	O	Streaming Data Strobe. This line is driven low to indicate that data is valid during a streaming data transfer. The 82C614 drives this line when it is the master during streaming data write cycles. This line must be connected to the MicroChannel through a 24 ma buffer. A 2.5K pullup resistor should be connected to the output of the buffer. 4mA TS.
-SDR0-1	I	Streaming Data Request 0 and 1. These lines indicate the addressed device supports streaming data transfers and indicates the speed at which these transfers can occur. The 82C614 supports 100ns streaming data transfers when a master. The 82C614 is not a streaming data slave, and therefore does not drive these lines. These pins may be connected directly to the MicroChannel. 20K pullup resistors should be provided on the board to satisfy the MicroChannel specification.

MicroChannel PINS

Signal	Type	Description
-ADL	I/O	**Address Decode Latch.** This signal is used to latch the addresses and certain status lines on the MicroChannel in transparent latches. The 82C614 drives this line when it is the master and receives this line when it is a slave. This line must be connected to the MicroChannel through a 24 mA bi-directional buffer. 4mA TS.
-CMD	I/O	**Command.** This signal provides the command timing for MicroChannel cycles other than streaming data cycles. When the 82C614 is the master it drives this line. When it is a slave it receives this line. This line must be connected to the MicroChannel through a 24mA bi-directional buffer. 4mA TS.
-S0-1	I/O	**Status 0 and 1.** These signals carry the coded status (in conjunction with M/-I/O) of the type of cycle occurring on the MicroChannel. The falling edge of either is used to indicate that a cycle is starting. The 82C614 drives these lines when it is the master and receives them when it is a slave. These lines must be connected to the MicroChannel through a 24 mA bi-directional buffer. 4mA TS.
M/-IO	I/O	**Memory/I/O.** This signal indicates whether the current cycle is a memory or I/O cycle. When the 82C614 is the master it drives this line and receives it when it is a slave. This line must be connected to the MicroChannel through a 24mA bi-directional buffer. 4mA TS. M/IO -S0 -S1 Decoded Command 0 0 0 Reserved 0 0 1 I/O Write 0 1 0 I/O Read 0 1 1 Inactive 1 0 0 Reserved 1 0 1 Memory Write 1 1 0 Memory Read 1 1 1 Inactive
TTL	O	**TTL Direction.** This line is used to control the direction of the "245" type buffer that is used on the "strobe" signals identified above as requiring an external buffer to connect to the MicroChannel. This line is high to indicate that the 82C614 is the bus master and the buffered signals should be driving out onto the bus. This line is low at all other times. 4mA TP.

MicroChannel PINS (continued)

Signal	Type	Description
CHRESET	I	**Channel Reset.** This active high line indicates a bus reset. At reset the 82C614 will down-load its configuration registers from the INITROM and all other registers will return to the default state. This line may be connected directly to the MicroChannel.
-BHE	I/O	**Byte High Enable.** During 16 bit transfers this line is used to indicate whether or not the data on D8-15 is valid. If BHE is low and A0 is high, a byte transfer on D8-15 is occurring. If BHE and A0 are low then a 16 bit transfer is occurring. The 82C614 drives this line when it is the master and receives it when it is a slave. This line may be connected directly to the MicroChannel. 24mA TS.
-IRQA-B	O	**System Interrupt Request.** These lines are driven low to cause an interrupt on the MicroChannel. They can be activated by an end of process interrupt from any of the DMA controllers or from any of the local bus interrupt requests. If POS control of the interrupt level is desired, additional System interrupt lines are available through the multifunction pins. These lines can be connected directly to the MicroChannel. Note that since these lines are open collector, an external 4.7K ohm pull-up should be used if these lines are not connected directly to the MicroChannel. 24mA OC.
-CDDS16	O	**Card Data Size 16.** This pin is driven by the 82C614 as a slave to indicate that it is a 16 bit device. The 82C614 will drive it low for all register accesses. It will also drive it low for accesses to a local peripheral if that peripheral is configured for a data size of 16 bits. Each Programmable decode may be individually programmed for an 8 or 16 bit data size. The fixed decodes may be programmed as a block. If an external decode is used, the data size information from the external decoder is fed into one of the multifunction pins. The 82C614 passes it onto this line, and uses it internally for steering. The 82C614 does not assert this line during master operations. This line may be connected directly to the MicroChannel. 6mA TP.
-DS16RTN	I	**Card Data Size 16 Return.** This is the logical OR of all of the individual CDDS16 lines on the MicroChannel. As a master the 82C614 monitors this line to determine the data size of the addressed slave. This line may be connected directly to the MicroChannel.

MicroChannel PINS (continued)

Signal	Type	Description
-CDSFDBK	O	**Card Selected Feedback.** If the 82C614 is successfully addressed as a slave it will drive this line low to indicate that it has been selected. This line may be connected directly to the MicroChannel. 6mA TP.
-SFDBKRTN	I	**Card Selected Feedback Return.** This signal is the logical OR of all of the individual CDSFDBK lines on the MicroChannel. When it is a master, the 82C614 monitors this line to determine if the addressed slave actually exists or not. If the slave does not exist, the 82C614 can be programmed to indicate an error for that DMA channel, to assert CHCK, or to ignore the error (for diagnostic purposes).
CDCHRDY	O	**Card Channel Ready.** This signal is used by slave devices to extend the current MicroChannel cycle. When this signal is high, the device is "ready" and the cycle completes. The 82C614 drives this signal when it is a slave. 6mA TP.
CHRDYRTN	I	**Card Channel Ready Return.** This signal is the logical AND of all the individual CDCHRDY signals. The 82C614 receives this line when it is a master so that it may extend bus cycles for slaves that request it.
-CHCK	I/O	**Channel Check.** This signal is driven low by the 82C614 when a slave to indicate a write data parity error or error from a device on the local bus. The 82C614 also receives this pin, and checks it during each bus cycle when a bus master. 24mA OC.
-CDSETUP	I	**Card Setup.** This signal is driven low to indicate that access to the 82C614's POS registers is required. When CDSETUP is low, the 82C614 will only allow I/O accesses to the POS register space and will only decode address lines A0-2.

Adapter Logic Pins

Signal	Type	Description
AD0-15	I/O	Local Address/Data Bits 0-15. While the ALE signal is high (and for some hold time) this bus contains a local address. While a read command is active, this bus is an input, receiving data from the local peripheral or memory. While a write command is active, this bus contains write data. These signals function slightly differently during the INIT ROM loading. See the INIT ROM section for further details. 8mA TS.
-LBHE	O	Local Byte High Enable. Active for byte accesses to an odd location, or Word accesses. Note that to be compatible with a normal 286 type of interface, LBHE will be active for byte accesses to an odd location even if the device being accessed is 8 bit (the 82C614 knows in advance whether the device is 8 or 16 bit). Inactive during INIT ROM cycles (they are always even addresses). Does not need to be latched externally. 8mA TS.
ALE	O	Local Address Latch Enable. This signal is used to latch the local address from the 82C614 LAD0-15 lines. It is active high, so that 373 type transparent latches may be used. 4mA TP.
DREQ0-3	I	DMA Request 0-3. These lines are used by peripheral devices to request a DMA transfer. The direction of the transfer is determined by the programming of the DMA channel. Configuration registers individually program these pins to be either edge triggered or level triggered. They may be programmed to be active high or low as a block. The priority of these lines can be set to fixed or rotating.
DACK0-3	O	DMA Acknowledge 0-3. When an internal DMA controller is performing a local bus cycle, it's associated DMA acknowledge is active. It is activated slightly after the address lines and chip selects, to ensure that it toggles between consecutive bus cycles. The polarity of these signals is programmable as a group. 4mA TP.
-IOR, -MEMR	I/O	I/O and Memory Read Strobes. These lines provide the timing for I/O and Memory reads. 8mA TS (-IOR), 4mA TS (-MEMR).
-IOW, -MEMW	I/O	I/O and Memory Write Strobes. These lines provide the timing for I/O and memory write cycles. 8mA TS (-IOW), 4mA TS (-MEMW).

Adapter Logic Pins (continued)

Signal	Type	Description
READY	I	**Local Bus Ready.** When the 82C614 is accessing a local device, this pin is used by the device to add wait states. The 82C614 will only sample this pin after the internally programmed wait states for that decode have been exhausted.
-CS0-3	O	**Programmable Decodes 0-3.** These four lines may be programmed to provide a variety of MicroChannel slave decoding functions eliminating the need for address decoding logic on the board. Each output can be programmed to respond to an I/O or memory area, and may be relocated by the POS bits. 4mA TP.
LOCALINT0	I	**Local Interrupt 0.** This input is used by the peripheral devices to get service from the system. Pulling this input low causes a MicroChannel Interrupt, if enabled. This line should be held low until the interrupt is serviced. Three more Local Interrupt lines are provided by the multifunction pins.
-INITROM	I/O	**Initialization ROM Enable.** Shortly after CHRESET goes inactive the INIT ROM is downloaded into the 82C614. This pin is a chip select for that ROM. It is an input just after RESET to determine the INIT ROM loading protocol. See the INIT ROM section for further details. 4mA TS.
CLK	I	**Clock Input.** This input is the master clock that drives the MicroChannel state machine and all timing for the 82C614. It should be connected to a 40MHz TTL level clock.
-CHCKIN	I	**Channel Check Input.** This input is used by the adapter logic to signal a serious error condition. If it is active during an access from the MicroChannel, the 82C614 will activate -CHCK on the MicroChannel if enabled. If it is low during a bus cycle initiated by one of the 82C614 DMA controllers, it will set the CHCKIN bit of DMA controllers Secondary Status register and optionally halt the DMA controller.
MFP0-7	I/O	**Multi-Function Pins 0-7.** These eight lines can be programmed to a variety of functions to "customize" the interface to the adapter logic and peripheral chips. They can be programmed to provide such functions as an AEN function, Terminal count, more local address lines, local CPU interface support, etc. 4mA TS.

6.0 Operating Considerations

6.1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	-	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{OP}	-25°	85°	C
Storage Temperature	T_{STG}	-40°	125°	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

6.2 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0°	70°	C

6.3 DC Characteristics (T_A = 0°C to 70°C; V_{CC} = 5V +/- 5%)

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}	-	0.8	V
Input High Voltage	V_{IH}	2.0	-	V
Output Low Voltage	V_{OL}	-	0.45	V
Output High Voltage	V_{OH}	2.4	-	V
Input Low Current ($0 < V_{IN} < V_{CC}$)	I_{IL}	-	±10	uA
Power Supply Current @ 40MHz	I_{CC}			mA
Output High-Z Leakage Current ($0 < V_{IN} < V_{CC}$)	I_{OZL}	-	±10	uA
Static Power Supply Current	I_{CCSB}			mA

I_{OH} and I_{OL} - Output drive capability (for both V_{OH} and V_{OL})

$I_{OL}=I_{OH}$=4mA: -ADL, -CMD, -CS0-3, -INITROM, -MEMR, -MEMW, -S0-1, -SDSTROBE, ALE, DACK0-3, M/-IO, MFP0-7, TTLDIR.

$I_{OL}=I_{OH}$=6mA: -CDDS16, -CDSFDBK, CDCHRDY.

$I_{OL}=I_{OH}$=8mA: -LBHE, -IOR, -IOW, AD0-15.

$I_{OL}=I_{OH}$=24mA: -BHE, -BURST, -CHCK, -DPAREN, -IRQA, -IRQB, -PREEMPT, A0-31, ARB0-3, D0-15, DPAR0-1, MADE24.

7.0 AC CHARACTERISTICS

7.1 Local Bus Cycles (Normal Cycles)

READ/WRITE CYCLES		Min	Max	Units
t100	ALE pulse width	40	-	nS
t101	AD(15:0) set-up to ALE inactive	30	-	nS
t102	AD(15:0) hold from ALE inactive	15	-	nS
t103	-CSn, -BHE set-up to ALE inactive	30	-	nS
t104	-CSn, -BHE set-up to COMMAND active	80	-	nS
t105	COMMAND active delay from ALE inactive	40	-	nS
t106	Read data valid from COMMAND active	-	110	nS
t107	Read data invalid from COMMAND inactive	0	40	nS
t108	COMMAND pulse width	140		nS
t109	-CSn, -BHE hold from COMMAND inactive	40	-	nS
t110	-DACKn set-up to COMMAND active	40	-	nS
t111	-DACKn hold from COMMAND inactive	40	-	nS
t112	ALE active from COMMAND inactive	40	-	nS
t113	Write data set-up to COMMAND active	15	-	nS
t115	Write data hold from COMMAND inactive	40	-	nS

Note: Add 100nS per wait state to t106 timing.

READY TIMING		Min	Max	Units
t130	READY inactive from COMMAND active	-	90	nS
t131	COMMAND inactive from READY active	25	-	nS
t132	Read data valid from READY active	-	10	nS

Local Bus Cycles (Normal Cycles) continued

DREQ TIMING		Min	Max	Units
t140	-DACKn active from DREQn active (all modes)	50	-	nS
t141	DREQn inactive from -DACKn active (modes 1 and 2)	0	-	nS
t142	COMMAND inactive from DREQn inactive (mode 2)	50	-	nS
t143	DREQn inactive from -DACKn inactive (mode 3)	-	90	nS
t144	-TC active from COMMAND active	-	60	nS
t145	-TC inactive from COMMAND inactive	15	-	nS

7.2 Local Bus Cycles (Compressed Cycles)

READ/WRITE CYCLES		Min	Max	Units
t100	ALE pulse width	20	-	nS
t101	AD(15:0) set-up to ALE inactive	15	-	nS
t102	AD(15:0) hold from ALE inactive	15	-	nS
t103	-CSn, -BHE set-up to ALE inactive	15	-	nS
t104	-CSn, -BHE set-up to COMMAND active	60	-	nS
t105	COMMAND active delay from ALE inactive	40	-	nS
t106	Read data valid from COMMAND active	-	60	nS
t107	Read data invalid from COMMAND inactive	0	15	nS
t108	COMMAND pulse width	90		nS
t109	-CSn, -BHE hold from COMMAND inactive	15	-	nS
t110	-DACKn set-up to COMMAND active	40	-	nS
t111	-DACKn hold from COMMAND inactive	15	-	nS
t112	ALE active from COMMAND inactive	15	-	nS
t114	Write data valid from COMMAND active	20	-	nS
t115	Write data hold from COMMAND inactive	15	-	nS

Note: Add 100nS per wait state to t106 timing.

READY TIMING		Min	Max	Units
t130	READY inactive from COMMAND active	-	40	nS
t131	COMMAND inactive from READY active	25	-	nS
t132	Read data valid from READY active	-	10	nS

Local Bus Cycles (Compressed Cycles) continued

DREQ TIMING		Min	Max	Units
t140	-DACKn active from DREQn active (all modes)	50	-	nS
t141	DREQn inactive from -DACKn active (modes 1 and 2)	0	-	nS
t142	COMMAND inactive from DREQn inactive (mode 2)	50	-	nS
t143	DREQn inactive from -DACKn inactive (mode 3)	-	115	nS
t144	-TC active from COMMAND active	-	60	nS
t145	-TC inactive from COMMAND inactive	15	-	nS

7.3 MicroChannel Bus Cycles (Slave Cycles)

BASIC TRANSFER DEFAULT CYCLES (200 ns Minimum)		Min	Max	Units
t201	Status active from Address, M/-IO, -REFRESH and MADE24 valid	10	-	nS
t202	-CMD active from status active	55	-	nS
t202A	Status pulse width of an aborted cycle	85	-	nS
t203	-ADL active from Address, M/-IO, -REFRESH and MADE24 valid	45	-	nS
t204	-ADL active to -CMD active	40	-	nS
t205	-ADL active from status active	12	-	nS
t206	-ADL pulse width	40	-	nS
t207	Status hold from -ADL inactive	25	-	nS
t208	Address, M/-IO, -REFRESH, -BHE and MADE24 hold from -ADL inactive	25	-	nS
t209	Address, M/-IO, -REFRESH, -BHE and MADE24 hold from -CMD active	30	-	nS
t210	Status hold from -CMD active	30	-	nS
t211	-BHE setup to -ADL inactive	40	-	nS
t212	-BHE setup to -CMD active	40	-	nS
t213	-CDDS16 active from Address Bus and M/-IO valid	-	55	nS
t213R	-DS16RTN active from Address Bus and M/-IO valid	-	75	nS
t214	-CDSFDBK active from Address Bus and M/-IO valid	-	60	nS
t214R	-SFDBKRTN active from Address Bus and M/-IO valid	-	80	nS
t215	-CMD active from Address valid	85	-	nS
t216	-CMD pulse width	90	-	nS

MicroChannel Bus Cycles (Slave Cycles) continued

BASIC TRANSFER DEFAULT CYCLES (200 ns Minimum)		Min	Max	Units
t217	Write Data setup to -CMD active	0	-	nS
t218	Write Data hold from -CMD inactive	30	-	nS
t219	Status active to Read Data valid (access time) (valid only when t202 less than 65nS)	-	125	nS
t220	Read Data valid from -CMD active	-	60	nS
t221	Read Data hold from -CMD inactive	0	-	nS
t222	Read Data Bus tri-state from -CMD inactive	-	40	nS
t223	-CMD active to next -CMD active	190	-	nS
t223A	-CMD inactive to next -CMD active	80	-	nS
t223B	-CMD inactive to next -ADL active	40	-	nS
t224	Next status active from status inactive	30	-	nS
t225	Next status active to -CMD inactive	-	20	nS

BASIC TRANSFER SYNCHRONOUS-EXTENDED CYCLES (300 ns Minimum)		Min	Max	Units
t216A	-CMD pulse width	190	-	nS
t226	CDCHRDY inactive from Address Bus valid	-	60	nS
t226R	CHRDYRTN inactive from Address Bus valid	-	80	nS
t227	CDCHRDY inactive from status valid and previous -CMD inactive (valid only when t201 greater than 30nS)	0	30	nS
t227R	CHRDYRTN inactive from status valid and previous -CMD inactive (valid only when t201 greater than 30nS)	0	50	nS
t228	CDCHRDY active from -CMD active	0	30	nS
t228R	CHRDYRTN active from -CMD active	0	50	nS
t228D	Read Data valid from -CMD active (used with t228)	0	160	nS
t235	CDCHRDY active from CDCHRDY inactive	0	3.5	uS

MicroChannel Bus Cycles (Slave Cycles) continued

BASIC TRANSFER ASYNCHRONOUS-EXTENDED CYCLES (> 300 ns Minimum)		Min	Max	Units
t216A	-CMD pulse width	190	-	nS
t226	CDCHRDY inactive from Address Bus valid	-	60	nS
t226R	CHRDYRTN inactive from Address Bus valid	-	80	nS
t227	CDCHRDY inactive form status valid and previous -CMD inactive (valid only when t201 greater than 30nS)	0	30	nS
t227R	CHRDYRTN inactive from status valid and previous -CMD inactive (valid only when t201 greater than 30nS)	0	50	nS
t229S	Read Data from slave valid from CDCHRDY active	-	60	nS
t229M	Read Data valid to master from CHRDYRTN active	-	60	nS
t229A	-CMD inactive from CHRDYRTN active	60	-	nS
t235	CDCHRDY active from CDCHRDY inactive	0	3.5	uS

MicroChannel Bus Cycles (Slave Cycles) continued

BASIC TRANSFER ARBITRATION CYCLES (DMA SLAVE)		Min	Max	Units
t240	-PREEMPT active to EOT (channel release)	0	7.8	uS
t241	ARB/-GNT in the ARB state from EOT (channel release)	30	-	nS
t242	-PREEMPT inactive from ARB/-GNT in the -GNT state	0	50	nS
t242A	-PREEMPT inactive to status inactive	20	-	nS
t242B	-PREEMPT active from status inactive (compete for the channel after the inactive state)	10	-	nS
t243	-BURST active from ARB/-GNT in the -GNT state	-	50	nS
t244	ARB/-GNT in ARB state	100	-	nS
t245	Driver turn-on delay from ARB/-GNT in ARB state	0	50	nS
t245A	Driver turn-on delay from lower priority line	0	50	nS
t246	Driver turn-off delay from ARB/-GNT in ARB state	0	50	nS
t247	Driver turn-off delay from higher priority line	0	50	nS
t248	Arbitration bus stable before ARB/-GNT in -GNT state	10	-	nS
t249	Tri-state drivers from ARB/-GNT in ARB state	-	50	nS

BASIC TRANSFER FIRST CYCLE AFTER GRANT (DMA SLAVE)		Min	Max	Units
t202A	Status pulse width of an aborted cycle	85	-	nS
t243A	Address Bus valid from ARB/-GNT in the -GNT state	0	-	nS
t243B	-CMD active from ARB/-GNT in the -GNT state	115	-	nS
t243C	DMA controller delay	30	-	nS
t243D	Status inactive from ARB/-GNT in the -GNT state	145	-	nS

MicroChannel Bus Cycles (Slave Cycles) continued

DIRECT MEMORY ACCESS SINGLE DMA TRANSFER (DMA-Controller Controlled)		Min	Max	Units
t250	-BURST activated by the DMA controller from the first -CMD active	-	30	nS
t251	-BURST released by the DMA controller from the last status active	-	40	nS
t252	-TC setup to -CMD inactive (slower than 200nS cycles)	30	-	nS
t252D	-TC setup to -CMD inactive (200nS cycles only)	15	-	nS
t253	-TC hold from -CMD inactive	10	-	nS

DIRECT MEMORY ACCESS BURST DMA TRANSFER (DMA-Controller Terminated)		Min	Max	Units
t252	-TC setup to -CMD inactive (slower than 200nS cycles)	30	-	nS
t252D	-TC setup to -CMD inactive (200nS cycles only)	15	-	nS
t253	-TC hold from -CMD inactive	10	-	nS
t254	-BURST released by the DMA slave from -TC active	-	30	nS

DIRECT MEMORY ACCESS BURST DMA TRANSFER (DMA-Slave Terminated) (Default Cycle, 200 ns)		Min	Max	Units
t255	-BURST released by the DMA slave from the last I/O cycle status active (default cycle only)	-	40	nS
t255A	-BURST released by the DMA slave from I/O address valid for the last I/O cycle (default cycle only)	-	70	nS
t256	-BURST inactive to -CMD inactive	35	-	nS
t258	-BURST redrive from -CMD active	-	30	nS

MicroChannel Bus Cycles (Slave Cycles) continued

DIRECT MEMORY ACCESS BURST DMA TRANSFER (DMA-Slave Terminated) (Synchronous-Extended Cycle, 300 ns)		Min	Max	Units
t255E	-BURST released by the DMA slave from the last I/O -CMD active (extended cycles only)	-	80	nS
t256	-BURST inactive to -CMD inactive	35	-	nS

DIRECT MEMORY ACCESS BURST DMA TRANSFER (DMA-Slave Terminated) (Asynchronous-Extended Cycle, > 300 ns)		Min	Max	Units
t255X	-BURST released by the DMA slave before CDCHRDY active (asynchronous-extended cycles only)	50	-	nS
t256	-BURST inactive to -CMD inactive	35	-	nS

SYSTEM CONFIGURATION CYCLES		Min	Max	Units
t216A	-CMD pulse width	190	-	nS
t228D	Read Data valid from -CMD active	-	160	nS
t229S	Read Data from slave valid from CDCHRDY active	-	60	nS
t229M	Read data valid to master from CHRDYRTN active	-	60	nS
t260	CHRESET active pulse width	100	-	nS
t261	-CDSETUP active to -ADL active	15	-	nS
t262	-CDSETUP hold from -ADL inactive	25	-	nS
t263	-CDSETUP hold from -CMD active	30	-	nS
t264	-CDDS16 active from -CDSETUP active	-	25	nS
t265	CDCHRDY inactive from -CDSETUP active and status active	-	45	nS
t265A	CHRDYRTN inactive from -CDSETUP active and status active	-	25	nS
t266	Adapter ID valid from trailing edge of CHRESET	-	1	S
t266A	Adapter ID access from trailing edge of CHRESET	1	-	mS

MicroChannel Bus Cycles (Slave Cycles) continued

DATA PARITY CHECKING (READ) CYCLES		Min	Max	Units
t290	-DPAREN active from -CMD active (default cycle)	0	60	nS
t290	-DPAREN active from -CMD active (sync-extended cycle)	0	160	nS
t290	-DPAREN active from -CMD active (async-extended cycle)	0	-	nS
t290A	-DPAREN active to CDCHRDY active (async-extended cycle)	-	0	nS
t291	-DPAREN inactive from -CMD inactive	0	40	nS
t292	-DPAREN tri-stated from -CMD inactive	0	80	nS
t293	-DPAREN tri-stated from -DPAREN active	20	-	nS

CHANNEL-CHECK TIMING (DEFAULT CYCLES)		Min	Max	Units
t300	-CHCK active from -CMD active	0	50	nS
t300A	-CHCK pulse width	50	-	nS
t300P	-CHCK active from -CMD and -DPAREN active	0	50	nS
t301	-CHCK disabled from -CMD inactive	0	40	nS

CHANNEL-CHECK TIMING (EXTENDED CYCLES)		Min	Max	Units
t299	-CHCK active from -CMD active (async-extended and streaming data cycles)	0	-	nS
t299S	-CHCK active from -CMD active (sync-extended cycle)	0	150	nS
t302	-CHCK active from CDCHRDY active (async-extended and streaming data cycles)	-	50	nS

7.4 MicroChannel Bus Cycles (Master Cycles)

BASIC TRANSFER DEFAULT CYCLES (200 ns Minimum)		Min	Max	Units
t501	Status active from Address, M/-IO, -REFRESH and MADE24 valid	10	-	nS
t502	-CMD active from status active	55	-	nS
t502A	Status pulse width of an aborted cycle	85	-	nS
t503	-ADL active from Address, M/-IO, -REFRESH and MADE24 valid	45	-	nS
t504	-ADL active to -CMD active	40	-	nS
t505	-ADL active from status active	12	-	nS
t506	-ADL pulse width	40	-	nS
t507	Status hold from -ADL inactive	25	-	nS
t508	Address, M/-IO, -REFRESH, -BHE and MADE24 hold from -ADL inactive	25	-	nS
t509	Address, M/-IO, -REFRESH, -BHE and MADE24 hold from -CMD active	30	-	nS
t510	Status hold from -CMD active	30	-	nS
t511	-BHE setup to -ADL inactive	40	-	nS
t512	-BHE setup to -CMD active	40	-	nS
t513	-CDDS16 active from Address Bus and M/-IO valid	-	55	nS
t513R	-DS16RTN active from Address Bus and M/-IO valid	-	75	nS
t514	-CDSFDBK active from Address Bus and M/-IO valid	-	60	nS
t514R	-SFDBKRTN active from Address Bus and M/-IO valid	-	80	nS
t515	-CMD active from Address valid	85	-	nS
t516	-CMD pulse width	90	-	nS

MicroChannel Bus Cycles (Master Cycles) continued

BASIC TRANSFER DEFAULT CYCLES (200 ns Minimum)		Min	Max	Units
t517	Write Data setup to -CMD active	0	-	nS
t518	Write Data hold from -CMD inactive	30	-	nS
t519	Status active to Read Data valid (access time) (valid only when t202 less than 65nS)	-	125	nS
t520	Read Data valid from -CMD active	-	60	nS
t521	Read Data hold from -CMD inactive	0	-	nS
t522	Read Data Bus tri-state from -CMD inactive	-	40	nS
t523	-CMD active to next -CMD active	190	-	nS
t523A	-CMD inactive to next -CMD active	80	-	nS
t523B	-CMD inactive to next -ADL active	40	-	nS
t524	Next status active from status inactive	30	-	nS
t525	Next status active to -CMD inactive	-	20	nS

BASIC TRANSFER SYNCHRONOUS-EXTENDED CYCLES (300 ns Minimum)		Min	Max	Units
t516A	-CMD pulse width	190	-	nS
t526	CDCHRDY inactive from Address Bus valid	-	60	nS
t526R	CHRDYRTN inactive from Address Bus valid	-	80	nS
t527	CDCHRDY inactive from status valid and previous -CMD inactive (valid only when t201 greater than 30nS)	0	30	nS
t527R	CHRDYRTN inactive from status valid and previous -CMD inactive (valid only when t201 greater than 30nS)	0	50	nS
t528	CDCHRDY active from -CMD active	0	30	nS
t528R	CHRDYRTN active from -CMD active	0	50	nS
t528D	Read Data valid from -CMD active (used with t228)	0	160	nS
t535	CDCHRDY active from CDCHRDY inactive	0	3.5	uS

MicroChannel Bus Cycles (Master Cycles) continued

BASIC TRANSFER ASYNCHRONOUS-EXTENDED CYCLES (> 300 ns Minimum)		Min	Max	Units
t516A	-CMD pulse width	190	-	nS
t526	CDCHRDY inactive from Address Bus valid	-	60	nS
t526R	CHRDYRTN inactive from Address Bus valid	-	80	nS
t527	CDCHRDY inactive form status valid and previous -CMD inactive (valid only when t201 greater than 30nS)	0	30	nS
t527R	CHRDYRTN inactive from status valid and previous -CMD inactive (valid only when t201 greater than 30nS)	0	50	nS
t529S	Read Data from slave valid from CDCHRDY active	-	60	nS
t529M	Read Data valid to master from CHRDYRTN active	-	60	nS
t529A	-CMD inactive from CHRDYRTN active	60	-	nS
t535	CDCHRDY active from CDCHRDY inactive	0	3.5	uS

MicroChannel Bus Cycles (Master Cycles) continued

BASIC TRANSFER ARBITRATION CYCLES (DMA SLAVE)		Min	Max	Units
t540	-PREEMPT active to EOT (channel release)	0	7.8	uS
t541	ARB/-GNT in the ARB state from EOT (channel release)	30	-	nS
t542	-PREEMPT inactive from ARB/-GNT in the -GNT state	0	50	nS
t542A	-PREEMPT inactive to status inactive	20	-	nS
t542B	-PREEMPT active from status inactive (compete for the channel after the inactive state)	10	-	nS
t543	-BURST active from ARB/-GNT in the -GNT state	-	50	nS
t544	ARB/-GNT in ARB state	100	-	nS
t545	Driver turn-on delay from ARB/-GNT in ARB state	0	50	nS
t545A	Driver turn-on delay from lower priority line	0	50	nS
t546	Driver turn-off delay from ARB/-GNT in ARB state	0	50	nS
t547	Driver turn-off delay from higher priority line	0	50	nS
t548	Arbitration bus stable before ARB/-GNT in -GNT state	10	-	nS
t549	Tri-state drivers from ARB/-GNT in ARB state	-	50	nS

BASIC TRANSFER FIRST CYCLE AFTER GRANT (DMA SLAVE)		Min	Max	Units
t502A	Status pulse width of an aborted cycle	85	-	nS
t543A	Address Bus valid from ARB/-GNT in the -GNT state	0	-	nS
t543B	-CMD active from ARB/-GNT in the -GNT state	115	-	nS
t543C	DMA controller delay	30	-	nS
t543D	Status inactive from ARB/-GNT in the -GNT state	145	-	nS

MicroChannel Bus Cycles (Master Cycles) continued

DIRECT MEMORY ACCESS SINGLE DMA TRANSFER (DMA-Controller Controlled)		Min	Max	Units
t550	-BURST activated by the DMA controller from the first -CMD active	-	30	nS
t551	-BURST released by the DMA controller from the last status active	-	40	nS
t552	-TC setup to -CMD inactive (slower than 200nS cycles)	30	-	nS
t552D	-TC setup to -CMD inactive (200nS cycles only)	15	-	nS
t553	-TC hold from -CMD inactive	10	-	nS

DIRECT MEMORY ACCESS BURST DMA TRANSFER (DMA-Controller Terminated)		Min	Max	Units
t552	-TC setup to -CMD inactive (slower than 200nS cycles)	30	-	nS
t552D	-TC setup to -CMD inactive (200nS cycles only)	15	-	nS
t553	-TC hold from -CMD inactive	10	-	nS
t554	-BURST released by the DMA slave from -TC active	-	30	nS

DIRECT MEMORY ACCESS BURST DMA TRANSFER (DMA-Slave Terminated) (Default Cycle, 200 ns)		Min	Max	Units
t555	-BURST released by the DMA slave from the last I/O cycle status active (default cycle only)	-	40	nS
t555A	-BURST released by the DMA slave from I/O address valid for the last I/O cycle (default cycle only)	-	70	nS
t556	-BURST inactive to -CMD inactive	35	-	nS
t558	-BURST redrive from -CMD active	-	30	nS

MicroChannel Bus Cycles (Master Cycles) continued

DIRECT MEMORY ACCESS BURST DMA TRANSFER (DMA-Slave Terminated) (Synchronous-Extended Cycle, 300 ns)		Min	Max	Units
t555E	-BURST released by the DMA slave from the last I/O -CMD active (extended cycles only)	-	80	nS
t556	-BURST inactive to -CMD inactive	35	-	nS

DIRECT MEMORY ACCESS BURST DMA TRANSFER (DMA-Slave Terminated) (Asynchronous-Extended Cycle, > 300 ns)		Min	Max	Units
t555X	-BURST released by the DMA slave before CDCHRDY active (asynchronous-extended cycles only)	50	-	nS
t556	-BURST inactive to -CMD inactive	35	-	nS

SYSTEM CONFIGURATION CYCLES		Min	Max	Units
t516A	-CMD pulse width	190	-	nS
t528D	Read Data valid from -CMD active	-	160	nS
t529S	Read Data from slave valid from CDCHRDY active	-	60	nS
t529M	Read data valid to master from CHRDYRTN active	-	60	nS
t560	CHRESET active pulse width	100	-	nS
t561	-CDSETUP active to -ADL active	15	-	nS
t562	-CDSETUP hold from -ADL inactive	25	-	nS
t563	-CDSETUP hold from -CMD active	30	-	nS
t564	-CDDS16 active from -CDSETUP active	-	25	nS
t565	CDCHRDY inactive from -CDSETUP active and status active	-	45	nS
t565A	CHRDYRTN inactive from -CDSETUP active and status active	-	25	nS
t566	Adapter ID valid from trailing edge of CHRESET	-	1	S
t566A	Adapter ID access from trailing edge of CHRESET	1	-	mS

MicroChannel Bus Cycles (Master Cycles) continued

STREAMING DATA TRANSFERS		Min	Max	Units
t522	Data bus tri-state from -CMD inactive	0	40	nS
t570	-SDR(0,1) and -MSDR valid from -ADL active (slave only)	0	40	nS
t570A	-SDR(0,1) and -MSDR valid from -ADL active (masters only, for deferred cycle use)	0	115	nS
t571	-SDR(0,1) and -MSDR inactive from last -SDSTROBE fall (slave terminated cycle)	0	40	nS
t571A	-S0, -S1 inactive from last -SDSTROBE fall (master terminated cycle)	-	10	nS
t571B	-SDR(0,1) and -MSDR inactive from -S0, -S1 inactive (master terminated, slave ready)	0	40	nS
t572	-SDR(0,1) and -MSDR tri-state from -CMD inactive (master-terminated cycle)	0	40	nS
t573	-SDSTROBE active to -CMD active	-	10	nS
t573A	-SDSTROBE active from CHRDYRTN active	0	-	nS
t574	-SDSTROBE period	100	-	nS
t574A	-CMD inactive from last -SDSTROBE fall	100	-	nS
t579	Status inactive from -CMD active (master-terminated cycle)	-	7.8	uS
t580	-TC active from last -SDSTROBE fall	-	60	nS
t581	-TC hold from -CMD inactive	10	-	nS
t582A	A(0-31) tri-stated from CDCHRDY active	0	-	nS

MicroChannel Bus Cycles (M er Cycles) continued

STREAMING DATA TRANSFERS		Min	Max	Units
t574	-SDSTROBE period	100	-	nS
t574A	-CMD inactive from last -SDSTROBE fall	100	-	nS
t575	-SDSTROBE active	35	-	nS
t575A	-SDSTROBE inactive	35	-	nS
t575B	-SDSTROBE inactive to -CMD inactive	35	-	nS
t576	Send Data valid from -SDSTROBE fall	-	60	nS
t576A	CDCHRDY valid from -SDSTROBE fall	3	25	nS
t576B	CHRDYRTN valid from -SDSTROBE fall	3	45	nS
t577	Send Data and CDCHRDY hold from -SDSTROBE fall	10	-	nS
t577A	Write Data hold from -CMD inactive	11	-	nS
t577B	Read data hold from -CMD inactive	7	-	nS
t578	Receive Data valid before -SDSTROBE fall	25	-	nS
t578A	Receive Data valid before -CMD inactive	25	-	nS

MicroChannel Bus Cycles (Master Cycles) continued

DATA PARITY CHECKING (READ) CYCLES		Min	Max	Units
t590	-DPAREN active from -CMD active (default cycle)	0	60	nS
t590	-DPAREN active from -CMD active (sync-extended cycle)	0	160	nS
t590	-DPAREN active from -CMD active (async-extended cycle)	0	-	nS
t590A	-DPAREN active to CDCHRDY active (async-extended cycle)	-	0	nS
t591	-DPAREN inactive from -CMD inactive	0	40	nS
t592	-DPAREN tri-stated from -CMD inactive	0	80	nS
t593	-DPAREN tri-stated from -DPAREN active	20	-	nS

DATA PARITY CHECKING (WRITE) CYCLES		Min	Max	Units
t594	-DPAREN active from -CMD active	-	20	nS
t595	-DPAREN active from -ADL active	40	-	nS
t596	-CMD active from write data setup	15	-	nS
t606	-DPAREN inactive from -CMD inactive	20	-	nS

DATA PARITY CHECKING (WRITE) CYCLES		Min	Max	Units
t597	-DPAREN hold from -CMD inactive	40	-	nS
t598	-BURST inactive from -DPAREN inactive	0	-	nS

MicroChannel Bus Cycles (Master Cycles) continued

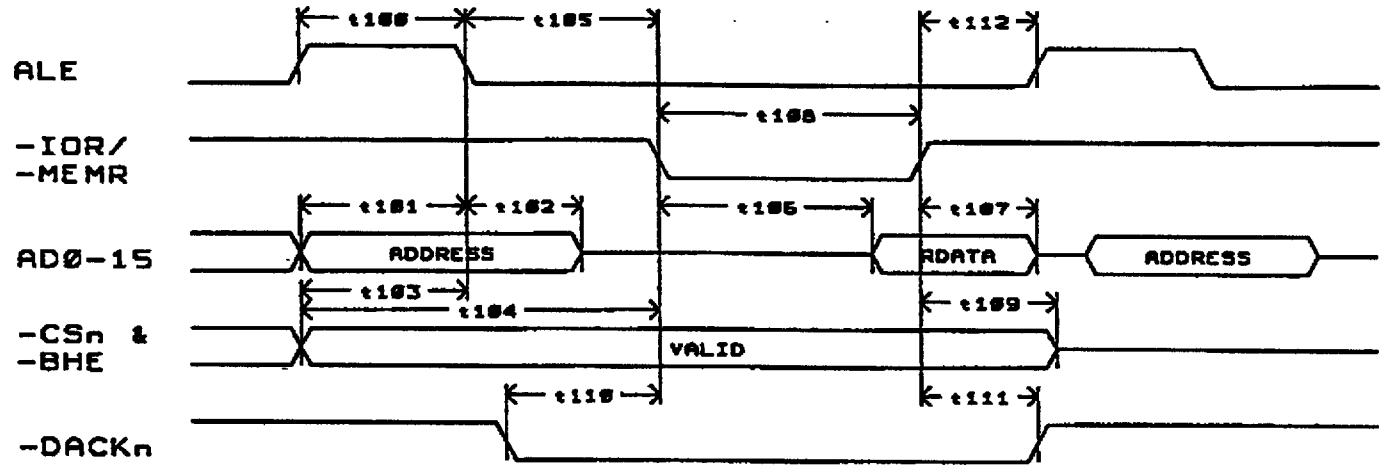
CHANNEL-CHECK TIMING (DEFAULT CYCLES)		Min	Max	Units
t600	-CHCK active from -CMD active	0	50	nS
t600A	-CHCK pulse width	50	-	nS
t600P	-CHCK active from -CMD and -DPAREN active	0	50	nS
t601	-CHCK disabled from -CMD inactive	0	40	nS

CHANNEL-CHECK TIMING (EXTENDED CYCLES)		Min	Max	Units
t599	-CHCK active from -CMD active (async-extended and streaming data cycles)	0	-	nS
t599S	-CHCK active from -CMD active (sync-extended cycle)	0	150	nS
t602	-CHCK active from CDCHRDY active (async-extended and streaming data cycles)	-	50	nS

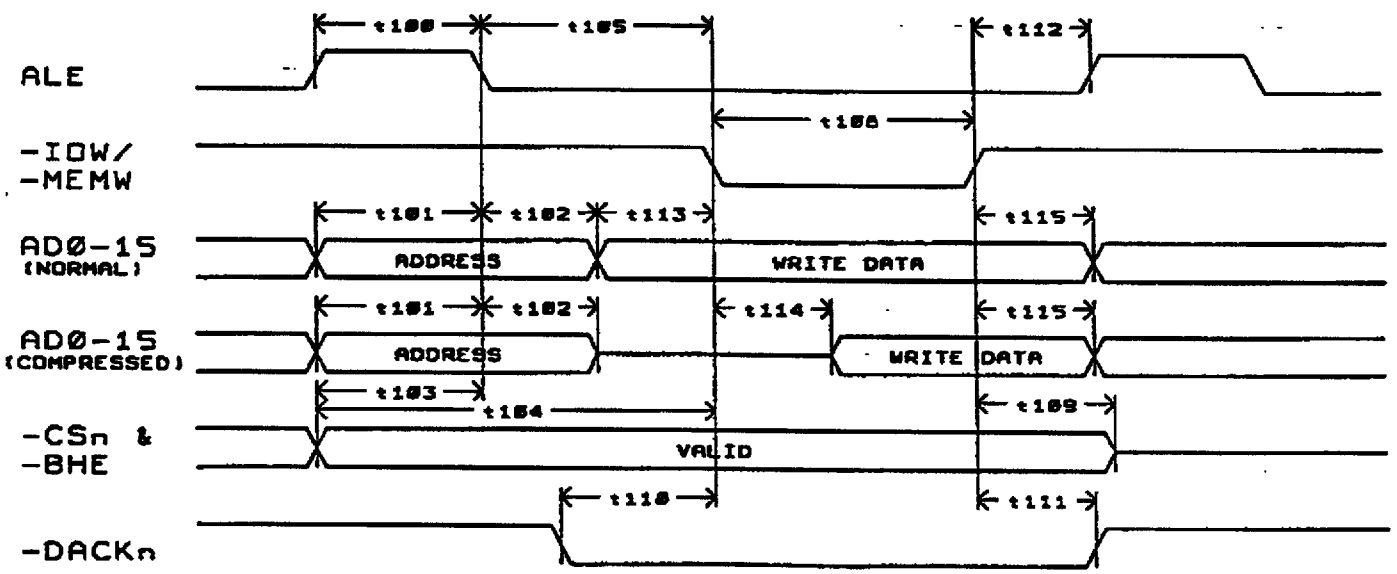
CHANNEL-CHECK TIMING (STREAMING DATA READ)		Min	Max	Units
t603	-CHCK active from last -SDSTROBE active	-	50	nS

CHANNEL-CHECK TIMING (STREAMING DATA WRITE)		Min	Max	Units
t604	-CHCK active from -CMD inactive	-	40	nS
t605	-CHCK disabled from -DPAREN inactive	0	40	nS

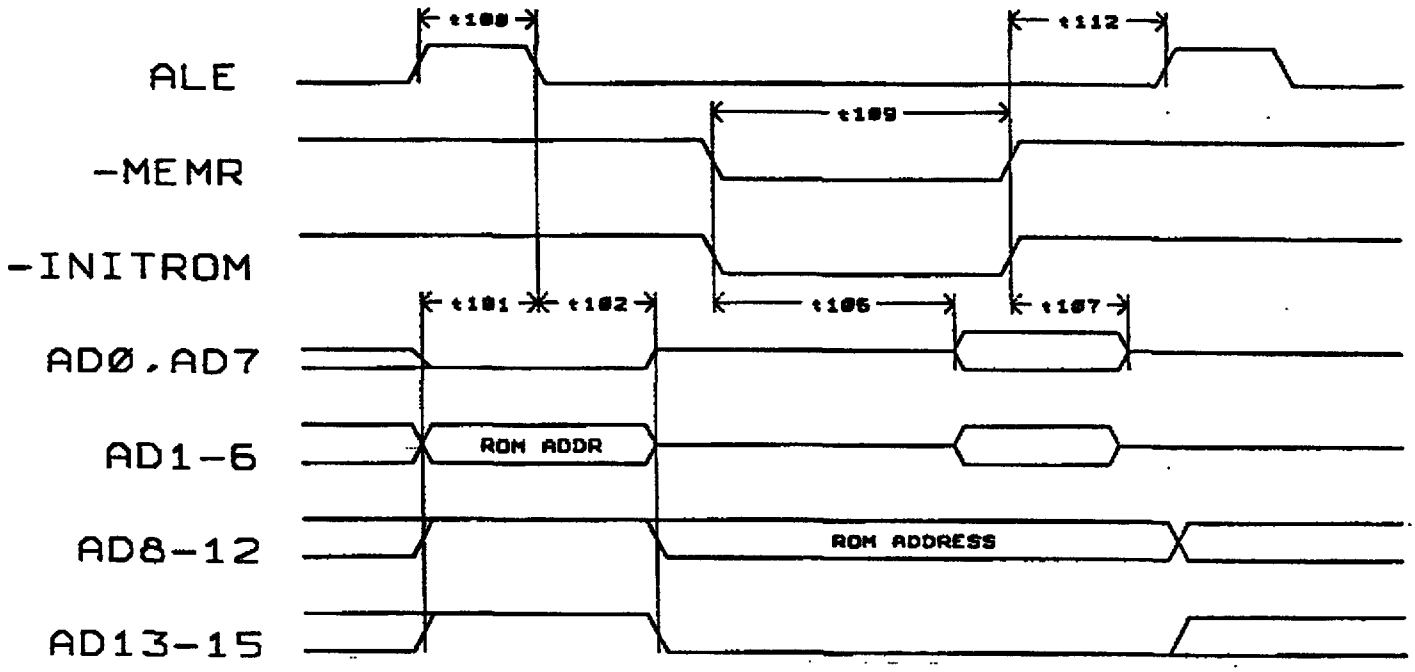
8.0 TIMING DIAGRAMS



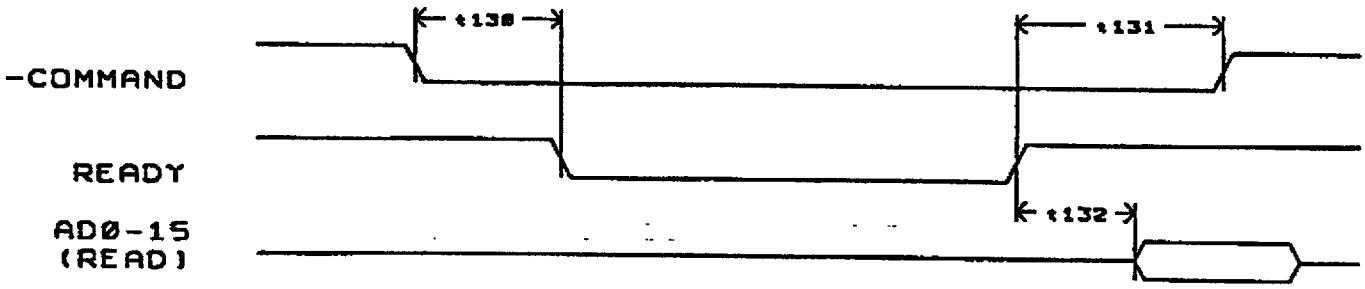
8.1 LOCAL BUS READ CYCLE



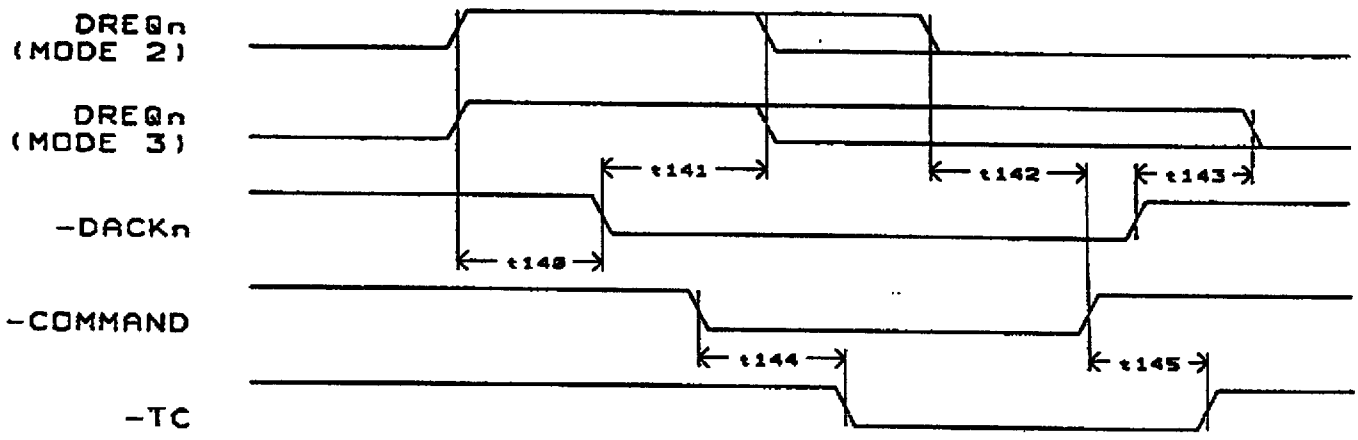
8.2 LOCAL BUS WRITE CYCLE



8.3 LOCAL BUS INIT ROM TIMING



8.4 LOCAL BUS READY TIMING

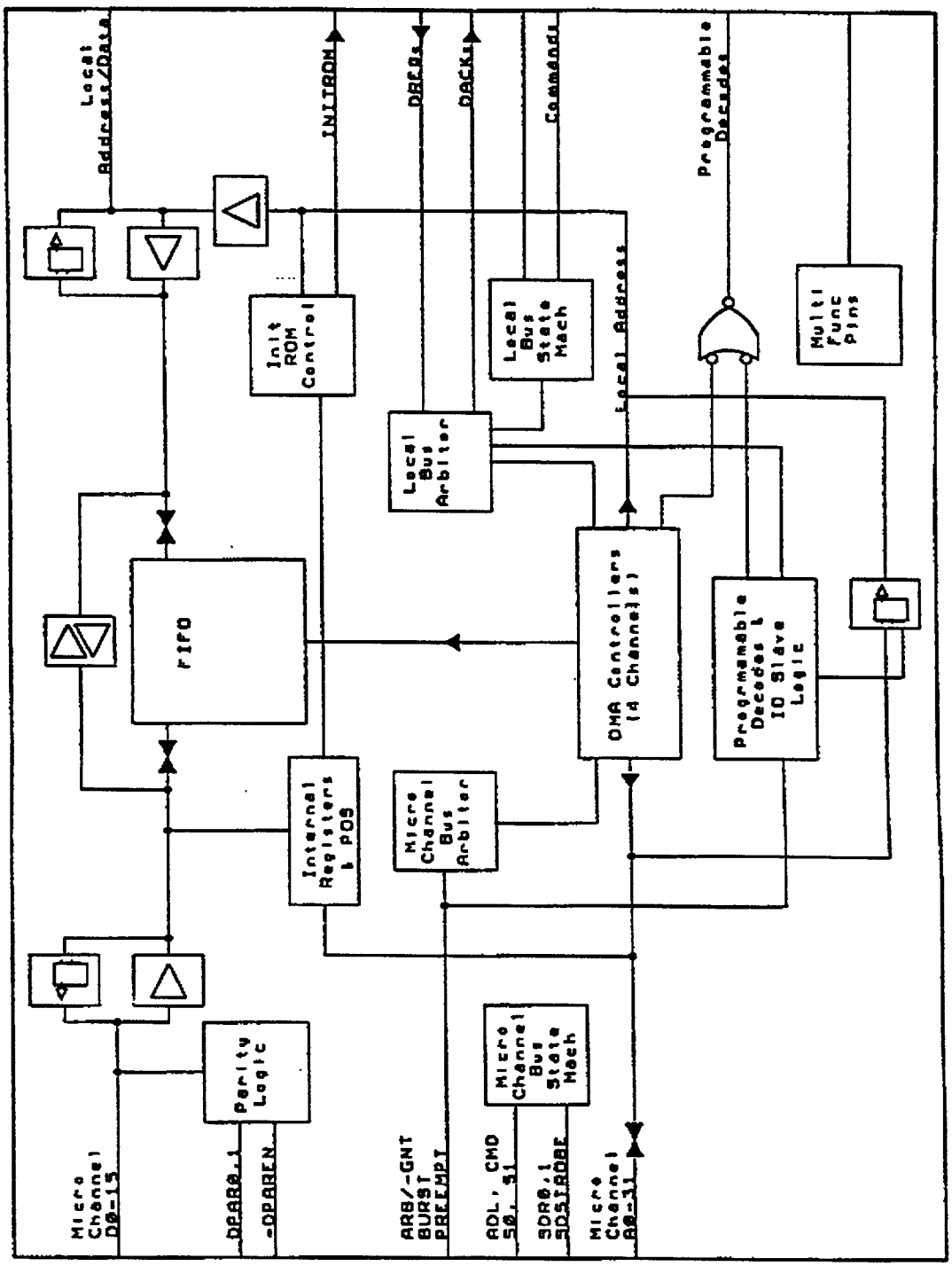


8.5 LOCAL BUS DREQ TIMING

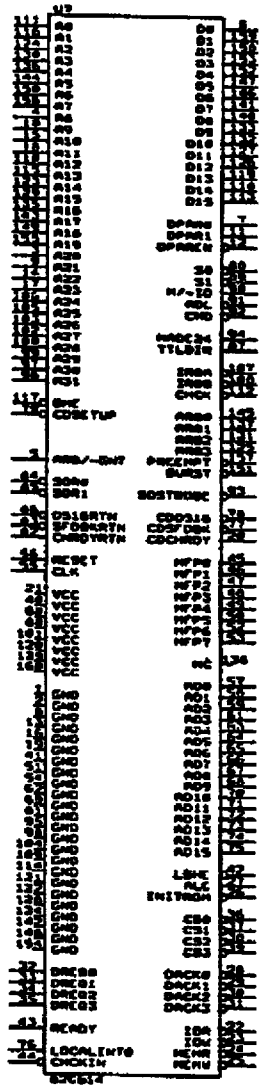
Appendix A

This appendix contains the following:

- 82C614 Block Diagram
- 82C614 Bus Master/Suggested Logic Symbol
- 82C614 Application Example
- 160 Pin PFP Pinout Diagram
- 160 Pin PFP Physical Dimension Diagram

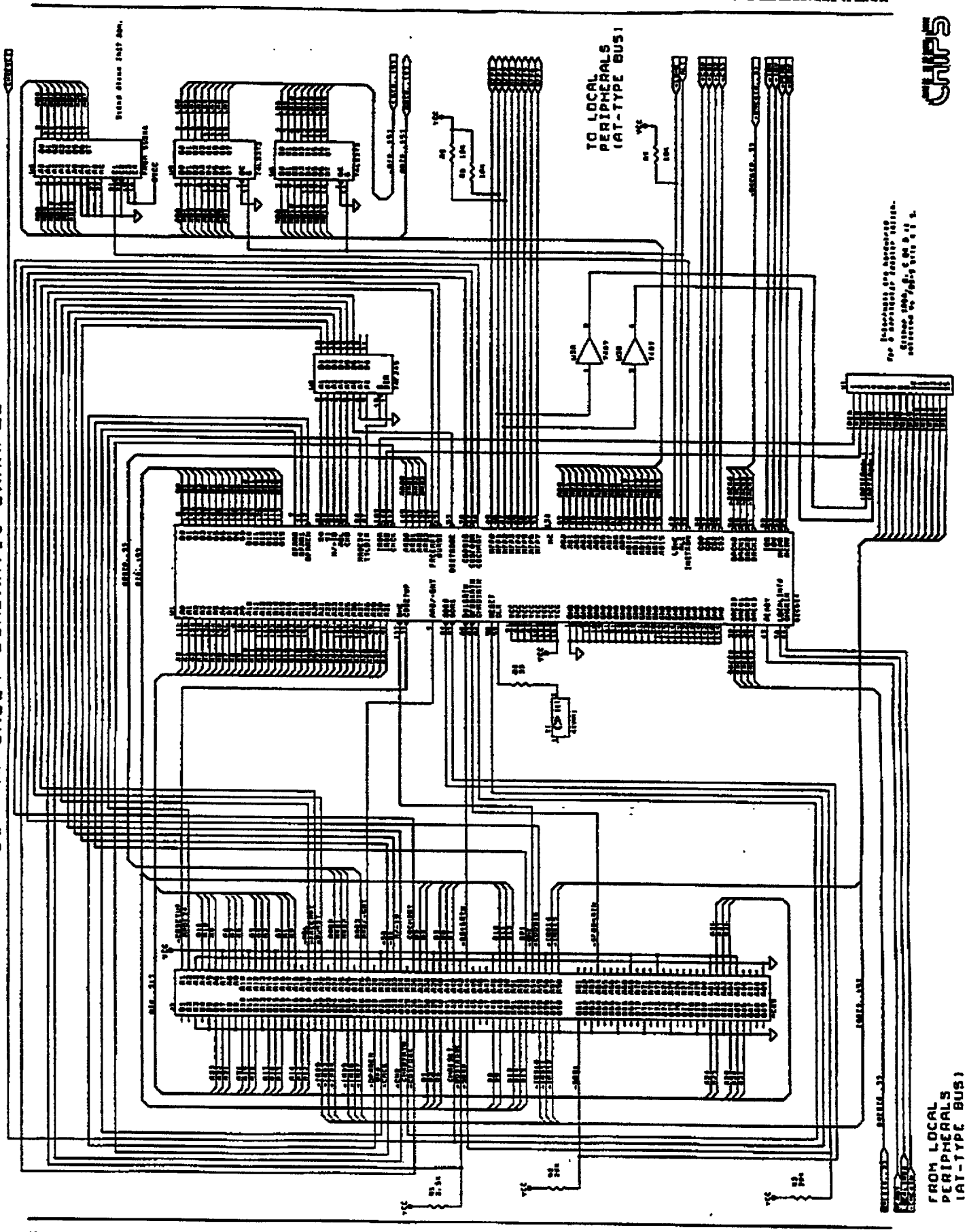


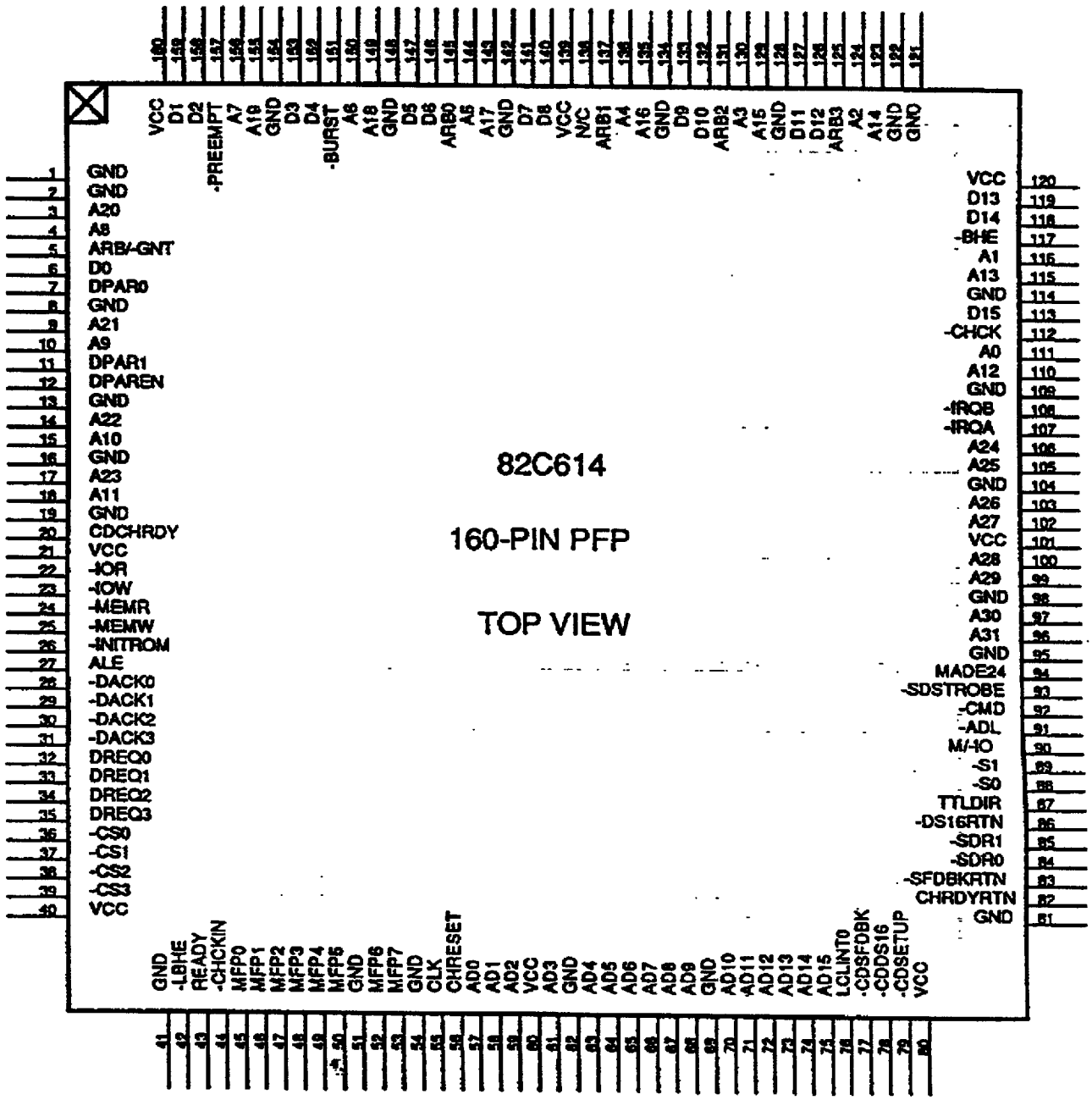
82C614 BUS MASTER MicroCHIP



SUGGESTED LOGIC SYMBOL

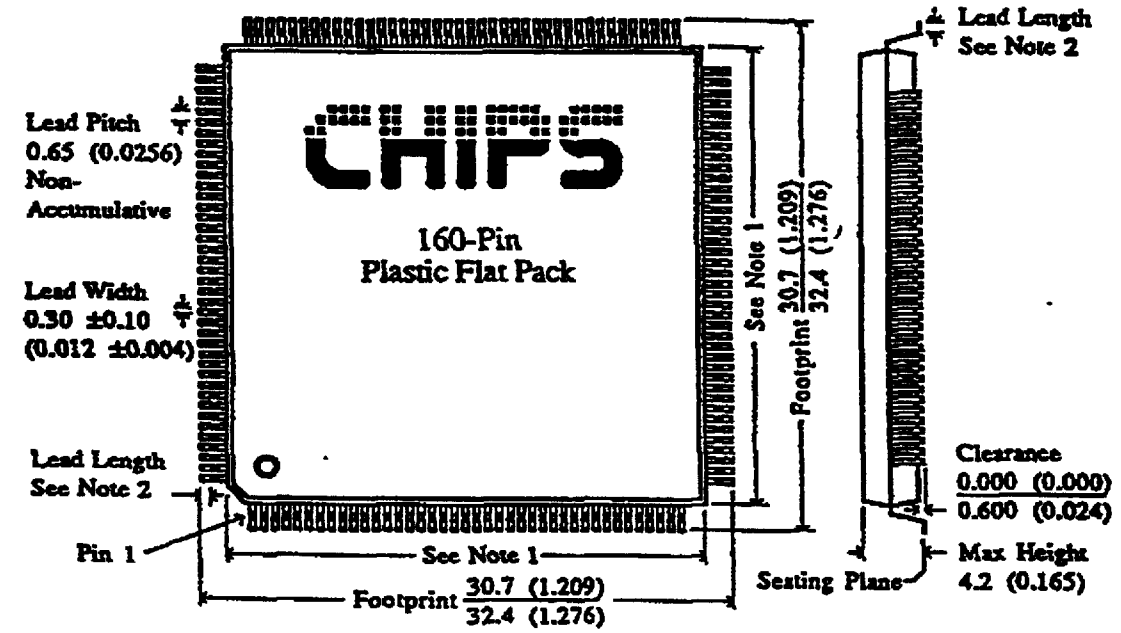
SINGLE SHEET SCHEMATIC EXAMPLE





REVISIONS				
REV.	SIM	DESCRIPTION	DATE	APPROVED
—	N/A	INITIAL RELEASE	7-1-91	

DIMENSIONS: mm (in)



Note 1: Package Body Size = 28 +0.2/-0.4 (1.102 +0.008/-0.016) (Swire)
Package Body Size = 28 ±0.2 (1.102 ±0.008) (All Other Package Vendors)

Note 2: Lead Length = 0.6 ±0.3 (0.024 ±0.012) (Package Vendor = Seiko)
Lead Length = 0.7 ±0.2 (0.028 ±0.008) (Package Vendor = Yamaha)
Lead Length = 0.8 ±0.2 (0.031 ±0.008) (All Other Package Vendors)

APPROVALS	DATE
DRAWN	
CHECKED	5-22-91
ISSUED	

CHIPS
Chips and Technologies, Inc.
3050 Zanker Road
San Jose, CA 95134

160 Pin Plastic Flat Package (Square)
DOCUMENT NO: MFG40001

SIZE	PSCM NO.	DWG. NO.	REV.
A		160SPFP-01	—
SCALE N/A		SHEET	OF