EXEL MICROELECTRONICS Excellence in E²

XL24C16

Advance Information

16,384-Bit Serial Electrically Erasable PROM
3 Volt and 5 Volt Operation

FEATURES

- **Low Power CMOS**
  - — Active current less than 1mA
  - — Standby current less than 2μA
- **Two Voltage Ranges**
  - — 2.7 to 5.5V
  - — 4.5 to 5.5V
- **Hardware Write Protection**
  - — Write Control pin
  - — Low Vcc lockout write protection (5V only)
- **Internally Organized as 2,048 x 8**
- **Two Wire Serial Interface (I²C™)**
  - — Bidirectional data transfer protocol
- **Sixteen-Byte Page-Write Mode**
  - — Minimizes total write time per byte
- **Automatic Word Address Incrementing**
  - — Sequential register read
- **Self-Timed Write Cycle**
  - — Maximum write cycle time of 10ms
- **High Reliability**
  - — Endurance: 100,000 cycles per byte
  - — Data retention: 10 years
- **8-Pin PDIP or SOIC Packages**

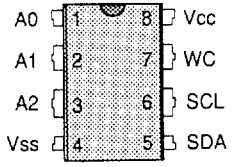
OVERVIEW

The XL24C16 is a low-cost 16,384-bit serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology and operates from a single 3 volt or 5 volt supply.

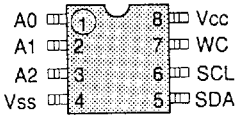
The XL24C16 is internally organized as eight 2K x 8 memory banks. The XL24C16 features a serial interface and software protocol allowing operation on a simple two-wire bus (I²C™). Only one XL24C16 may be connected to the 2-wire bus, due to I²C™ protocol.

PIN CONFIGURATIONS

Plastic Dual-in-line
"P" Package



EIAJ Small Outline
"JR" Package



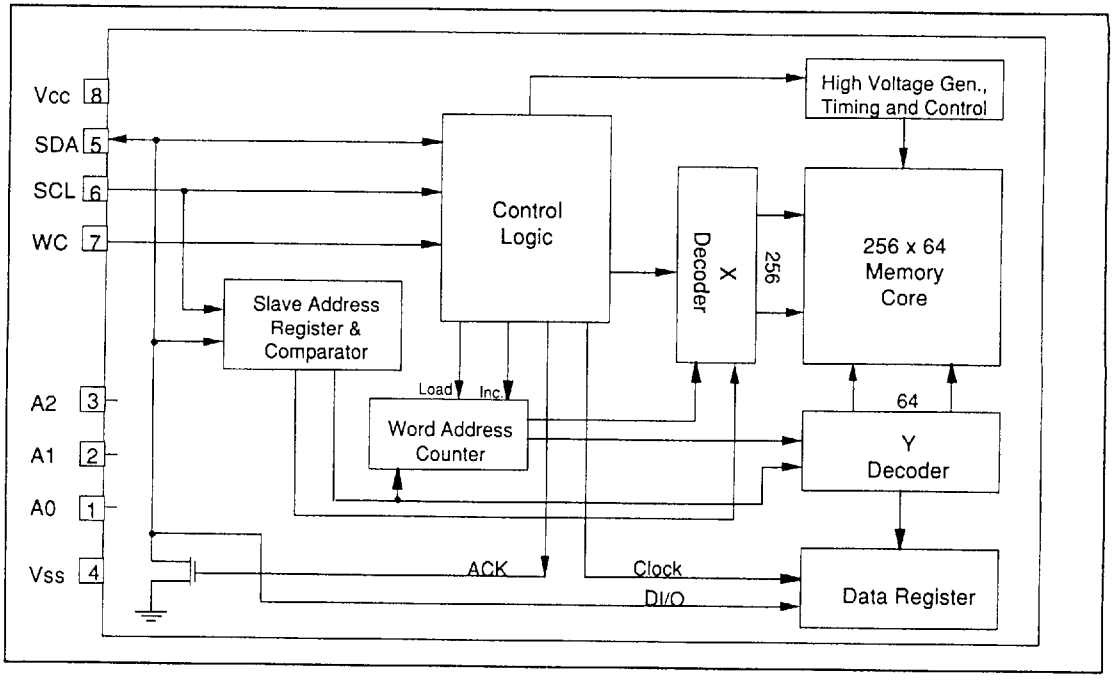
PIN NAMES

A0-A2	Address Inputs
SDA	Serial Data I/O
SCL	Serial Clock Input
WC	Write Control Input
V_{SS}	Ground
V_{CC}	Supply Voltage

EXEL

Advance Information

BLOCK DIAGRAM



PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock all data into and out of the device. In the WRITE mode, data must remain stable when SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW. It is an open-drain output, and may be wire-ORed with any number of open-drain or open-collector outputs.

A0, A1 and A2 - The address inputs are unused on the XL24C16 and are not connected. They may be tied HIGH, LOW or left open.

Write Control (WC) - The Write Control input is used to disable any attempt to write to the memory. When HIGH, the memory is protected; when LOW, the write function is normal.

ENDURANCE AND DATA RETENTION

The XL24C16 is designed for applications requiring up to 100,000 write cycles and unlimited read cycles. It provides ten years of secure data retention, with or without power applied, after the execution of 100,000 write cycles.

APPLICATIONS

The XL24C16 is ideal for high volume applications requiring low power and low density storage. This device uses a low-cost, space-saving 8-pin plastic package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation.

Vcc Lockout — Inadvertent WRITE Protection (5V parts only)

To insure against inadvertent WRITE operations, the XL24C16 has been equipped with an internal Vcc sensor circuit, which inhibits data alteration when the supply voltage falls below V_{WI}. If the applied Vcc is below 3.0V (typical), the XL24C16 is inhibited from executing WRITE operations, thereby protecting the nonvolatile data from being altered inadvertently.

CHARACTERISTICS OF THE I²C™ BUS

General Description

The I²C™ bus was designed for 2-way, 2-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus. Refer to Figure 1 below, "Typical System Configuration." Data transfer may be initiated only when the bus is "not busy," which is defined as both SCL and SDA inputs being HIGH.

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, because changes on the data line at this time will be interpreted as control signals. Refer to Figure 2 below.

START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the "STOP" condition. Refer to Figure 3 below.

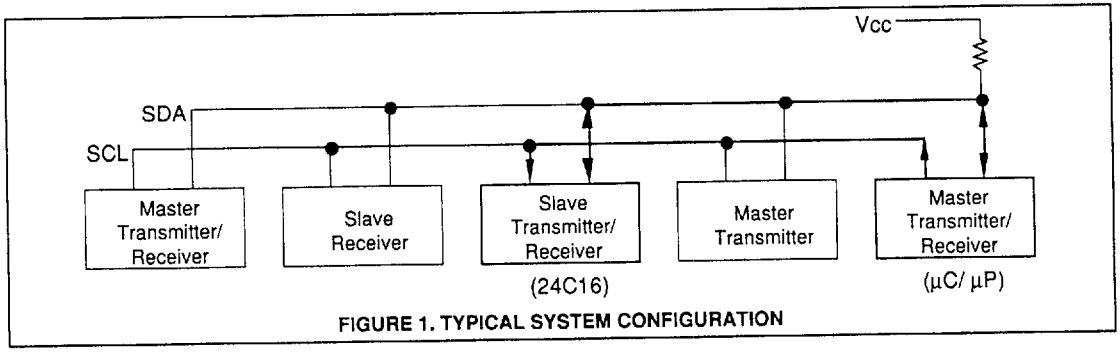


FIGURE 1. TYPICAL SYSTEM CONFIGURATION

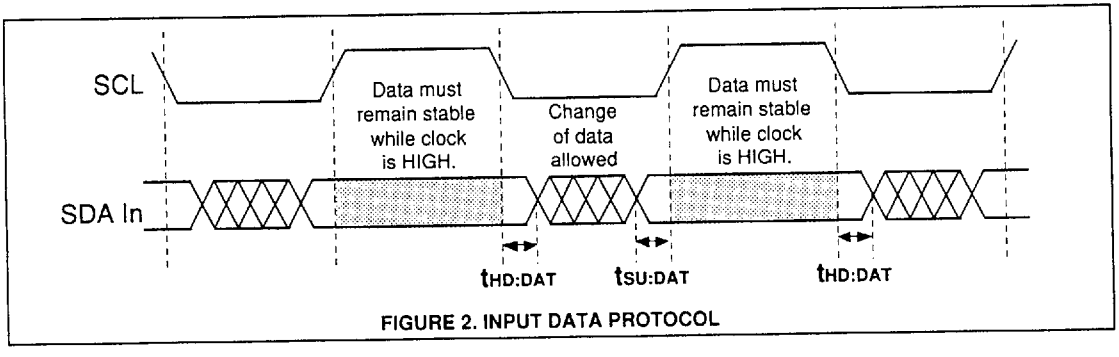


FIGURE 2. INPUT DATA PROTOCOL

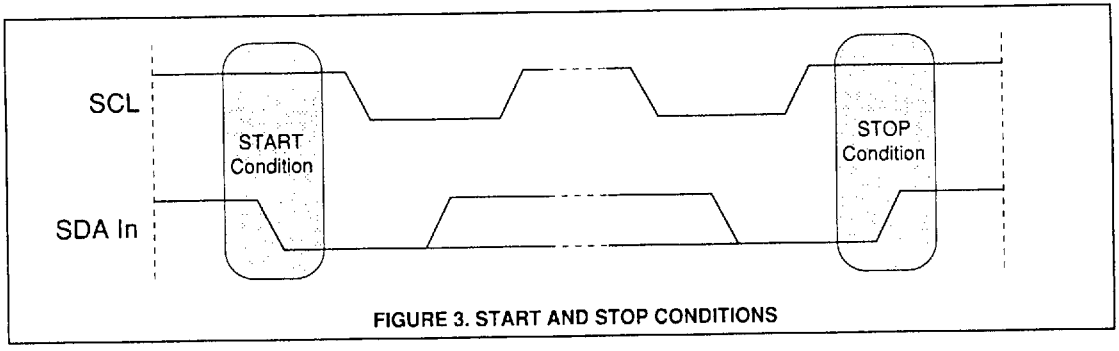


FIGURE 3. START AND STOP CONDITIONS

Advance Information

DEVICE OPERATION

The XL24C16 is a 16,384-bit serial E²PROM. The device supports a bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter," and the receiving device as the "receiver." The device controlling the data transmission is the "master," and the controlled device is the "slave." In all cases, the XL24C16 will be a "slave" device, since it never initiates any data transfers.

A single XL24C16 may be connected to the bus. This is due to the fact that the I²C™ protocol is limited to 16K addresses. The A0, A1 and A2 inputs are not connected.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data. (See Figure 4.)

The XL24C16 will respond with an ACKnowledge after recognition of a START condition and its slave address. If both the device and a WRITE operation have been selected, the XL24C16 will respond with an ACKnowledge, after the receipt of each subsequent 8-bit word.

In the READ mode, the XL24C16 will transmit eight bits of data, release the SDA line, and monitor the line for an ACKnowledge. If an ACKnowledge is detected, and no STOP condition is generated by the master, the XL24C16 will continue to transmit data. If an ACKnowledge is not detected, the XL24C16 will terminate further data transmissions. The master must then issue a STOP condition to return the XL24C16 to the standby power mode.

Slave Address Byte

Following a START condition, the master must output the address of the slave that it is accessing. The most significant four bits of the slave address are the "device type identifier." For an I²C™ memory device, this is fixed as 1010. Refer to Figure 5 below.

The next three significant address bits address a particular bank in the device. They are, in effect, A10, A9 and A8 of the memory device.

The last bit of the slave address defines the operation to be performed. When set to "1," a READ operation is selected; when set to "0," a WRITE operation is selected.

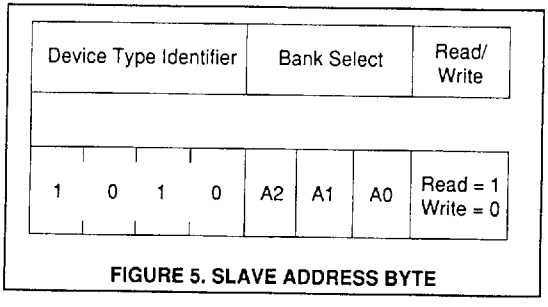


FIGURE 5. SLAVE ADDRESS BYTE

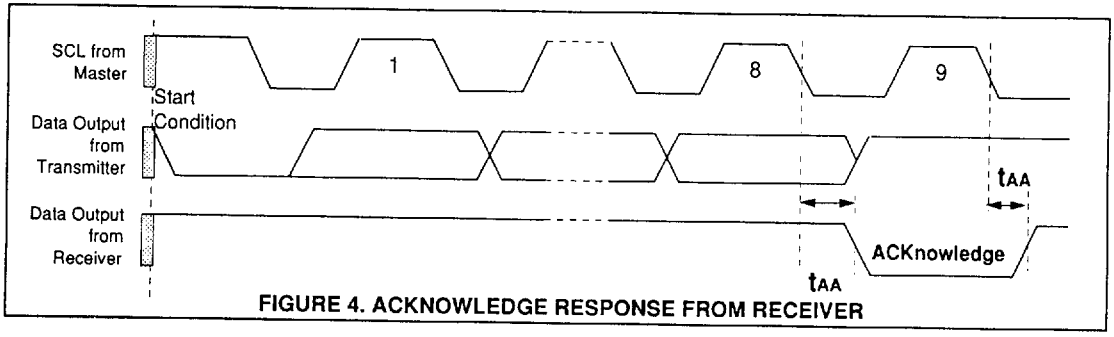


FIGURE 4. ACKNOWLEDGE RESPONSE FROM RECEIVER

WRITE OPERATIONS

Byte WRITE

For a WRITE operation, the XL24C16 requires a second address field. This address field is the word address, comprised of eight bits, which provides access to any one of the 2K words of memory which reside in each bank.

Upon receipt of the word address, the XL24C16 responds with an ACKnowledge, and waits for the next eight bits of data, again responding with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the XL24C16 begins the internal WRITE cycle to the nonvolatile array.

While the internal WRITE cycle is in progress, the XL24C16 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 6 below for the address, ACKnowledge, and data transfer sequence.

Page WRITE

The XL24C16 is capable of a 16-byte page-WRITE operation. It is initiated in the same manner as the byte-WRITE operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to 15 more words. After the receipt of each word, the XL24C16 will respond with an ACKnowledge.

After the receipt of each word, the four low order address bits are internally incremented by one. The high order four bits of the address remain constant. If the master should transmit more than 16 words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-WRITE operation, all inputs are disabled until completion of the internal WRITE cycle. Refer to Figure 6 below for the address, ACKnowledge, and data transfer sequence.

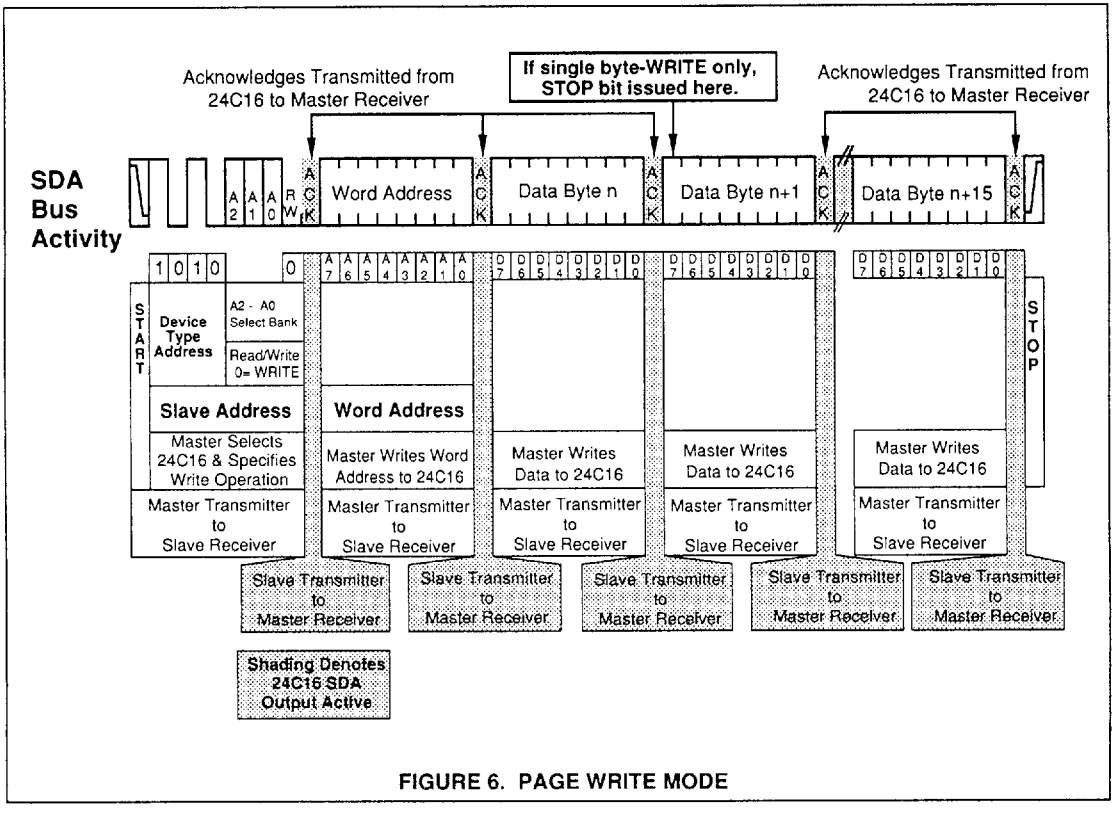


FIGURE 6. PAGE WRITE MODE

Acknowledge Polling

When the XL24C16 is performing an internal WRITE operation, it will not recognize a START condition. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation. Refer to Figure 7 below.

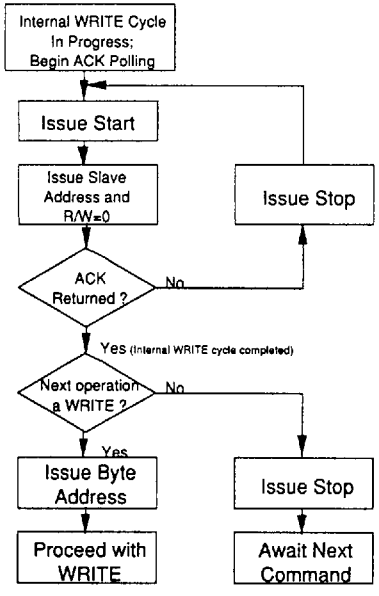


FIGURE 7. ACKNOWLEDGE POLLING

READ OPERATIONS

READ operations are initiated in the same manner as WRITE operations, except that the R/W bit of the slave address byte is set to "1." There are four different READ operation options:

1. Current Address Byte READ
2. Random Address Byte READ
3. Current Address Sequential READ
4. Random Address Sequential READ

Current Address Byte READ

The XL24C16 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a READ or a WRITE) was to address n, the next READ operation would access data from address n+1, and update the current address pointer. When the XL24C16 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address n+1.

If the current address READ operation only accesses a single byte of data, the master does not acknowledge the transfer, but does generate a STOP condition. At this point, the XL24C16 discontinues transmission. See Figure 8 below for the address, acknowledge, and data transfer sequence.

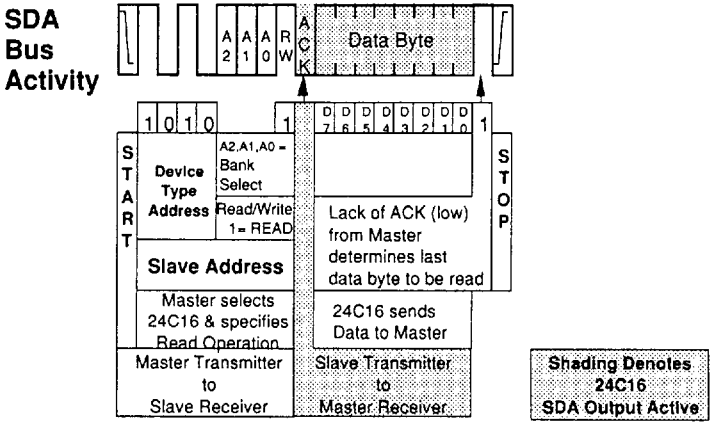


FIGURE 8. CURRENT ADDRESS BYTE READ MODE

READ OPERATIONS (continued)

Random Address Byte READ

Random address READ operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a WRITE command which includes the START condition and the slave address field (with the R/W bit set to "0"), followed by the address of the word it is to READ. This procedure sets the internal address counter of the XL24C16 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a START condition followed by another slave address field with the R/W bit set to "1." The XL24C16 will respond with an acknowledge and transmit the eight data bits stored at the addressed location. At this point, the master does not acknowledge the transmission, but does generate the STOP condition. The XL24C16 discontinues transmission and reverts to its standby power mode. See Figure 9 below for the address, acknowledge, and data transfer sequence.

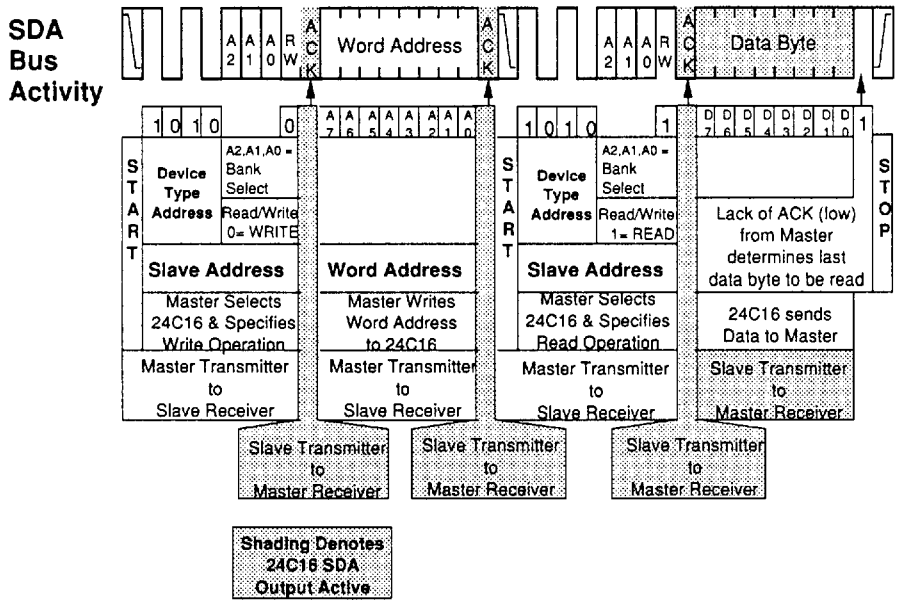


FIGURE 9. RANDOM ACCESS BYTE READ MODE

READ OPERATIONS (continued)

Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes; however, the master now responds with an ACKnowledge, indicating that it requires additional data from the XL24C16. The XL24C16 continues to output data for each ACKnowledge received. The sequential READ operation is terminated by the master, by not responding with an ACKnowledge, and by issuing a STOP condition.

The data output is sequential, with the data from address n followed by the data from address n+1. The address counter for READ operations increments automatically, as well as the bank address, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 2,047), the counter "rolls over" to address 0, and the XL24C16 continues to output data for each ACKnowledge received.

Refer to Figure 10 below for the address, ACKnowledge, and data transfer sequence. Figure 10 shows a sequential READ starting with a random address. A sequential READ may also begin with a current address READ.

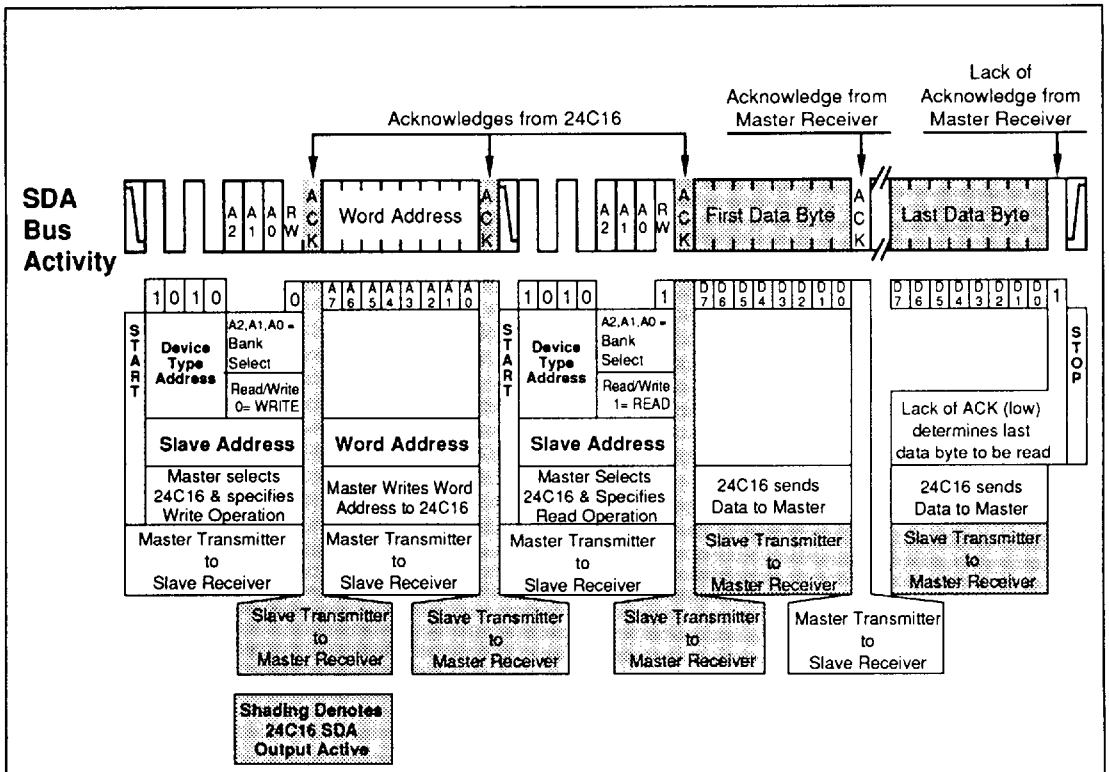


FIGURE 10. SEQUENTIAL READ OPERATION (starting with a Random Address READ)

EXEL

XL24C16

Advance Information

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias: ..... -40°C to +85°C
Storage Temperature ..... -65°C to +125°C
Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.5V to V_{CC}+0.5V
ESD Voltage (JEDEC method) 2,000V
Output Current ..... +5mA

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS24C16 or -40°C to +85°C for the XLE24C16, V_{CC} = 3V±10% or 5V±10%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs=GND or Vcc			1	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = Vcc All other inputs = GND or Vcc			2	µA
I_{LI}	Input Leakage	V_{IN} = 0 to Vcc			10	µA
I_{LO}	Output Leakage	V_{OUT} = 0 to Vcc			10	µA
V_{IL}	Input Low Voltage	SCL, SDA			0.3 x V_{CC}	V
V_{IH}	Input High Voltage	SCL, SDA	0.7 x V_{CC}			V
V_{OL}	Output Low Voltage	I_{OL} = 3mA			0.4	V
V_{WI}	Write Inhibit Voltage	(5 volt part only)	2.5	3.4	4.5	V

CAPACITANCE

T_A = 25°C, f = 100KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

Advance Information

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS24C16 or -40°C to +85°C for the XLE24C16, V_{CC} = 3V±10% or 5V±10%

Symbol	Parameter	Conditions	Min	Max	Units
f_{SCL}	SCL Clock Frequency		0	100	KHz
t_{LOW}	Clock Low Period		4.7		µs
t_{HIGH}	Clock High Period		4.0		µs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		µs
$t_{SU:STA}$	Start Condition Setup Time		4.7		µs
$t_{HD:STA}$	Start Condition Hold Time		4.0		µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		µs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	µs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		µs
t_R	SCL and SDA Rise Time			1000	ns
t_F	SCL and SDA Fall Time			300	ns
$t_{SU:DAT}$	Data In Setup Time		250		ns
$t_{HD:DAT}$	Data In Hold Time		0		ns
T_I	Noise Spike Width	Time Constant @ SCL, SDA Inputs		100	ns
t_{WR}	Write Cycle Time			10	ms

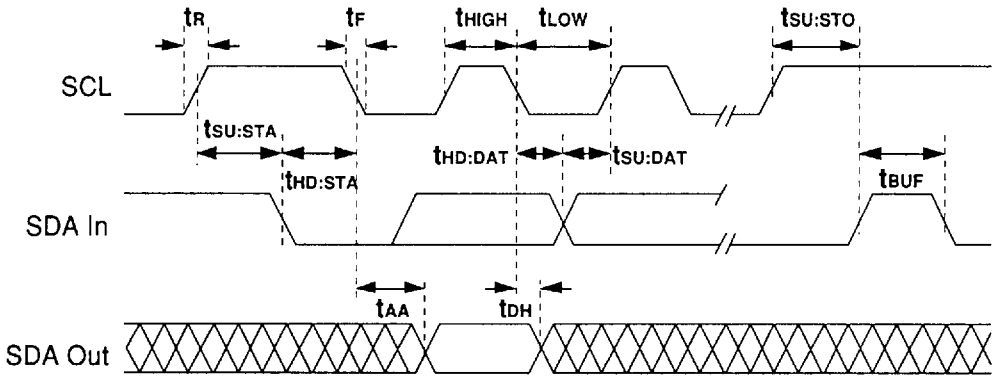


FIGURE 11. BUS TIMING