INTRODUCTION

The S6A2068 is a dot matrix LCD driver & controller LSI which is fabricated by low power CMOS technology.

FUNCTION

— Character type dot matrix LCD driver & controller
— Internal driver: 16 common and 60 segment signal output
— Display character format: 5 × 7 dots + cursor, 5 × 10 dots + cursor
— Easy interface with a 4-bit or 8-bit MPU
— Display character pattern: 5×7 dots format: 192 kinds, 5×10 dots format: 32 kinds
— The special character pattern is directly programmable by the Character Generator RAM.
— A customer character pattern programmable by mask option
— Automatic power on reset function
— It can drive a maximum of 80 characters by using the S6A0065 or S6A2067 externally.
— It is possible to read both Character Generator and Display Data RAM from MPU.

FEATURES

— Internal Memory
  – Character Generator ROM: 8,320bits
  – Character Generator RAM: 512 bits
  – Display Data RAM: 80 × 8bits (80 characters max.)
— Power Supply Voltage; 2.7 to 5.5V
— Supply voltage for display: 0 to -5 V (V5)
— CMOS process
— 1/8 duty, 1/11 duty or 1/16 duty: programmable
  (1/8 duty; 5 × 7 dots format 1-line, 1/11 duly; 5 × 10 dots format 1-line, 1/16 duty: 5 × 7 dots format 2-line)
— 100 QFP or bare chip available

Precautions for Light

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.
2. Always test and inspect products under the environment with no penetration of light.

BLOCK DIAGRAM

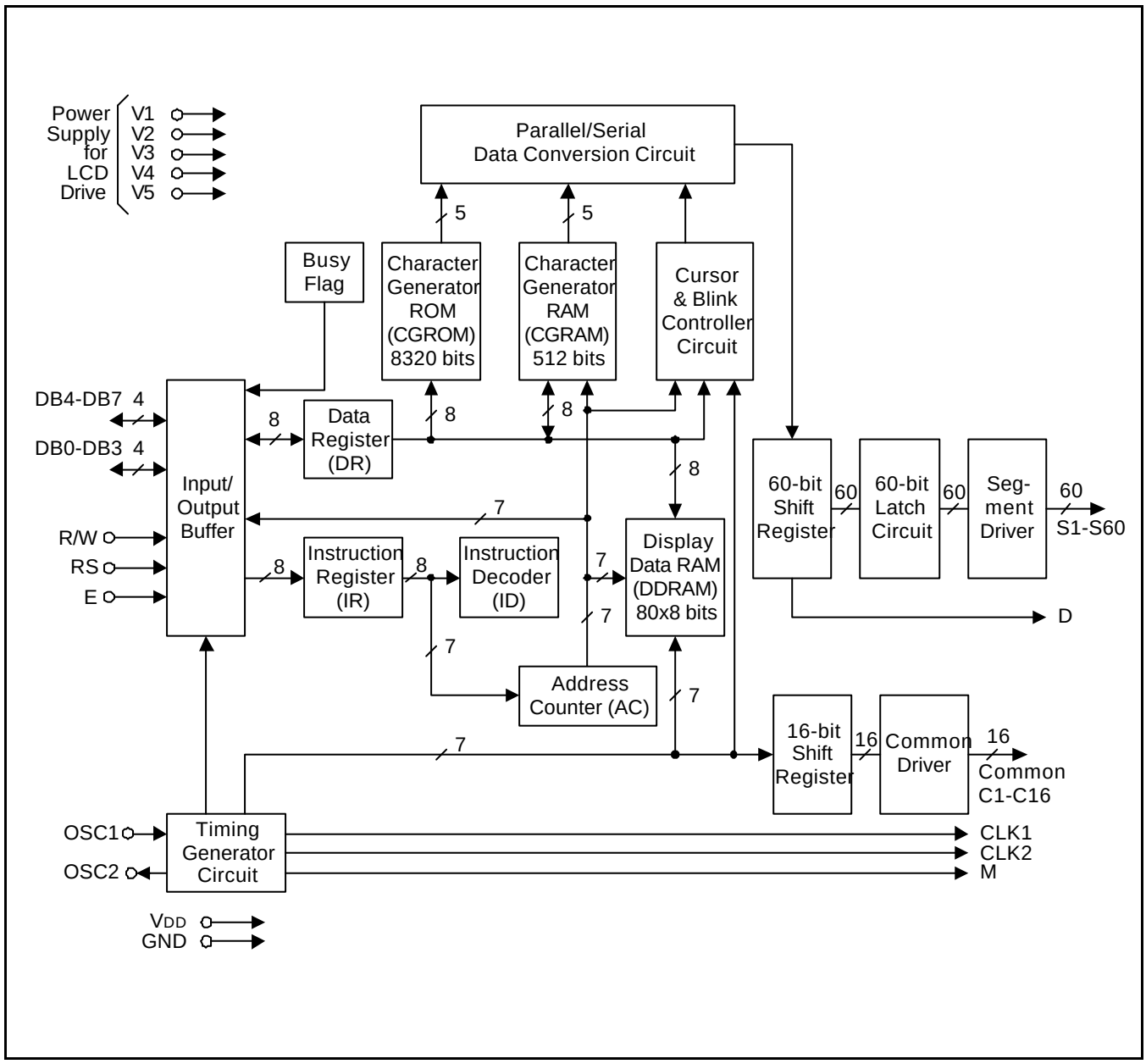


Figure 1. S6A2068 Block Diagram

PIN CONFIGURATION

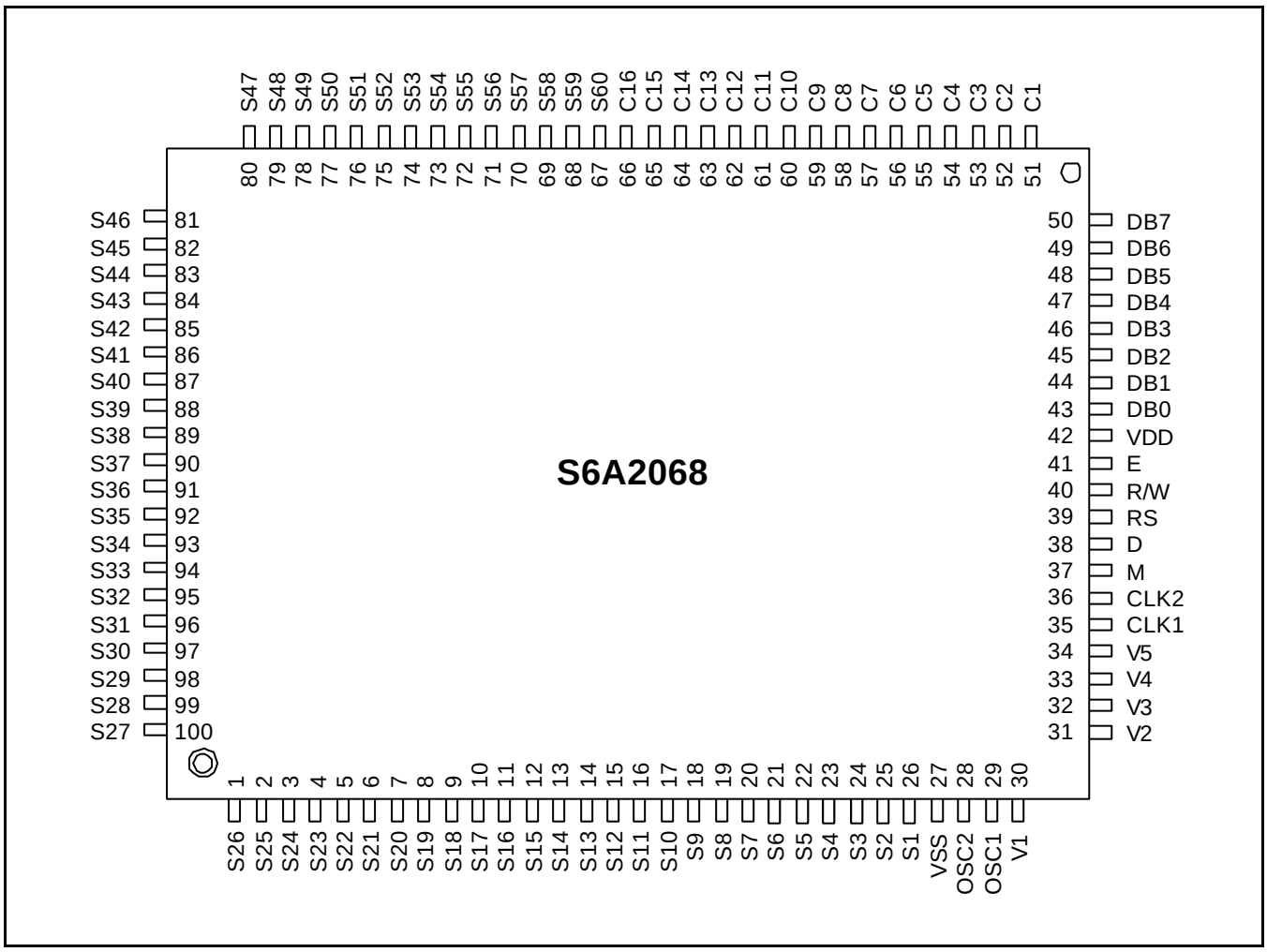


Figure 2. S6A2068 Pin Configuration

PAD DIAGRAM

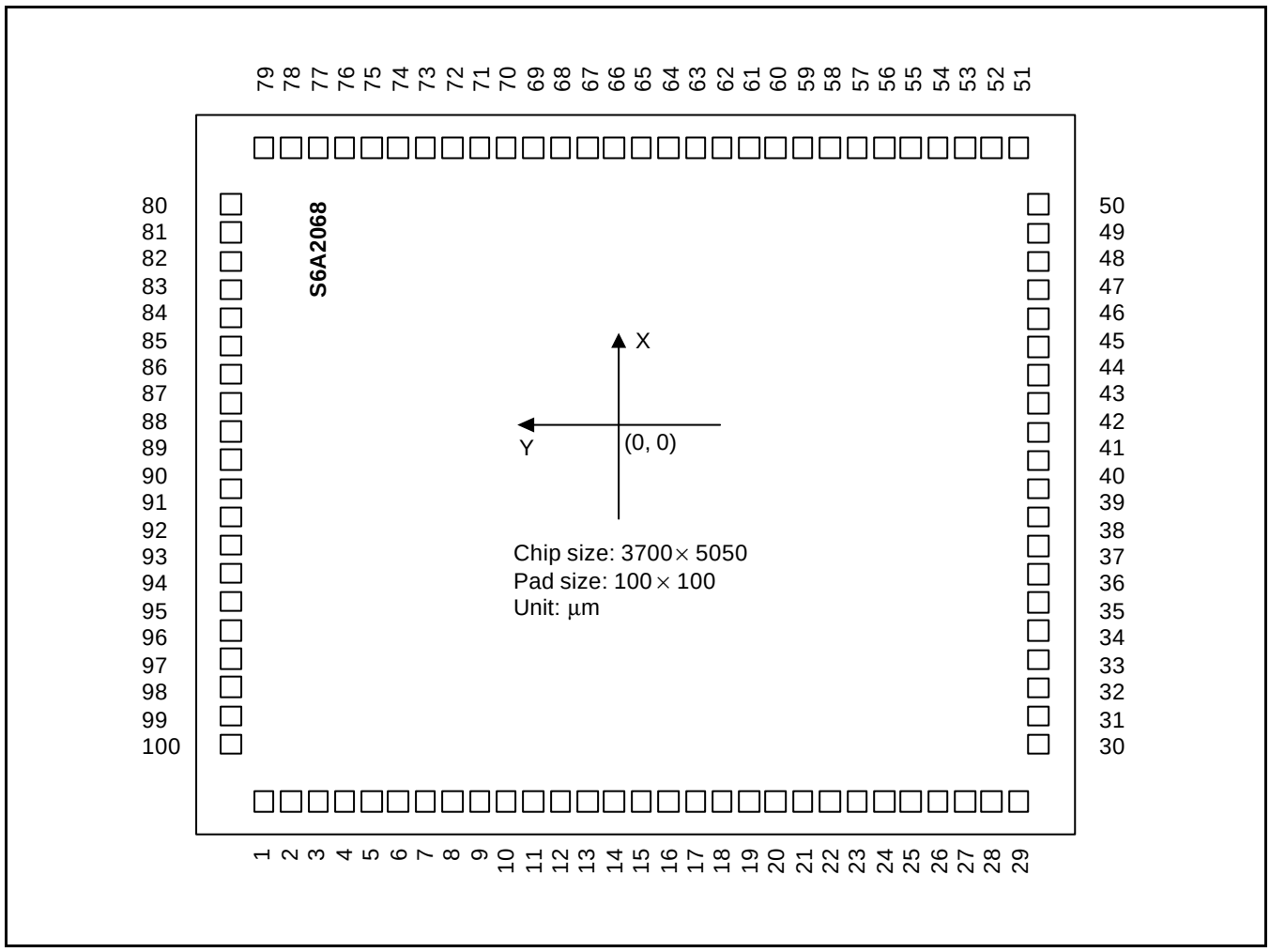


Figure 3. S6A2068 Pad Diagram

* S6A2068 Marking: easy to find the PAD No. 77, 82

PAD LOCATION

[Unit: μm] **Table 1. S6A2068 Pad Location**

PAD NUM.	PAD NAME	COORDINATE X	COORDINATE Y	PAD NUM.	PAD NAME	COORDINATE X	COORDINATE Y	PAD NUM.	PAD NAME	COORDINATE X	COORDINATE Y
1	S26	-1684	1686	35	CLK1	-453	-2358	69	S58	1684	436
2	S25	-1684	1560	36	CLK2	-328	-2358	70	S57	1684	560
3	S24	-1684	1436	37	M	-203	-2358	71	S56	1684	686
4	S23	-1684	1310	38	D	-78	-2358	72	S55	1684	810
5	S22	-1684	1186	39	RS	47	-2358	73	S54	1684	936
6	S21	-1684	1060	40	R/W	172	-2358	74	S53	1684	1060
7	S20	-1684	936	41	E	297	-2358	75	S52	1684	1186
8	S19	-1684	810	42	VDD	422	-2358	76	S51	1684	1310
9	S18	-1684	686	43	DB0	547	-2358	77	S50	1684	1436
10	S17	-1684	560	44	DB1	672	-2358	78	S49	1684	1560
11	S16	-1684	436	45	DB2	797	-2358	79	S48	1684	1686
12	S15	-1684	310	46	DB3	922	-2358	80	S47	1249	2358
13	S14	-1684	186	47	DB4	1047	-2358	81	S46	1124	2358
14	S13	-1684	60	48	DB5	1172	-2358	82	S45	999	2358
15	S12	-1684	-64	49	DB6	1297	-2358	83	S44	874	2358
16	S11	-1684	-190	50	DB7	1422	-2358	84	S43	749	2358
17	S10	-1684	-314	51	C1	1684	-1814	85	S42	624	2358
18	S9	-1684	-440	52	C2	1684	-1690	86	S41	499	2358
19	S8	-1684	-564	53	C3	1684	-1564	87	S40	374	2358
20	S7	-1684	-690	54	C4	1684	-1440	88	S39	249	2358
21	S6	-1684	-814	55	C5	1684	-1314	89	S38	124	2358
22	S5	-1684	-940	56	C6	1684	-1190	90	S37	-1	2358
23	S4	-1684	-1064	57	C7	1684	-1064	91	S36	-126	2358
24	S3	-1684	-1190	58	C8	1684	-940	92	S35	-251	2358
25	S2	-1684	-1314	59	C9	1684	-814	93	S34	-376	2358
26	S1	-1684	-1440	60	C10	1684	-690	94	S33	-501	2358
27	VSS	-1684	-1702	61	C11	1684	-564	95	S32	-626	2358
28	OSC2	-1684	-1868	62	C12	1684	-440	96	S31	-751	2358
29	OSC1	-1684	-1994	63	C13	1684	-314	97	S30	-876	2358
30	V1	-1078	-2358	64	C14	1684	-190	98	S29	-1001	2358
31	V2	-953	-2358	65	C15	1684	-64	99	S28	-1126	2358
32	V3	-828	-2358	66	C16	1684	60	100	S27	-1251	2358
33	V4	-703	-2358	67	S60	1684	186				
34	V5	-578	-2358	68	S59	1684	310				

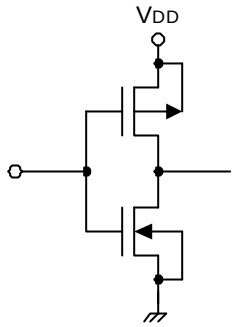
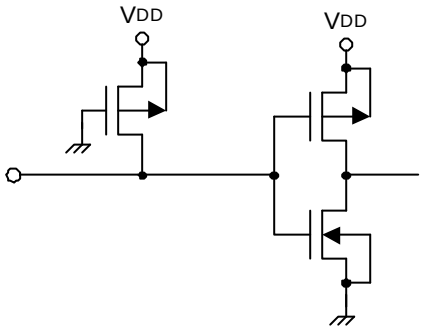
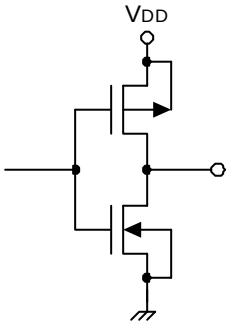
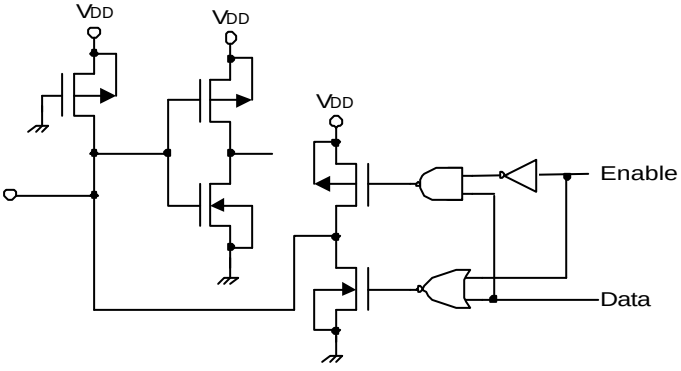
NOTE: "S6A2068" Marking: easy to find the PAD No. 77, 82.

PIN DESCRIPTION

Table 2. S6A2068 Pin Description

PIN (No).	I/O	Name	Description	Interface
V_{DD}(42)	Power	Power supply	for logical circuit (2.7V to 5.5V)	Power Supply
V_{SS}(GND) (27)			0V (GND)	
V1-V5(30-34)			Bias voltage level for LCD driving	
S1-S60 (1-26, 67-100)	Output	Segment output	Segment signal output for LCD driving	LCD
C1-C16 (51-66)	Output	Common output	Common signal output for LCD driving	LCD
OSC1, OSC2 (29) (28)	Input (OSC1) Output (OSC2)	Oscillator	Both pin connected to Rf resistor for internal oscillator circuit. In case of external frequency use only, the frequency is input to OSC1 terminal.	Resistor
CLK1 (35)	Output	Data latch clock	Clock output terminal for the serially transferred data to be latched to the driver.	S6A0065 or S6A2067
CLK2 (36)		Data shift clock	Clock output terminal used when D terminal data output shifts the inside of the driver.	
M (37)		Alternated signal for LCD driver output	The alternating signal to convert LCD drive waveform to AC.	
D (38)		Display data interface	Character pattern data, which is corresponding to each common signal, is supplied to driver serially.	
E (41)	Input	Read/Write Enable	Start enable signal to read or write the data	MPU
R/W (40)		Read/Write	R/W signal input is used to select the read/write mode	
RS (39)		Register select	register selection input	
DB0-DB7 (43-50)	Input/ Output	Data interface	Used for data transfer between the MPU and S6A2068. These terminals are for data bus with bi-directional three-state. First 4-bit (DB0-DB3) are not used during 4-bit operation (DB7 can be used as a busy flag).	

Internal logic of input/output terminal

Input/Output	Logic Diagram		Applicable pin
Input	No Pull up		E
	with pull up		RS, R/W
Output			CLK1, CLK2 M, D
Input/Output			DB0-DB7

MAXIMUM ABSOLUTE LIMIT

(T_A = 25°C)

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	-0.3 to +7.0	V
Driver Supply Voltage	V_{LCD}	V_{DD} - 11.5 to V_{DD} + 0.3	V
Input Voltage	V_{IN}	-0.3 to V_{DD} + 0.3	V
Power Dissipation	P_D	500	MW
Operating Temperature	T_{OPR}	-30 to +85	°C
Storage Temperature	T_{STG}	-55 to + 125	°C

NOTE: Voltage greater than above may damage the circuit ($V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$)

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = -30 to +85°C)

Characteristic		Symbol	Test condition	Min	Typ	Max	Unit	Applicable Pin
Operating Voltage		V_{DD}	–	4.5	–	5.5	V	
Operating Current (*1)		I_{DD1}	Ceramic resonator f_{OSC} = 250kHz	–	0.65	0.9	mA	
		I_{DD2}	Resistor oscillation external clock operation f_{OSC} = 270kHz	–	0.45	0.7		
Input Voltage 1	High	V_{IH1}	–	2.2	–	V_{DD}	V	E, DB0-DB7,
	Low	V_{IL1}	–	-0.3	–	0.6		R/W, RS
Input Voltage 2	High	V_{IH2}	–	V_{DD}-1.0	–	V_{DD}		OSC1
	Low	V_{IL2}	–	-0.2	–	1.0		
Output Voltage 1	High	V_{OH1}	I_{OH} = -0.205mA	2.4	–	–		DB0-DB7
	Low	V_{OL1}	I_{OL} = 1.2mA	–	–	0.4		
Output Voltage 2	High	V_{OH2}	I_O = -40µA	0.9V_{DD}	–	–		CLK1, LK2, M, D
	Low	V_{OL2}	I_O = 40µA	–	–	0.1V_{DD}		
Voltage Drop (*2)	COM	Vd_{COM}	I_O = ± 0.1mA	–	–	1		C1-C16
	SEG	Vd_{SEG}		–	–	1		S1-S60
Input Leakage Current		I_{LKG}	V_{IN} = 0 V or V_{DD}	-1	–	1	µA	E
Input Low Current		I_{IN}	V_{DD} = 5V(test pull up R)	-50	-125	-250		RS, R/W
External Clock	Frequency (*3)	f_{EC}	–	125	250	350	kHz	OSC1
	Duty	duty		45	50	55	%	
	Rise time	t_R		–	–	0.2	µs	
	Fall time	t_F		–	–	0.2	µs	
Internal Clock Frequency (*3)		f_{OSC1}	Rf = 91kΩ ±2% V_{DD} = 5V	190	270	360	kHz	OSC1, OSC2
LCD Driving Voltage (*4)		V_{LCD1}	V_{DD}-V5 1/5 bias	4.6	–	10.0	V	V1-V5
		V_{LCD2}	1/4 bias	3.0	–	10.0		

DC Characteristics

(V_{DD} = 2.7V to 4.5V, V_{SS} = 0V, T_A = -30 to +85°C)

Characteristic		Symbol	Test condition	Min	Typ	Max	Unit	Applicable Pin
Operating Voltage		V_{DD}	–	2.7	3.0	4.5	V	
Operating Current (*1)		I_{DD1}	Ceramic resonator f_{OSC} = 250kHz	–	0.3	0.5	mA	
		I_{DD2}	Resistor oscillation external clock operation f_{OSC} = 270kHz	–	0.17	0.3		
Input Voltage 1	High	V_{IH1}	–	1.9	–	VDD	V	E, DB0-DB7,
	Low	V_{IL1}	–	-0.3	–	0.4		R/W, RS
Input Voltage 2	High	V_{IH2}	–	$0.7V_{DD}$	–	V_{DD}		OSC1
	Low	V_{IL2}	–	–	–	$0.2V_{DD}$		
Output Voltage 1	High	V_{OH1}	I_{OH} = -0.205mA	2.0	–	–		DB0-DB7
	Low	V_{OL1}	I_{OL} = 1.2mA	–	–	0.4		
Output Voltage 2	High	V_{OH2}	I_O = -40µA	$0.8V_{DD}$	–	–		CLK1, CLK2,
	Low	V_{OL2}	I_O = 40µA	–	–	$0.2V_{DD}$		M, D
Voltage Drop (*2)	COM	Vd_{COM}	I_O = ± 0.1mA	–	–	1		C1-C16
	SEG	Vd_{SEG}		–	–	1.5		S1-S60
Input Leakage Current		I_{LKG}	V_{IN} = 0 V or V_{DD}	-1	–	1	µA	E
Input Low Current		I_{IN}	V_{DD} = 5V (test pull up R)	-10	-50	-120		RS, R/W
External Clock	Freq. (*3)	f_{EC}	–	125	250	350	kHz	OSC1
	Duty	duty		45	50	55	%	
	Rise time	t_R		–	–	0.2	µs	
	Fall time	t_F		–	–	0.2	µs	
Internal Clock Frequency (*3)		f_{OSC1}	Rf = 75kΩ ± 2% V_{DD} = 3V	190	270	350	kHz	OSC1, OSC2
LCD Driving Voltage		V_{LCD1}	V_{DD}-V5 1/5 bias	3.0	–	10.0	V	V1-V5
		V_{LCD2}	1/4 bias	3.0	-	10.0		

SAMSUNG ELECTRONICS

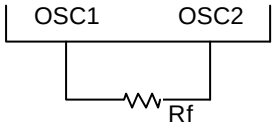
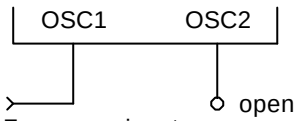
NOTES:

*1) The supply current value from V_{DD} when condition is as follows
V_{DD} = 5V, V_{SS} = 0V, V5 = -2V
V_{DD} = 3V, V_{SS} = 0V, V5 = -2V

*2) Applied to the voltage drop occurring from terminals V_{DD}, V1, V4 and V5 to each common terminal (C1-C16) when 0.1mA is flown in or out to and from all COM and SEG terminals, and also to voltage drop occurring from terminals V_{DD}, V2, V3 and V5 to each SEG terminal (S1-S60). When the output level is at V_{DD}, V1 or V2 level, 0.1mA is flown out, while 0.1mA flow in when the output level is at V3, V4 or V5 level. This occurs when 5 V or -5 V is input to V_{DD}, V1 and V3 or to V2, V4, and V5 respectively.

*3) and *4): Refer to oscillator circuit and input the voltage listed in the table bellow to V1-V5

*3) Oscillator circuit

Resistor Circuit	External Circuit
 Rf: 91kΩ ±2%	

*4) Input the voltage listed in the table below to V_1-V_5

Power supply	Duty 1/8, 1/11 Bias 1/4	Duty 1/16 Bias 1/5
V_1	V_{DD} - V_{LCD}/4	V_{DD} - V_{LCD}/5
V_2	V_{DD} - V_{LCD}/2	V_{DD} - 2V_{LCD}/5
V_3	V_{DD} - V_{LCD}/2	V_{DD} - 3V_{LCD}/5
V_4	V_{DD} - 3V_{LCD}/4	V_{DD} - 4V_{LCD}/5
V_5	V_{DD} - V_{LCD}	V_{DD} - V_{LCD}

NOTE: V_{LCD} is the LCD driving voltage, refer to the initial set of the instruction code.

AC Characteristics

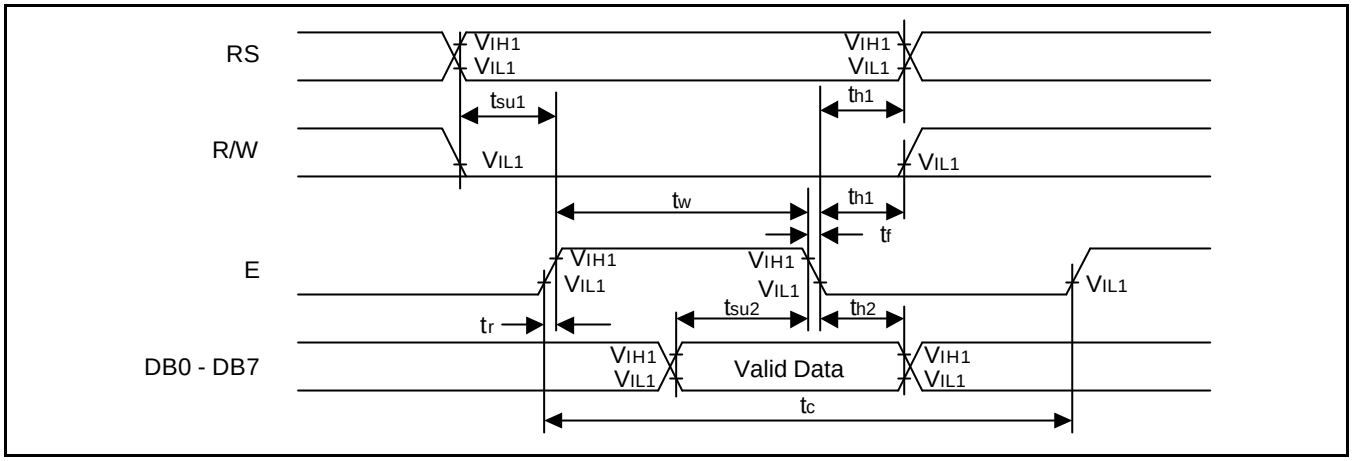
(1) Write Mode (Writing data from MICOM to S6A2068)

(V_{DD} = 4.5V to 5.5V, T_A = -30 to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
E Cycle Time	t_C	500	–	–	ns	E
E Rise Time	t_R	–	–	25	ns	E
E Fall Time	t_F	–	–	25	ns	E
E Pulse Width (High, Low)	t_W	220	–	–	ns	E
R/W and RS Set-Up Time	t_{SU1}	40	–	–	ns	R/W, RS
R/W and RS Hold Time	t_{H1}	10	–	–	ns	R/W, RS
Data Set-Up Time	t_{SU2}	60	–	–	ns	DB0 - DB7
Data Hold Time	t_{H2}	10	–	–	ns	DB0 - DB7

(V_{DD} = 2.7V to 4.5V, T_A = -30 to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
E Cycle Time	t_C	1400	–	–	ns	E
E Rise / Fall Time	t_R	–	–	25	ns	E
E Pulse Width (High, Low)	t_W	400	–	–	ns	E
R/W and RS Set-Up Time	t_{SU1}	60	–	–	ns	R/W, RS
R/W and RS Hold Time	t_{H1}	20	–	–	ns	R/W, RS
Data Set-Up Time	t_{SU2}	140	–	–	ns	DB0 - DB7
Data Hold Time	t_{H2}	10	–	–	ns	DB0 - DB7


RS
R/W
E
DB0 - DB7
VIH1
VIL1
tsu1
th1
tw
tf
tr
tsu2
th2
Valid Data
tc

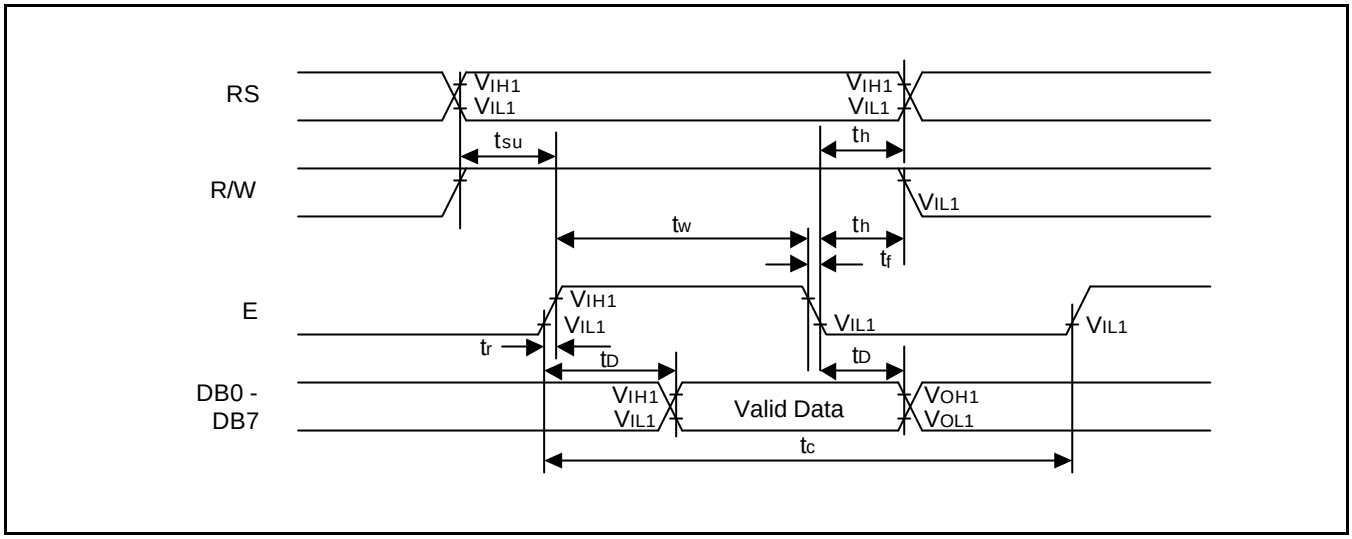
(2) Read Mode (Reading data from S6A2068 to MCU)

(V_{DD} = 4.5V to 5.5V, T_A = -30 to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
E Cycle Time	t_C	500	–	–	ns	E
E Rise Time	t_R	–	–	25	ns	E
E Fall Time	t_F	–	–	25	ns	E
E Pulse Width (High, Low)	t_W	220	–	–	ns	E
R/W and RS Set-Up Time	t_{SU}	40	–	–	ns	R/W, RS
R/W and RS Hold Time	t_H	10	–	–	ns	R/W, RS
Data Output Delay Time	t_D	–	–	120	ns	DB0 to DB7
Data Hold Time	t_{DH}	20	–	–	ns	DB0 to DB7

(V_{DD} = 2.7V to 4.5V, T_A = -30 to +85°C)

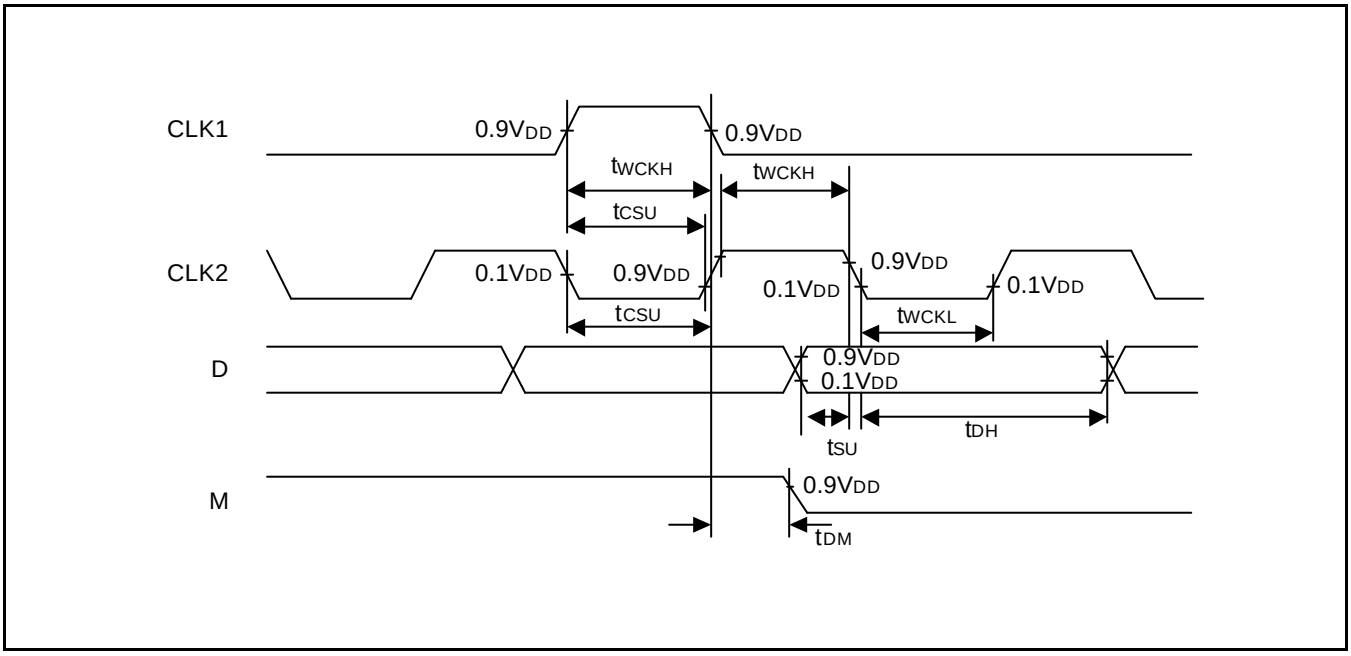
Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
E Cycle Time	t_C	1400	–	–	ns	E
E Rise / Fall Time	t_R	–	–	25	ns	E
E Pulse Width (High, Low)	t_W	400	–	–	ns	E
R/W and RS Set-Up Time	t_{SU}	60	–	–	ns	R/W, RS
R/W and RS Hold Time	t_H	20	–	–	ns	R/W, RS
Data Output Delay Time	t_D	–	–	360	ns	DB0 - DB7
Data Hold Time	t_{DH}	5	–	–	ns	DB0 - DB7


RS
R/W
E
DB0 -
DB7
VIH1
VIL1
tsu
th
tw
tf
tr
tD
VOH1
VOL1
Valid Data
tc

(3) Interface Mode (with S6A0065, S6A2067)

(V_{DD} = 2.7V to 5.5V, T_A = -30 to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
Clock Pulse Width High	t_{WCKH}	800	–	–	ns	CLK
Clock Pulse Width Low	t_{WCKL}	800	–	–	ns	CLK
Data Set-Up Time	t_{SU}	300	–	–	ns	D
Data Hold Time	t_{DH}	300	–	–	ns	D
Clock Set-Up Time	t_{CSU}	500	–	–	ns	CLK
M Delay Time	t_{DM}	-1000	–	1000	ns	M



CONTROL AND DISPLAY COMMAND

Command	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB4	DB1	DB0	Execution Time (f_{OSC}=250kHz)	Remark
Clear Display	0	0	0	0	0	0	0	0	0	1	1.64ms	
Return Home	0	0	0	0	0	0	0	0	1	X	1.64ms	cursor move to first digit
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	40µs	• I/D; set cursor move direction H: Increase L: Decrease • SH: Specifies shift of display H: Display is shifted L: Display is not shifted
Display On/Off	0	0	0	0	0	0	1	D	C	B	40µs	• Display: D H: Display ON L: Display OFF • Cursor: C H: Cursor ON L: Cursor OFF • Blinking: B H: Blinking ON L: Blinking OFF
Shift	0	0	0	0	0	1	S/C	R/L	X	X	40µs	• SC H: Display shift L: Cursor move • R/L H: Right shift L: Left shift
Set Function	0	0	0	0	1	DL	N	F	X	X	40µs	• DL H: 8-bit interface L: 4-bit interface • N H: 2 line display L: 1 line display • F H: 5 x 10 dots L: 5 x 7 dots

.

CONTROL AND DISPLAY COMMAND (CONTINUED)

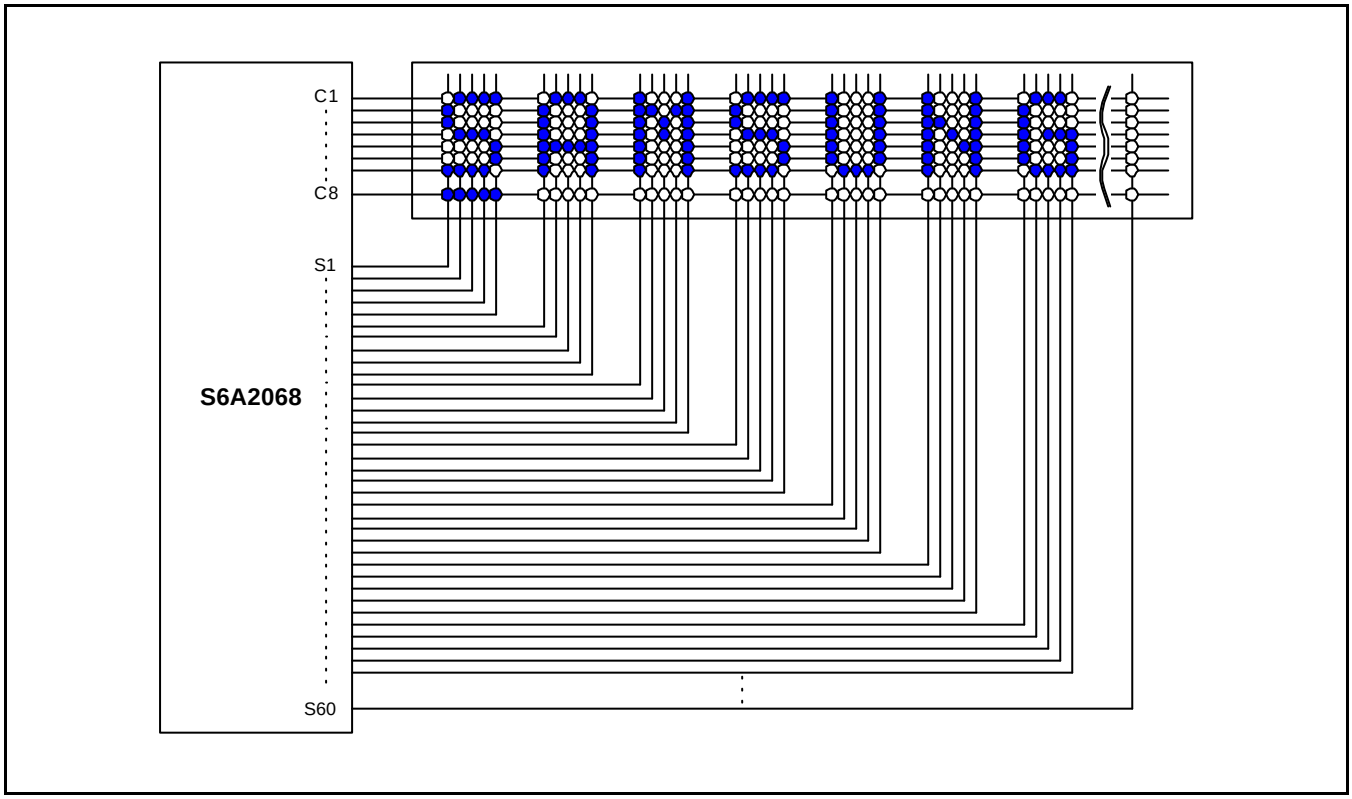
Command	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Execution Time (f_{OSC}=250kHz)	Remark
Set CG RAM Address	0	0	0	1	CG RAM address (corresponds to cursor address)						40µs	CG RAM Data is sent and received after this setting
Set DD RAM Address	0	0	1	DD RAM address							40µs	DD RAM Data is sent and received after this setting
Read Busy Flag & Address	0	1	BF	Address Counter used for Both DD & CD RAM address							0µs	BF H: Busy L: Ready - Reads BF indication internal operating is being performed. - Reads address counter contents
Write Data	1	0	Write Data								46µs	Write data into DD or CGRAM
Read Data	1	1	Read Data								46µs	Read data from DD or CGRAM

NOTES:

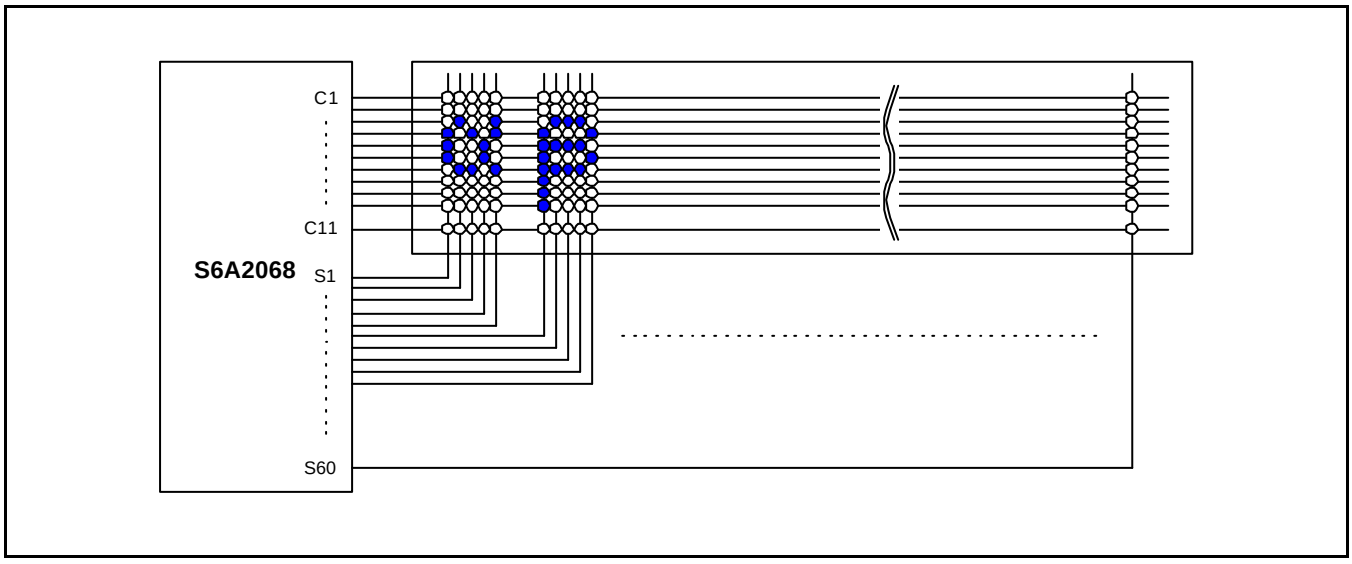
1. When a MPU program with Busy Flag (DB7) checking is made, 1/2 f_{OSC} (is necessary) for executing the next instruction by the "E" signal after the Busy Flag (DB7) goes to "Low".
2. "x" is don't care.

APPLICATION INFORMATION ACCORDING TO LCD PANEL

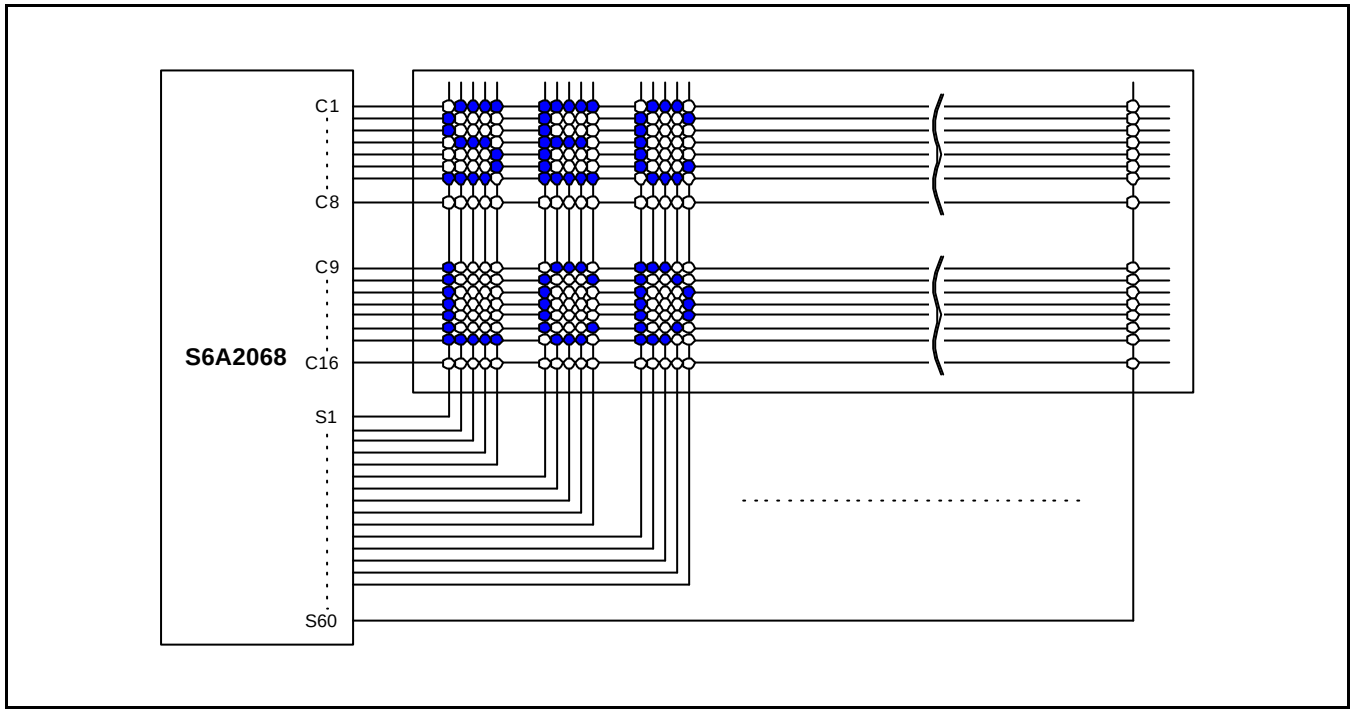
1) LCD Panel: 12 character ´ 1-line, Character Format; 5 ´ 7 dots + 1-cursor line (1/4 bias, 1/8 duty)



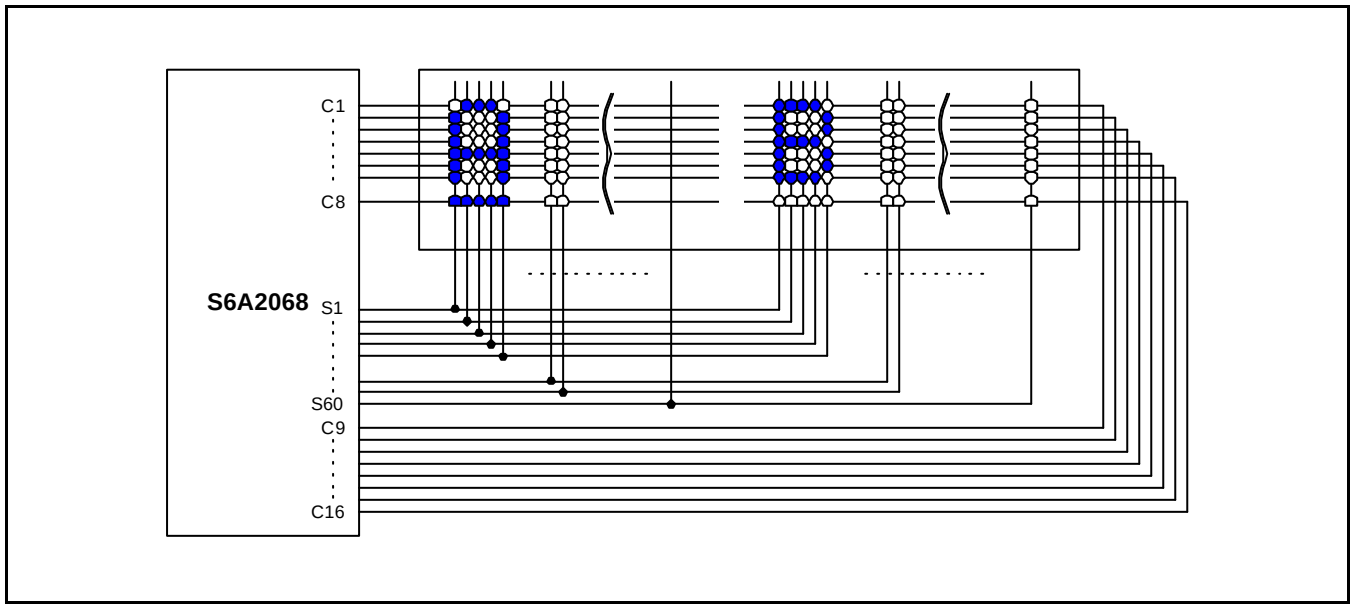
2) LCD Panel: 12 character ´ 1-line, Character Format; 5 ´ 10 dots + 1-cursor line (1/4 bias, 1/11 duty)



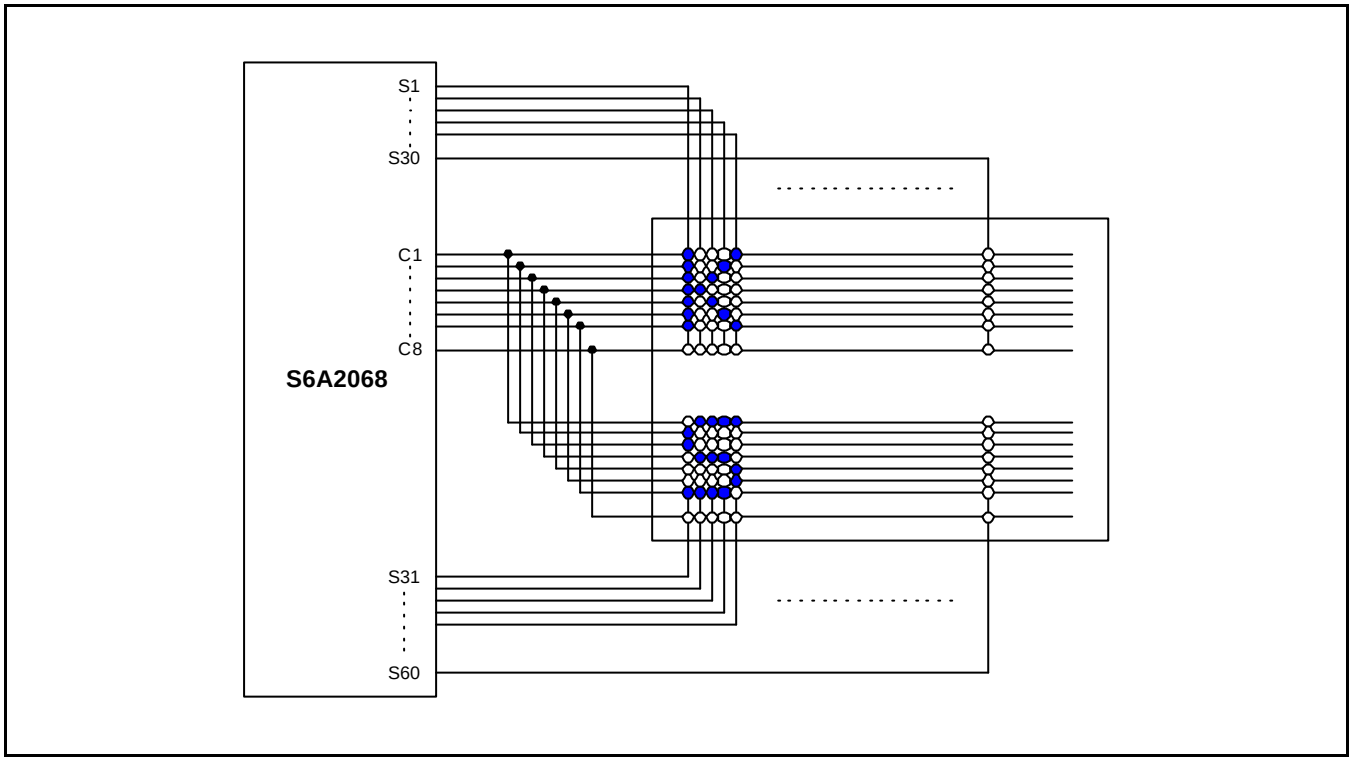
3) LCD Panel : 12 character ´ 2-line Character Format; 5 ´ 7 dots + 1-cursor line (1/5 bias, 1/16 duty)



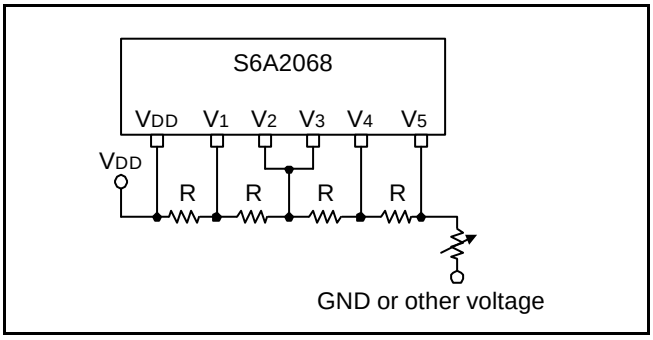
4) LCD Panel: 24 character´ 1-line, Character Format; 5´ 7 dots + 1 dot + 1-cursor line (1/5 bias, 1/16 duty)



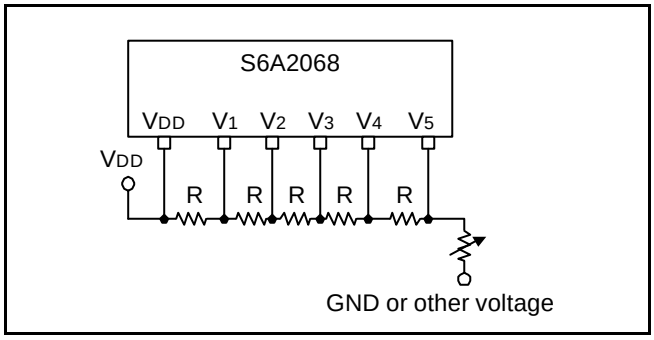
5) LCD Panel: 6 character x 2-line Character Format; 5 x 7 dots + 1-cursor line (1/4 bias, 1/8 duty)



BIAS VOLTAGE DIVIDE CIRCUIT

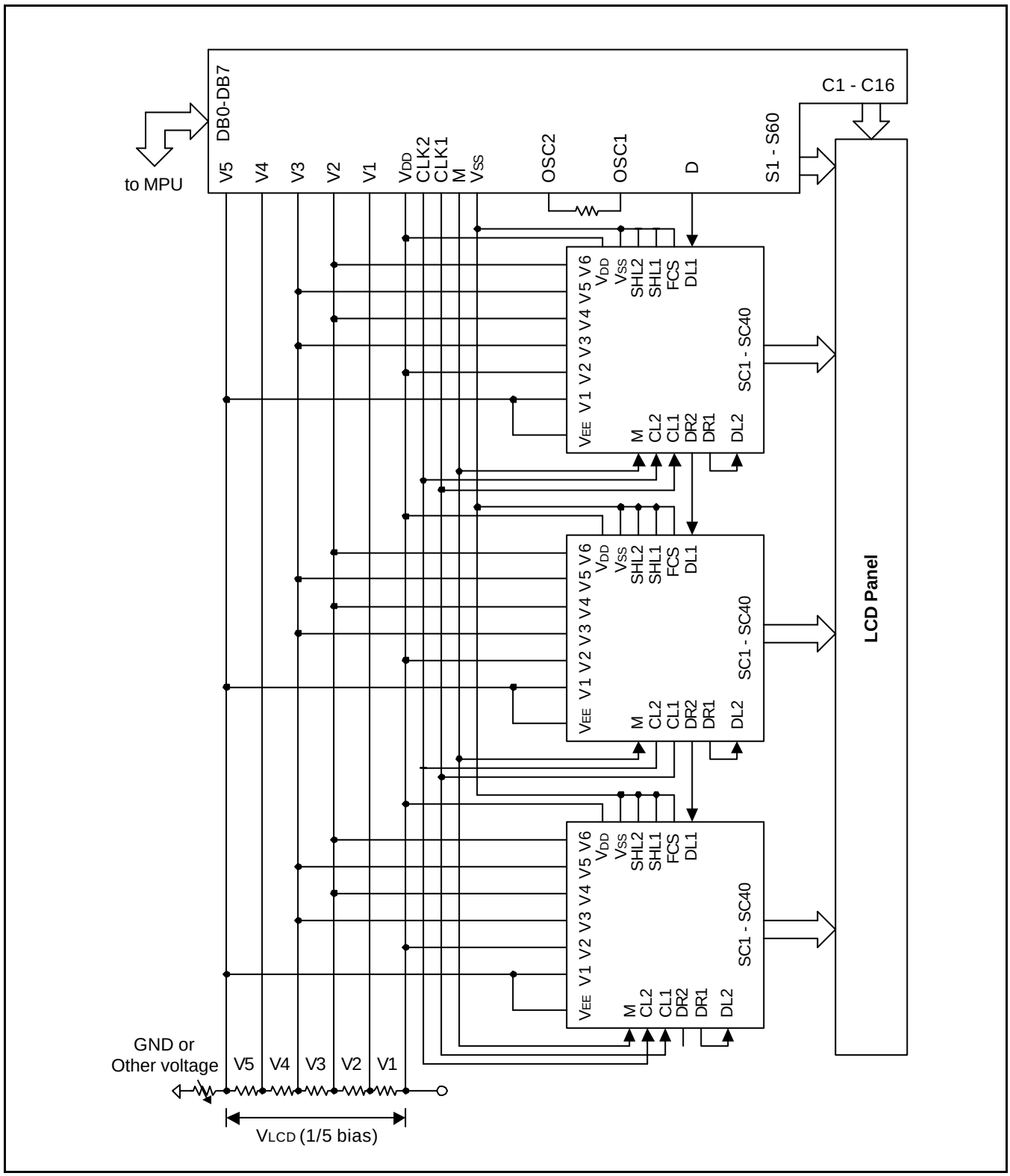


(1/4 bias, 1/8 or 1/11 duty)



(1/5 bias, 1/16 duty)

APPLICATION CIRCUIT



When S6A0065 is externally connected to the S6A2068, you can increase the number of display digits up to 80 characters.