LH64256B

CMOS 1M (256K × 4) Dynamic RAM

FUNCTION

- 262,144 words × 4 bit
- Access times: 70/80 ns (MAX)
- Cycle time: 130/160 ns (MIN)
- Fast page mode cycle time:
  50/55 ns (MIN)
- Single +5 V power supply
- Power consumption (MAX):
  Operating: 467.5/385 mW
  Standby: 11 mW
- Built-in latch circuit for row-address, column-address, and input data
- $\overline{OE}$ = don't care in early write operation
- $\overline{RAS}$ only refresh, hidden refresh, and $\overline{CAS}$ before $\overline{RAS}$ refresh capability
- On-chip refresh counter
- 512 refresh cycle/8 ms
- Packages:
  20-pin, 300-mil DIP
  26-pin, 300-mil SOJ
  20-pin, 400-mil ZIP

DESCRIPTION

The LH64256B is a 262,144 word × 4-bit dynamic RAM which allows fast page mode access. The LH64256B is fabricated on SHARP's advanced CMOS double-level polysilicon gate technology. With its input multiplexed and packaged in the standard 20-pin DIP, 26-pin SOJ, or 20-pin ZIP packages, it is easy to realize memory systems with low power dissipation and large memory capacity. The LH64256B operates on a single +5 V power supply and the built-in biasing voltage generator circuit.

PIN CONNECTIONS

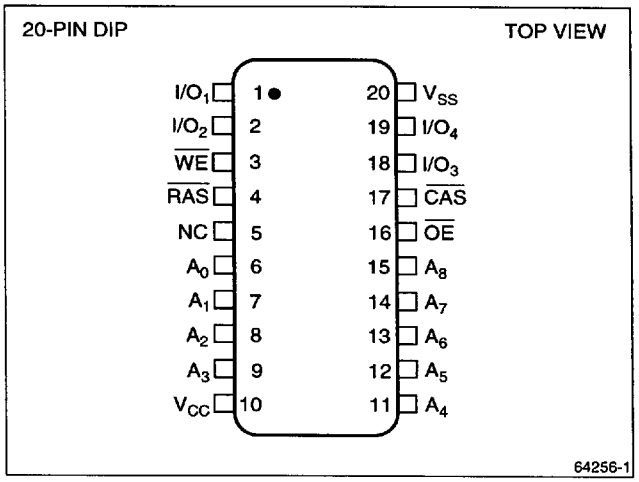


Figure 1. Pin Connections for DIP Package

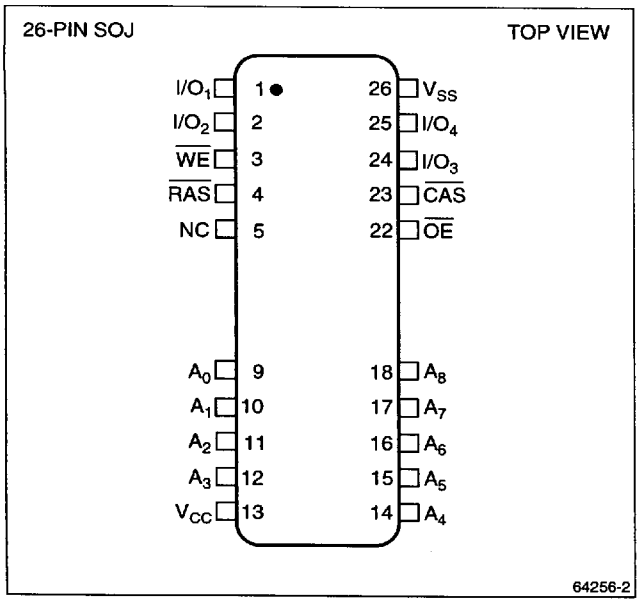


Figure 2. Pin Connections for SOJ Package

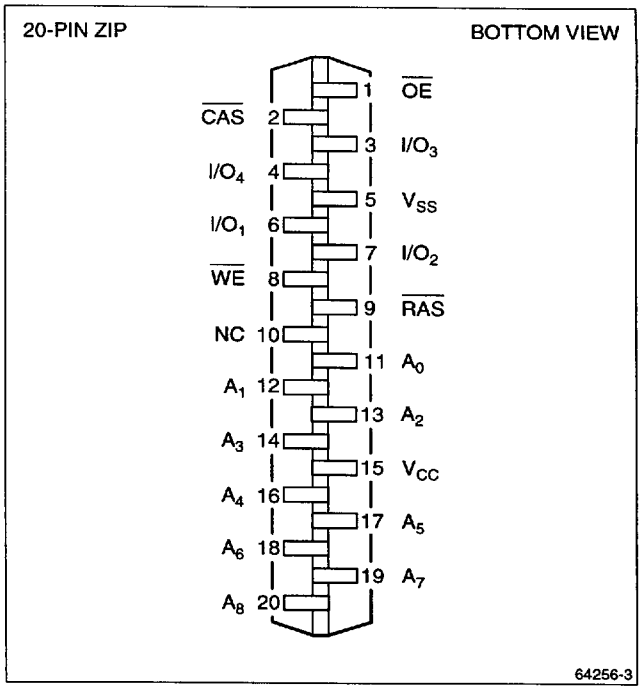


Figure 3. Pin Connections for ZIP Package

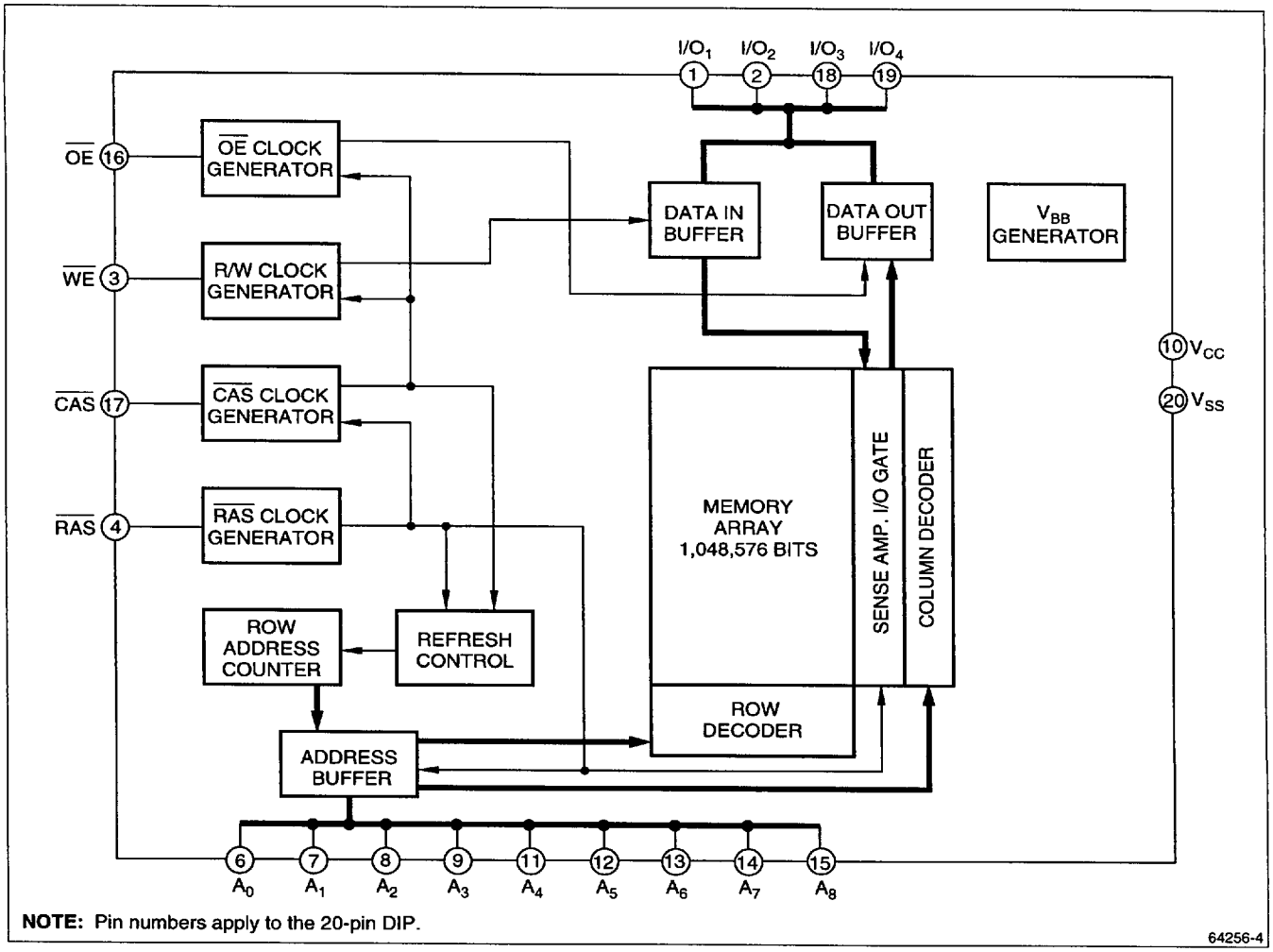


Figure 4. LH64256B Block Diagram

PIN DESCRIPTION

PIN NAME	FUNCTION
$A_0 - A_8$	Address input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable

PIN NAME	FUNCTION
$I/O_1 - I/O_4$	Data input/output
V_{CC}	Power supply (+5 V)
V_{SS}	Power supply (0 V)
NC	No connection

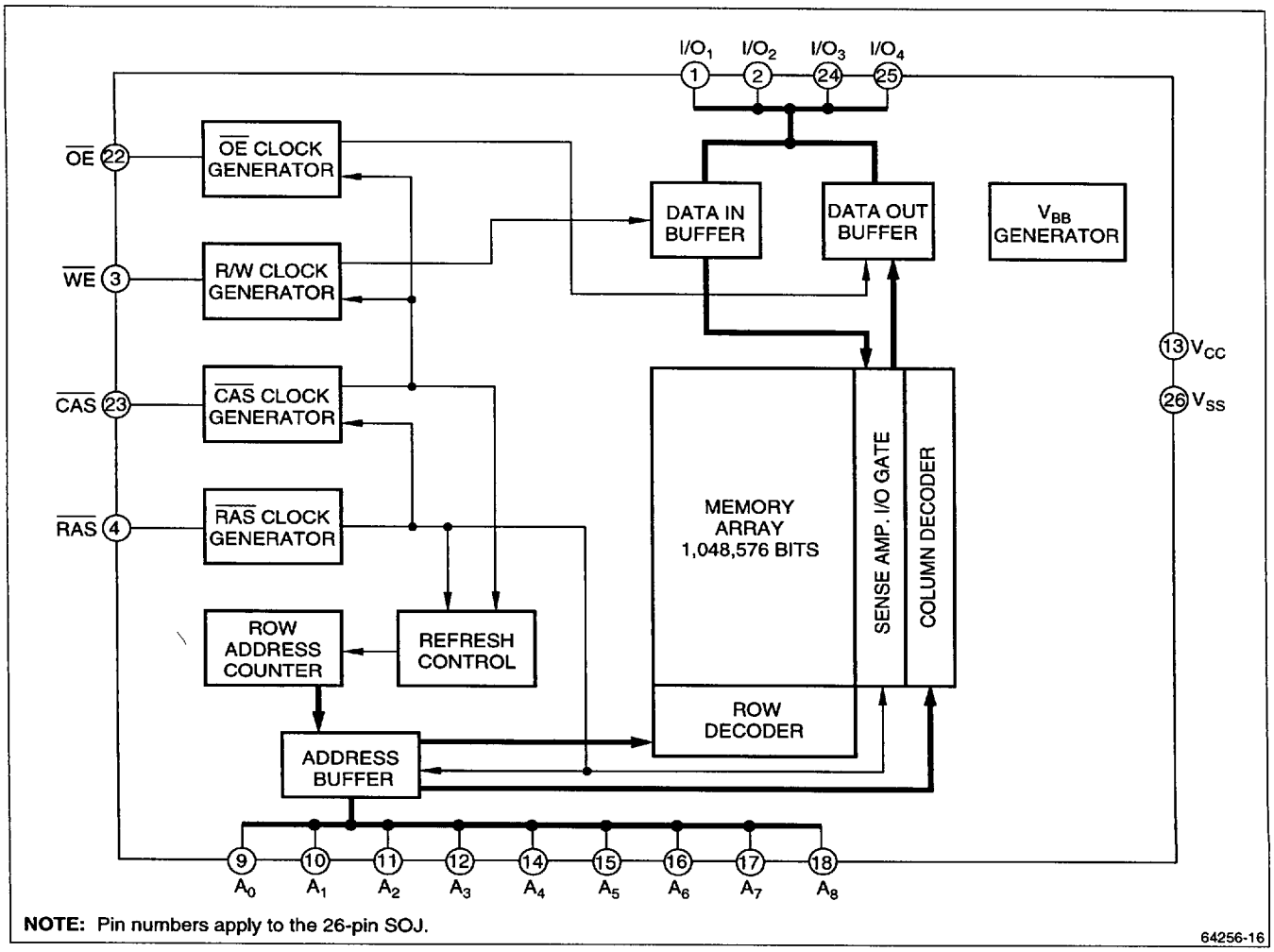


Figure 5. LH64256B Block Diagram

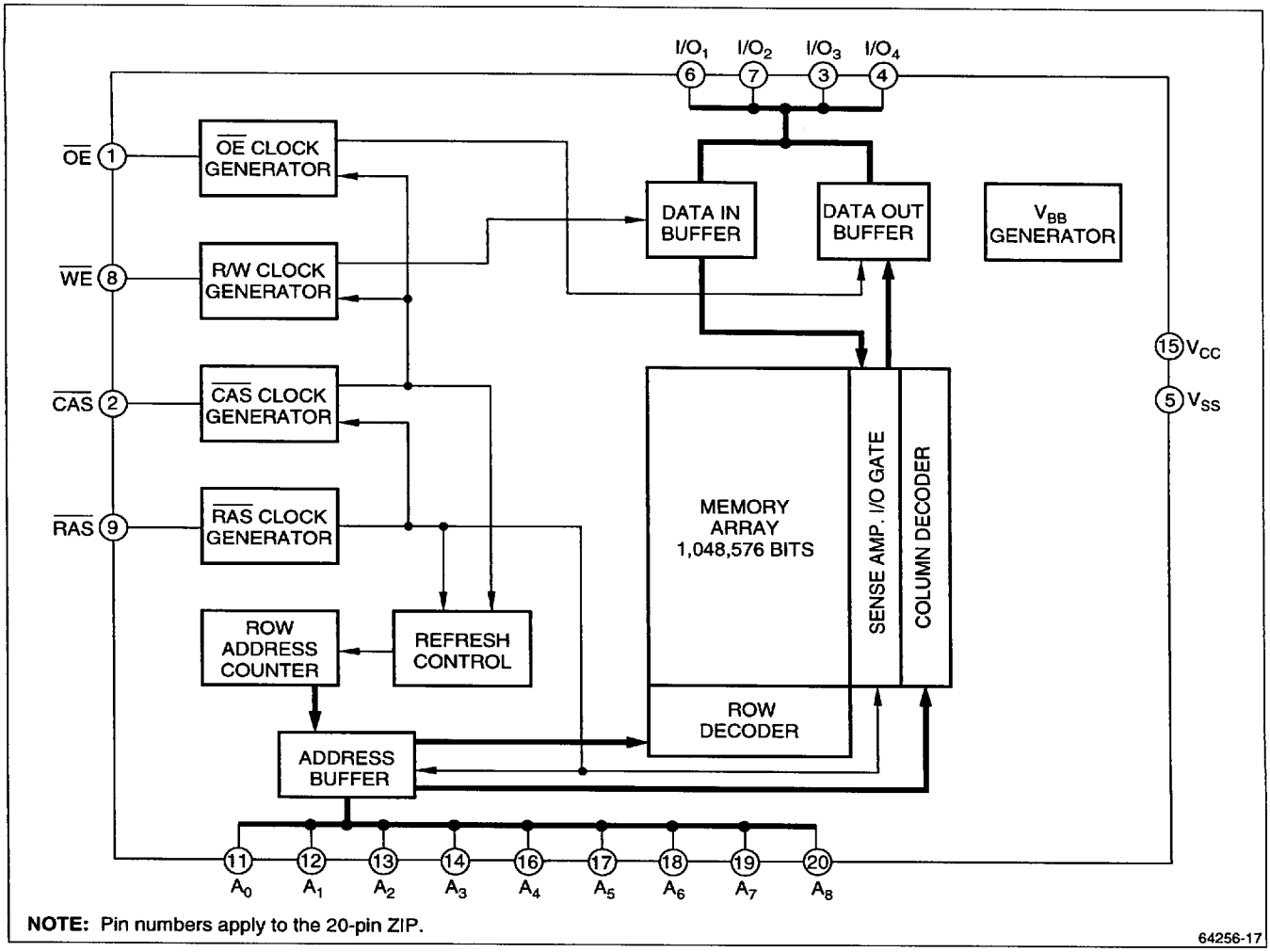


Figure 6. LH64256B Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	NOTE
Applied voltage on all pins	−1.0 to +7.0	V	1
Output short circuit current	50	mA	
Power dissipation	600	mW	
Operating temperature	0 to +70	°C	
Storage temperature	−65 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to V_{SS}.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.8		V_{CC} + 0.3	V
	V_{IL}	−0.3		0.6	V

CAPACITANCE (T_A = 0 to +70°C, f = 1 MHz, V_{CC} = 5.0 V ±10%)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_0 to A_8	C_{IN1}		6	pF
	$\overline{RAS}$, $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}		7	pF
Input/output capacitance	I/O_1 to I/O_4	C_{OUT1}		7	pF

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5.0 V ±10%)

PARAMETER	CONDITIONS	SYMBOL	−70 ns		−80 ns		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
Average supply current in normal operation		I_{CC1}		85		70	mA	1, 2, 3
Supply current in standby mode	MOS: $\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V	I_{CC2}		1		1	mA	1
	TTL: $\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	I_{CC2}		2		2	mA	1
Average supply current in fast page mode		I_{CC3}		65		55	mA	1, 2
Average supply current in $\overline{CAS}$ before $\overline{RAS}$ refresh cycle		I_{CC4}		85		65	mA	1, 2, 3
Average supply current in $\overline{RAS}$ only refresh cycle		I_{CC5}		85		65	mA	1, 2, 3
Input leakage current	0 V ≤ V_{IN} ≤ 6.5 V 0 V except on test pins	I_{LI}	−10	10	−10	10	µA	
Output leakage current	0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V Output in high-impedance state	I_{LO}	−10	10	−10	10	µA	
Output 'High' Voltage	I_{OUT} = −5.0 mA	V_{OH}	2.4		2.4		V	
Output 'Low' Voltage	I_{OUT} = 4.2 mA	V_{OL}		0.4		0.4	V	

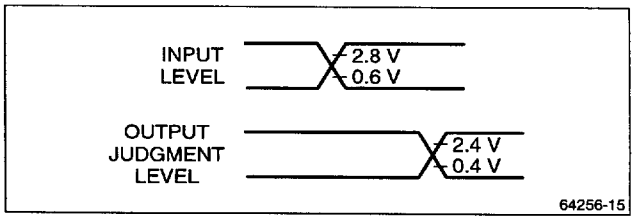
NOTES:
1. Specified values are with outputs open.
2. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on cycle time.
3. t_{RC} = t_{RC} (MIN.). Address transition is once at $\overline{RAS}$ = V_{IH} and once at $\overline{RAS}$ = V_{IL}.

AC ELECTRICAL CHARACTERISTICS [1, 2, 3, 4] (t_A = 0 to +70°C, V_{CC} = 5.0 V ±10%)

PARAMETER	SYMBOL	-70		-80		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Random read or write cycle time	t_{RC}	130		160		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80	ns	5
Access time from column address	t_{AA}		35		40	ns	5
Access time from $\overline{CAS}$	t_{CAC}		25		25	ns	5
Access time from $\overline{OE}$	t_{OEA}		20		25	ns	5
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		12		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time ($\overline{RAS}$)	t_{CAH}	15		20		ns	
Column address delay time ($\overline{RAS}$)	t_{RAD}	15	35	17	40	ns	6
Column address lead time ($\overline{RAS}$)	t_{RAL}	35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	ns	
$\overline{RAS}$ precharge time	t_{RP}	50		70		ns	
$\overline{CAS}$ precharge time ($\overline{RAS}$ ↓)	t_{CRP}	10		10		ns	
$\overline{CAS}$ delay time ($\overline{RAS}$)	t_{RCD}	20	45	22	55	ns	7
$\overline{CAS}$ lead time ($\overline{RAS}$)	t_{RSL}	25		25		ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	25	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		ns	
$\overline{OE}$ lead time ($\overline{RAS}$)	t_{ROL}	0		0		ns	
Output data disable time ($\overline{CAS}$)	t_{OFF}		20		20	ns	
Output data disable time ($\overline{OE}$)	t_{OEZ}		20		20	ns	
Output data hold time ($\overline{CAS}$)	t_{SOH}	0		0		ns	
Output data hold time ($\overline{OE}$)	t_{OOH}	0		0		ns	
Read command setup time ($\overline{CAS}$)	t_{RCS}	0		0		ns	
Read command hold time ($\overline{CAS}$)	t_{RCH}	0		0		ns	8
Read command hold time ($\overline{RAS}$ ↑)	t_{RRH}	10		10		ns	8
Transition time (rise and fall)	t_T	3	50	3	35	ns	
Refresh time interval	t_{REF}		8		8	ms	

NOTES:

1. For proper memory function, at least 200 µs of pause time should be kept after power on, followed by several dummy cycles. When $\overline{RAS}$ = V_{IH} is continued for more than 8 ms, the same dummy cycles should be given. Usually eight ordinary refresh cycles should be given.
2. The required V_{CC} current (I_{CC}) during power on depends on the input levels of $\overline{RAS}$. If $\overline{RAS}$ = V_{IL} during power on, the device goes into an active cycle, and I_{CC} exhibits large current transients. It is recommended that $\overline{RAS}$ tracks with V_{CC} or be held at a valid V_{IH} during power on.
3. AC characteristics assume t_T = 5 ns.
4. AC characteristics assume the following condition (see figure at right).
5. Load condition for 2TTL + 100 pF.
6. t_{RAD} (MAX) is the maximum point for t_{RAD} where t_{RAC} (MAX) is ensured, and does not represent a limit of operation. If $t_{RAD} \geq t_{RAD}$ (MAX), the access time comes under the control of t_{AA}.
7. t_{RCD} (MAX) is the maximum point for t_{RCD} where t_{RAC} (MAX) is ensured, and does not represent a limit of operation. If $t_{RCD} \geq t_{RCD}$ (MAX), the access time comes under the control of t_{CAC}.
8. The operation is ensured when either t_{RRH} or t_{RCH} is satisfied.



FAST PAGE MODE CYCLE

PARAMETER	SYMBOL	–70 ns		–80 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t_{PC}	50		55		ns	
$\overline{CAS}$ precharge time	t_{CP}	10		10		ns	
$\overline{CAS}$ precharge access time	t_{CACP}		45		50	ns	
Read-write cycle time (page mode)	t_{PRWC}	100		110		ns	1

NOTE:

1. t_{RWC}, t_{RWD}, t_{AWD}, t_{CWD}, and t_{PRWC} are not restrictive operating parameters and does not represent a limit of operation.

WRITE CYCLE

PARAMETER	SYMBOL	–70 ns		–80 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
EARLY WRITE							
Write command setup time ($\overline{CAS}$)	t_{WCS}	0		0		ns	1
Write command hold time ($\overline{CAS}$)	t_{WCH}	15		20		ns	
Data input setup time	t_{DS}	0		0		ns	
Data input hold time	t_{DH}	15		20		ns	
OE CONTROLLED							
$\overline{CAS}$ setup time	t_{CWS}	0		0		ns	1
Write command lead time ($\overline{RAS}$)	t_{RWL}	20		25		ns	
Write command lead time ($\overline{CAS}$)	t_{CWL}	20		25		ns	
Write pulse width ($\overline{WE}$)	t_{WP}	10		15		ns	
$\overline{OE}$ hold time ($\overline{WE}$)	t_{OEH}	20		25		ns	

NOTE:

1. t_{WCS} and t_{CWS} are not restrictive operating parameters. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and data out buffers remain inactive until $\overline{CAS}$ rises again.

READ-WRITE CYCLE/READ-MODIFY-WRITE CYCLE

PARAMETER	SYMBOL	–70 ns		–80 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read-write cycle time	t_{RWC}	180		220		ns	1
$\overline{WE}$ delay time ($\overline{RAS}$)	t_{RWD}	95		110		ns	1
Column address delay time ($\overline{WE}$)	t_{AWD}	60		70		ns	1
$\overline{WE}$ delay time ($\overline{CAS}$)	t_{CWD}	45		55		ns	1
$\overline{OE}$ delay time	t_{OED}	20		20		ns	

NOTE:

1. t_{RWC}, t_{RWD}, t_{AWD}, t_{CWD}, and t_{PRWC} are not restrictive operating parameters and does not represent a limit of operation.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE/HIDDEN REFRESH CYCLE

PARAMETER	SYMBOL	–70 ns		–80 ns		UNIT
		MIN.	MAX.	MIN.	MAX.	
$\overline{CAS}$ setup time ($\overline{RAS}$)	t_{CSR}	10		10		ns
$\overline{CAS}$ hold time ($\overline{RAS}$)	t_{CHR}	15		20		ns
$\overline{RAS}$ • $\overline{CAS}$ precharge time ($\overline{RAS}$ ↑)	t_{RPCP}	10		10		ns
$\overline{WE}$ precharge time ($\overline{RAS}$)	t_{WRP}	0		0		ns

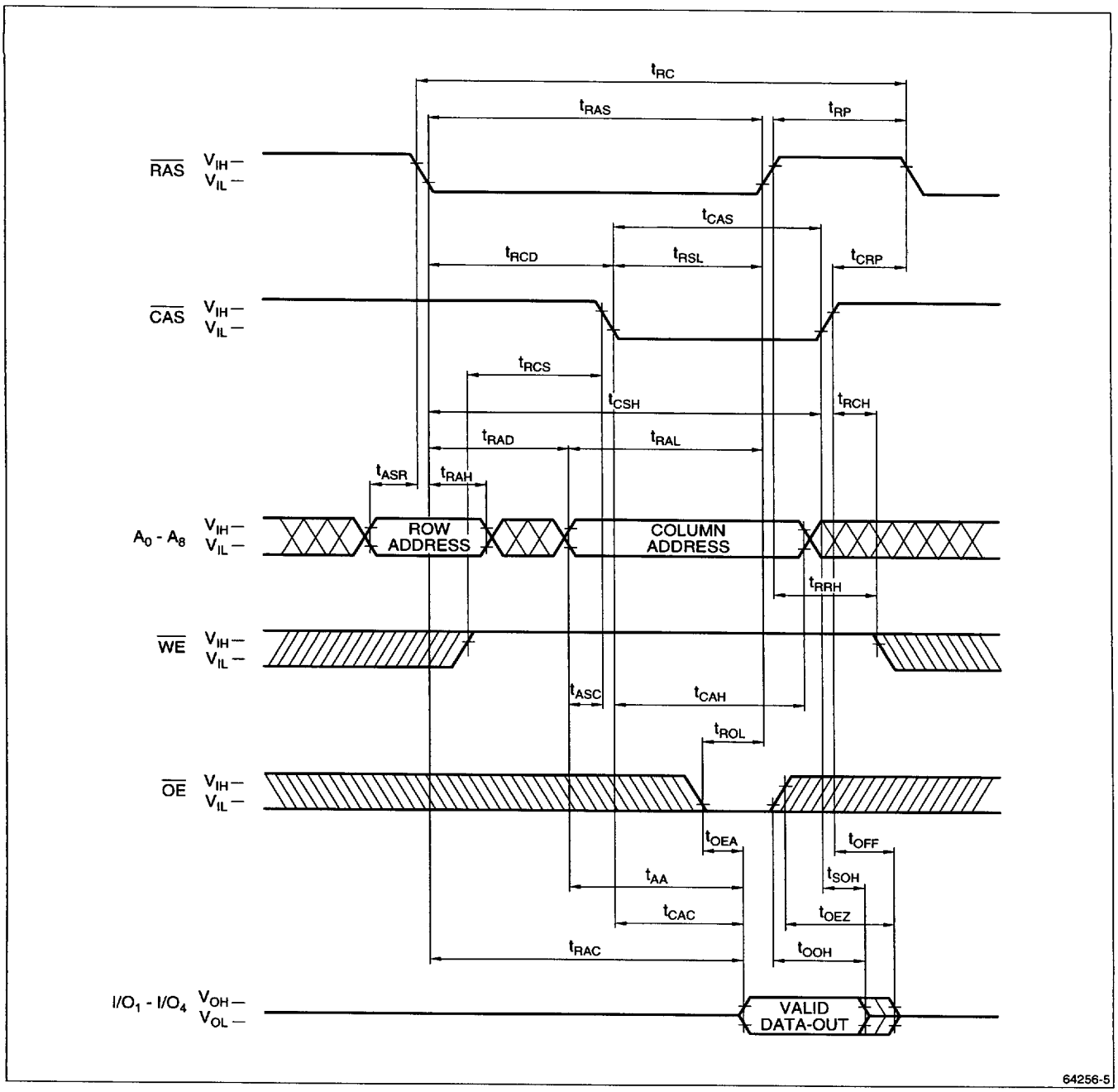


Figure 7. Read Cycle

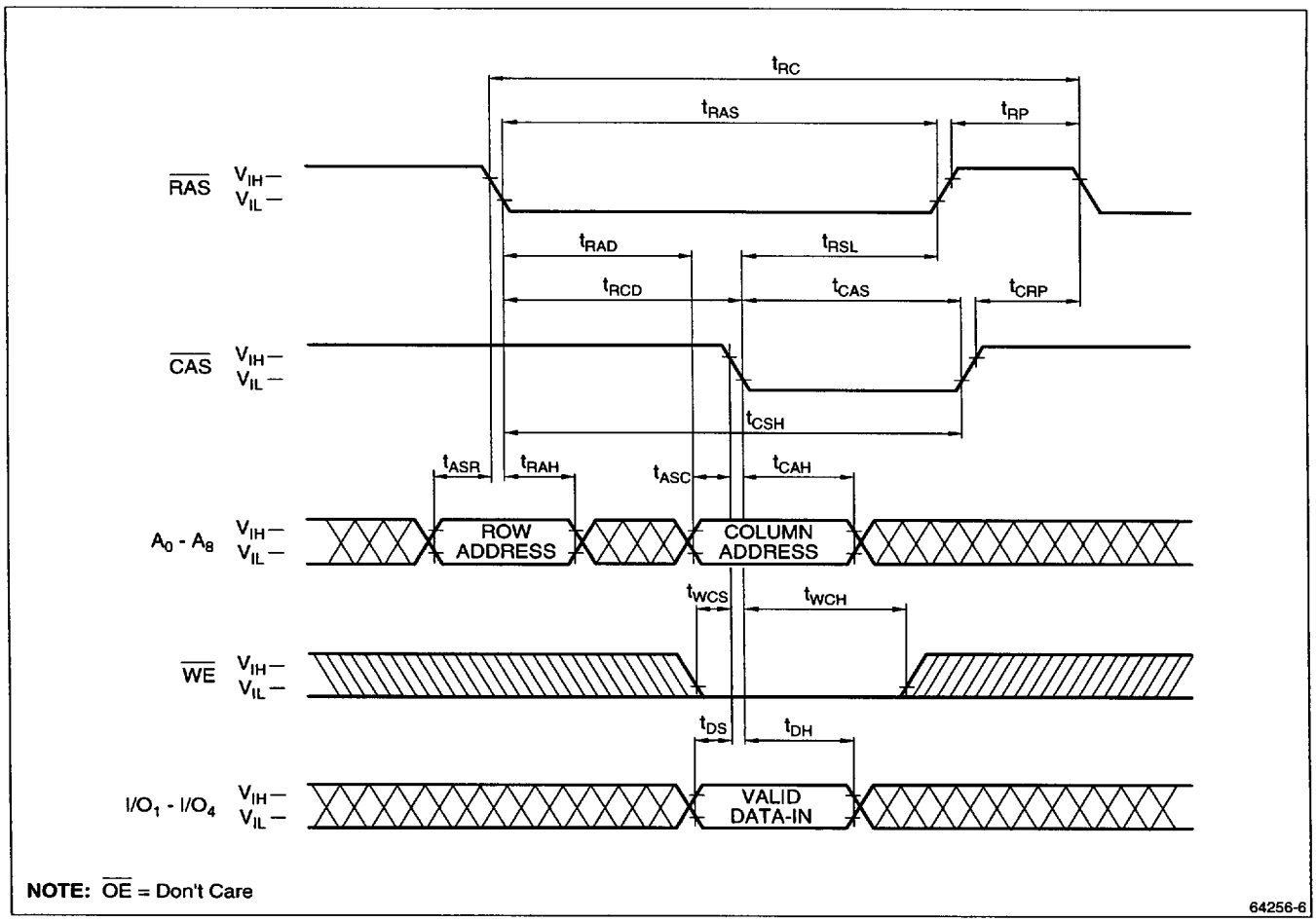


Figure 8. Write Cycle (Early Write)

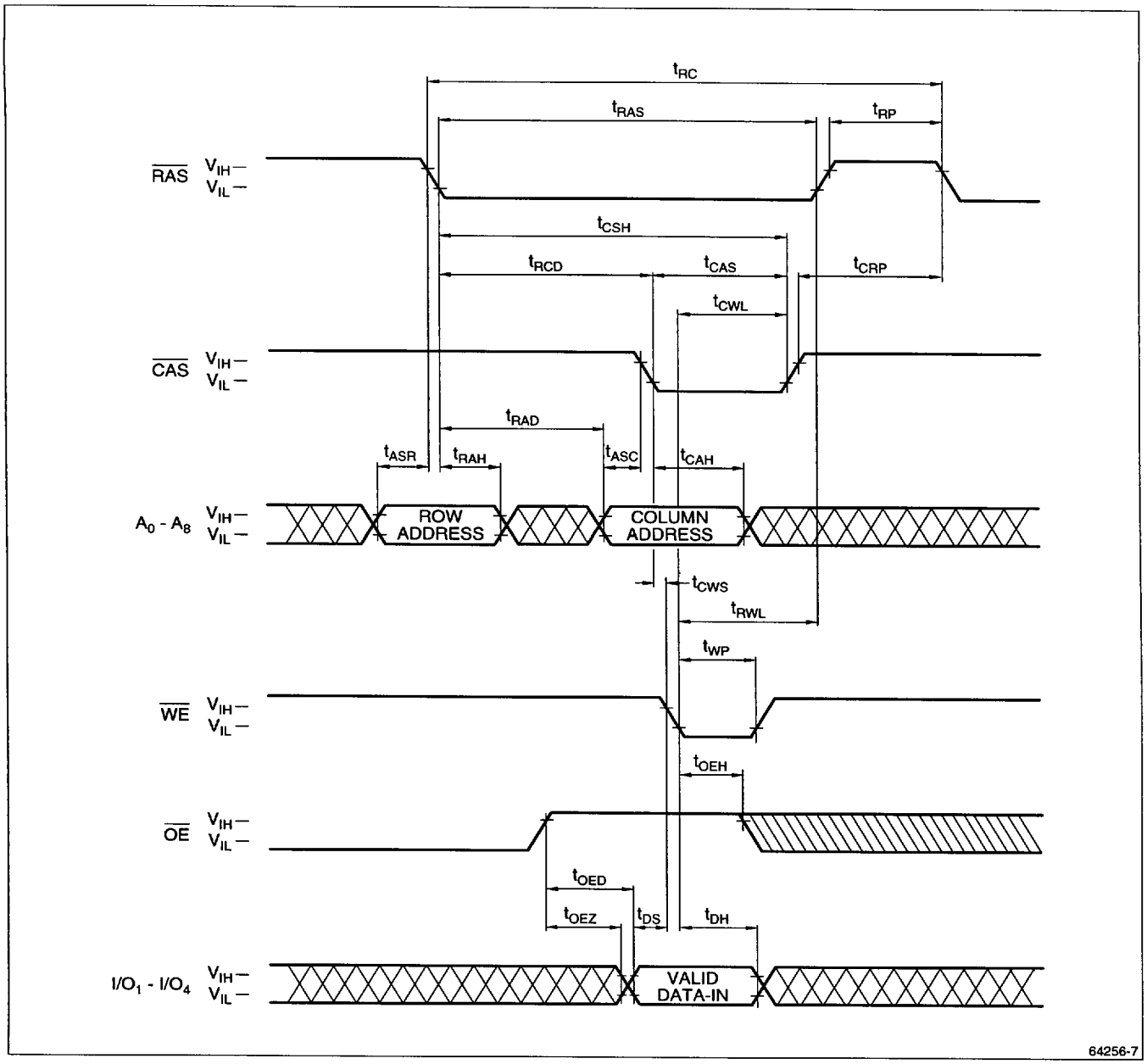


Figure 9. Write Cycle ($\overline{OE}$ Controlled Write)

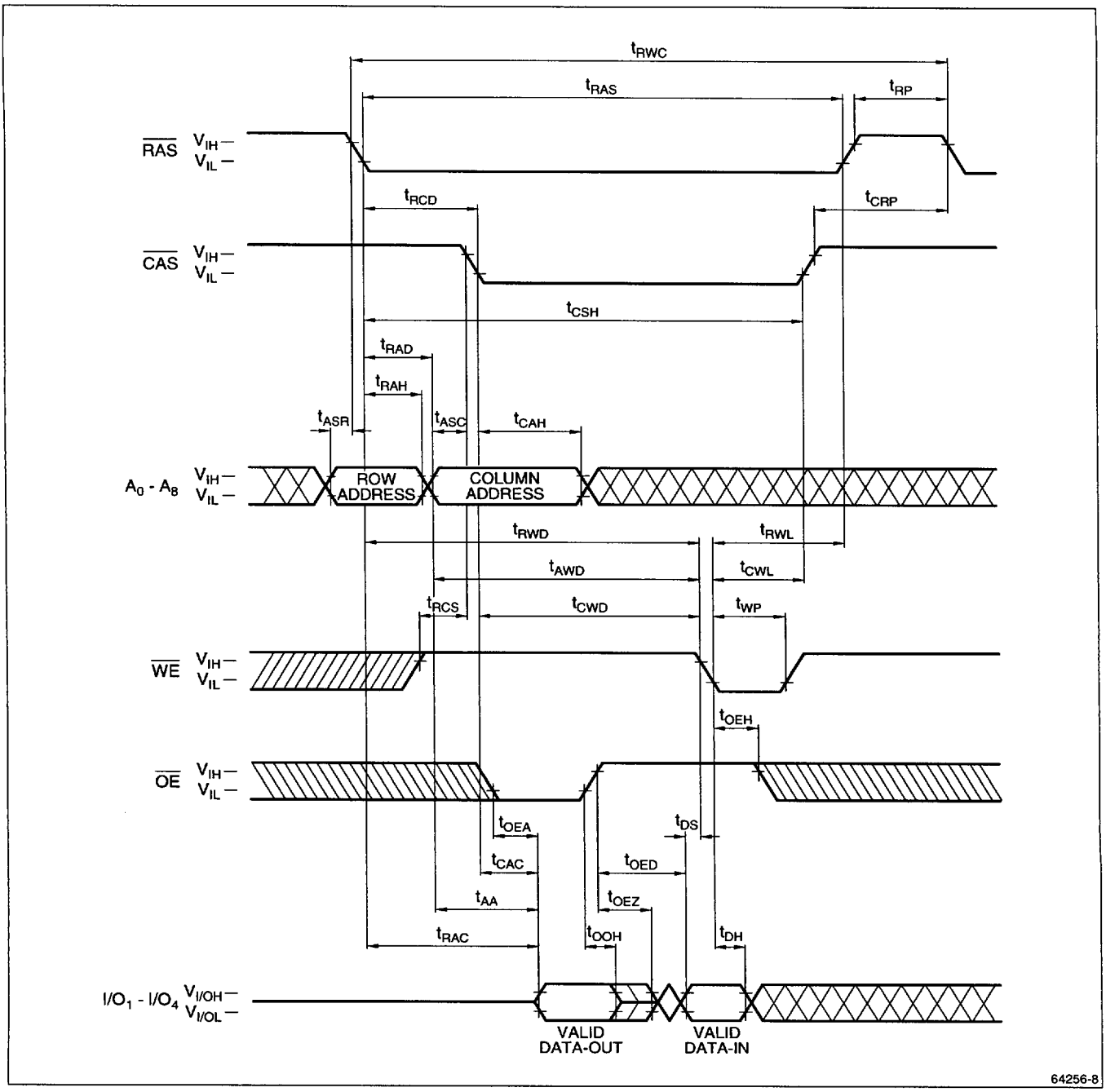


Figure 10. Read/Write Cycle

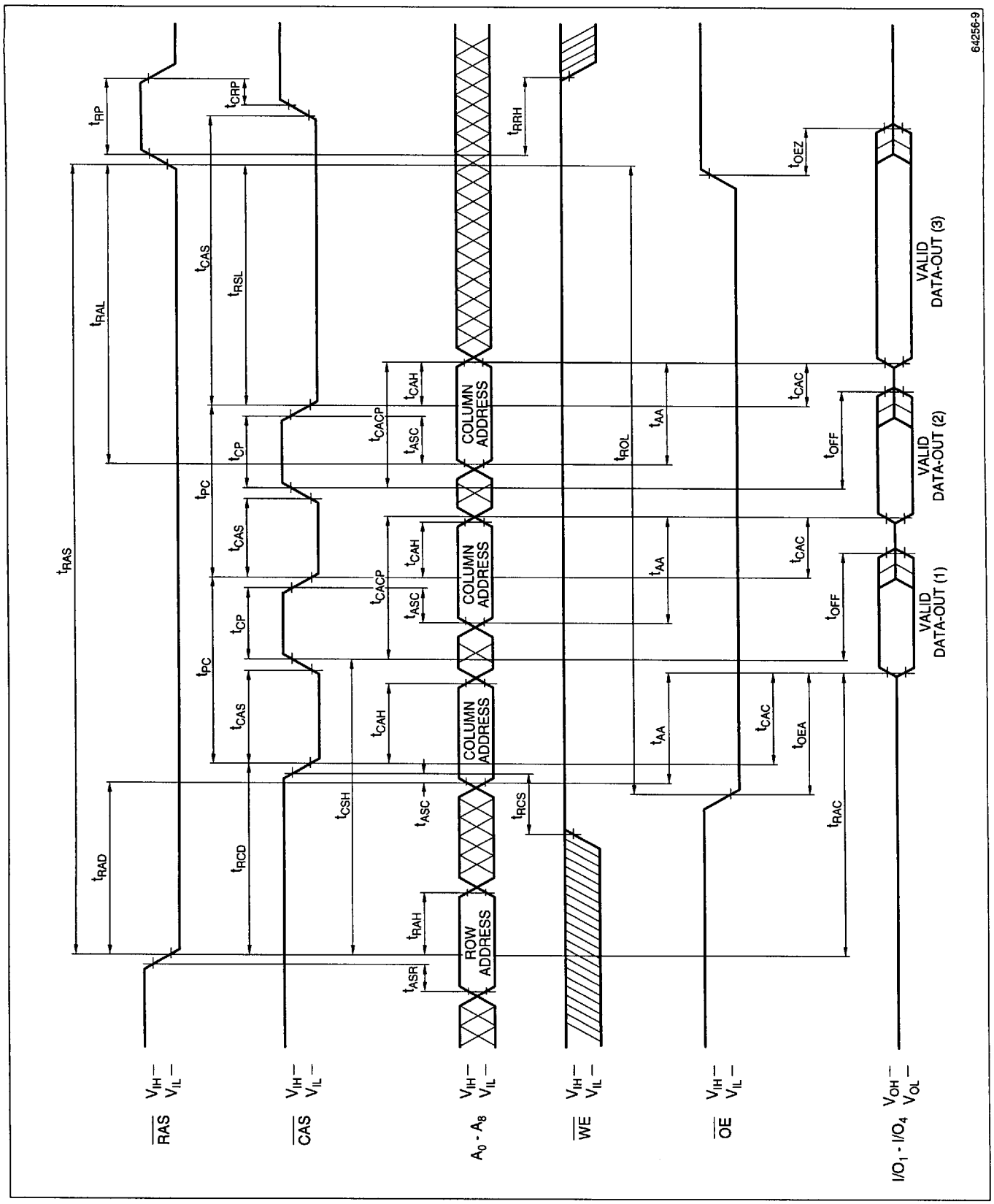


Figure 11. Fast Page Mode Read Cycle

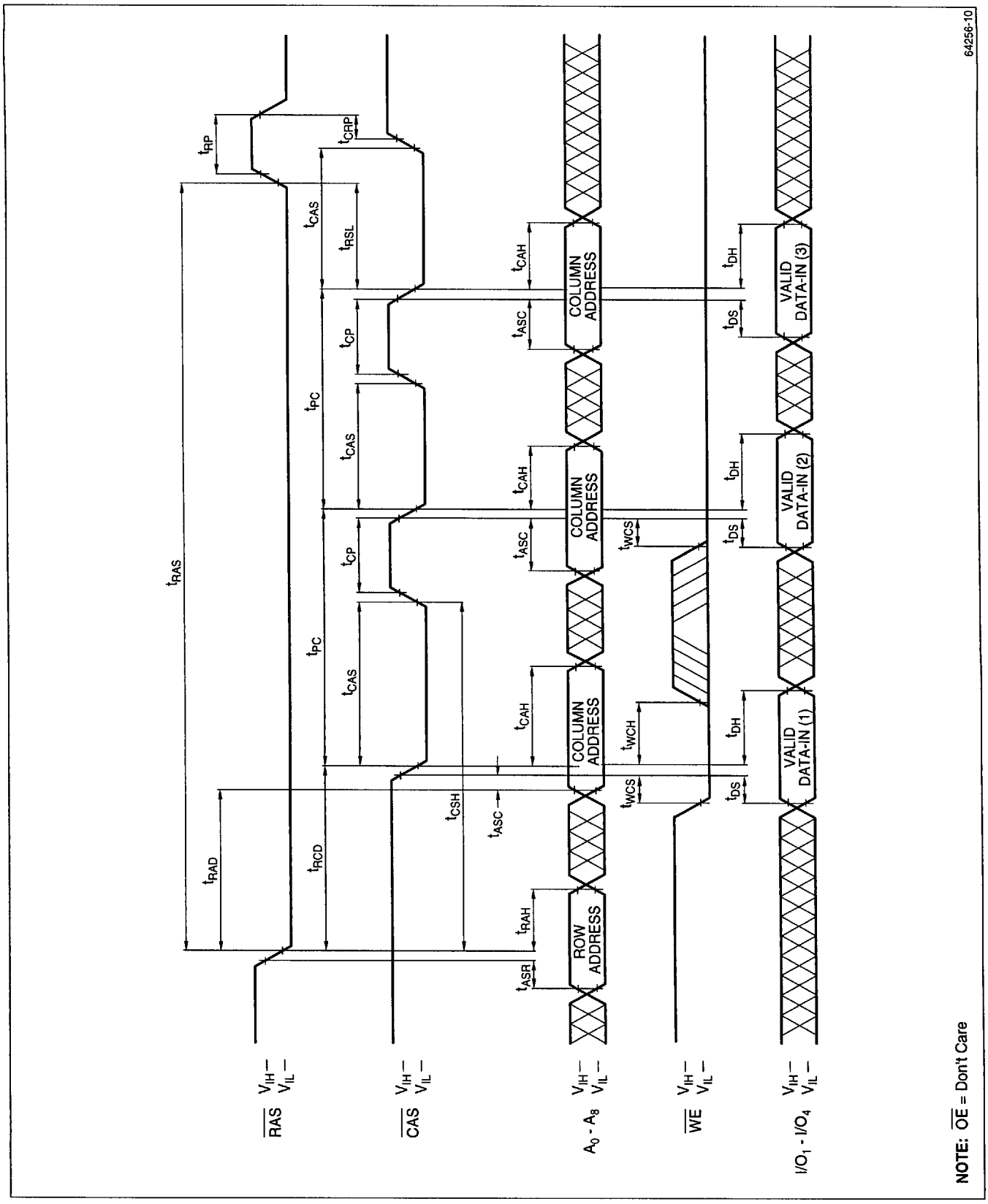


Figure 12. Fast Page Mode Write Cycle

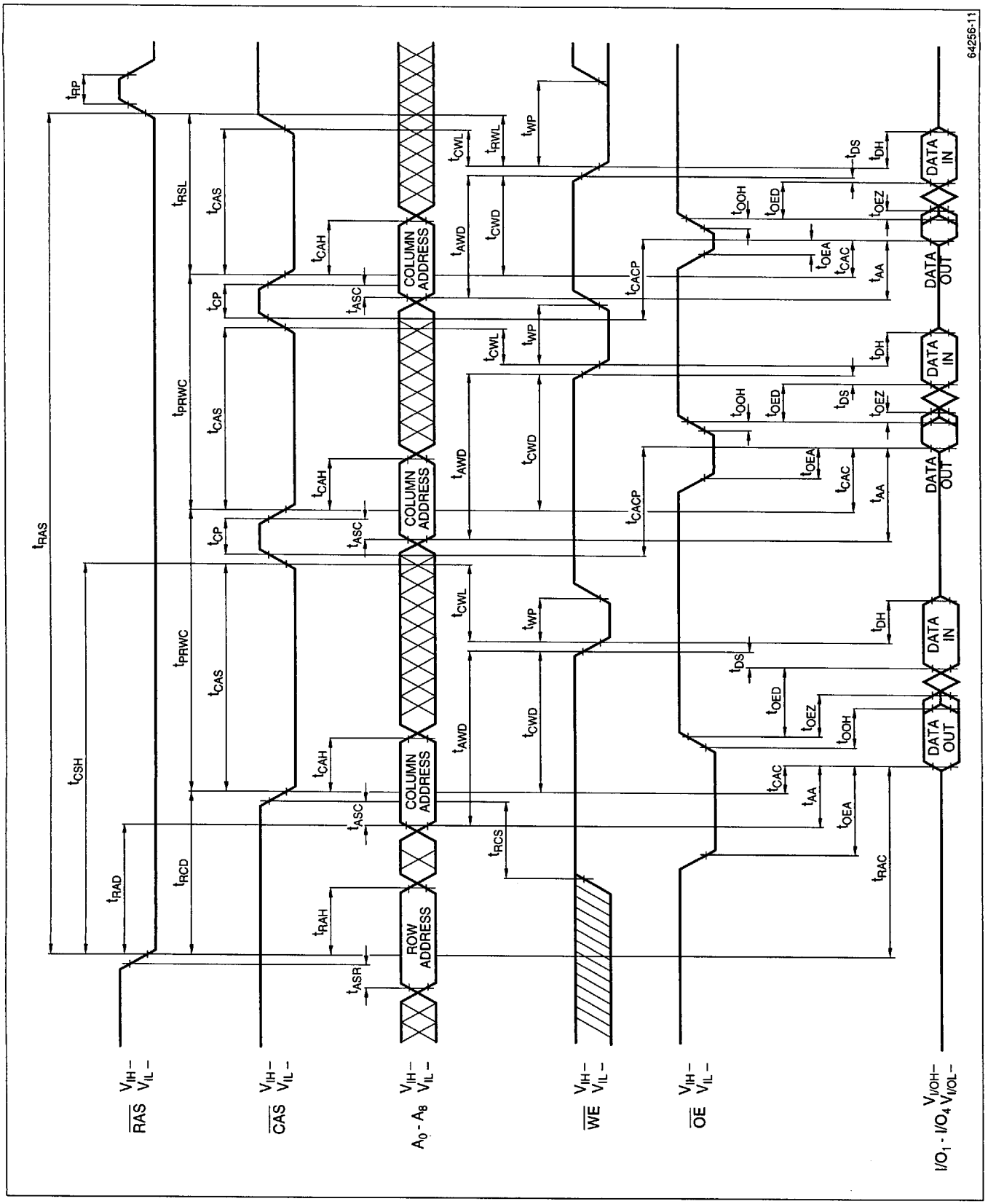


Figure 13. Fast Page Mode Read/Write Cycle

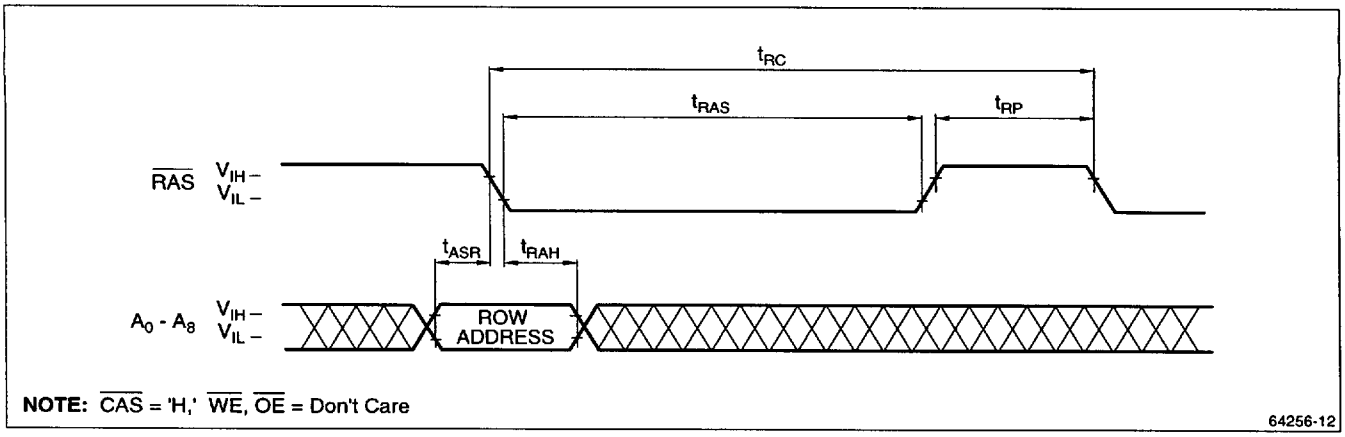


Figure 14. $\overline{RAS}$ Only Refresh Cycle

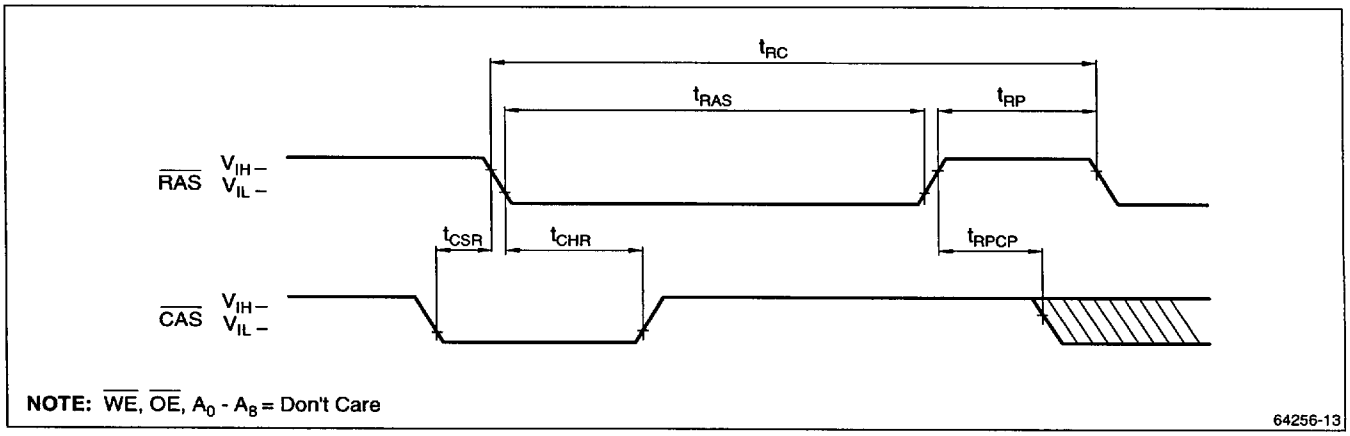


Figure 15. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

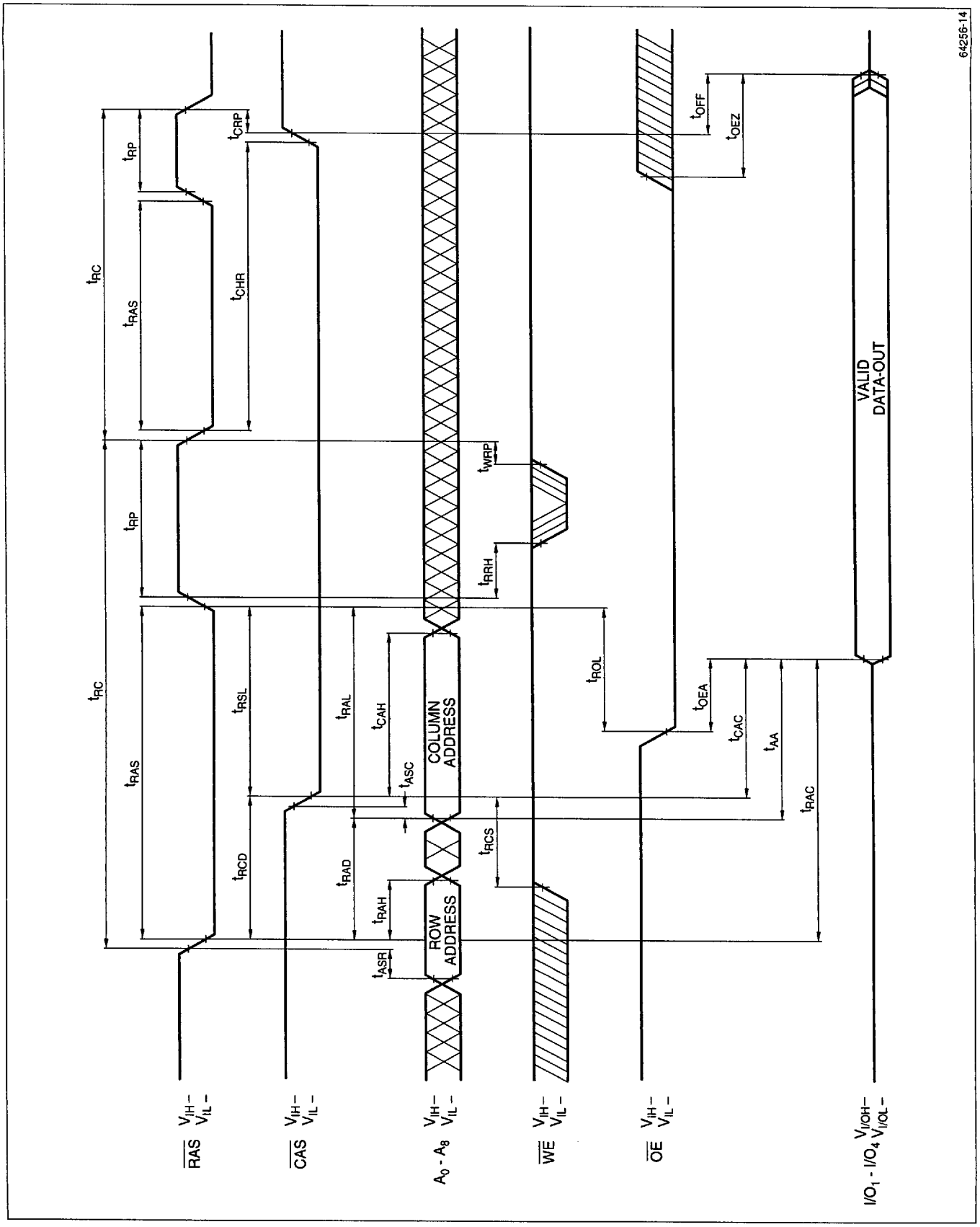
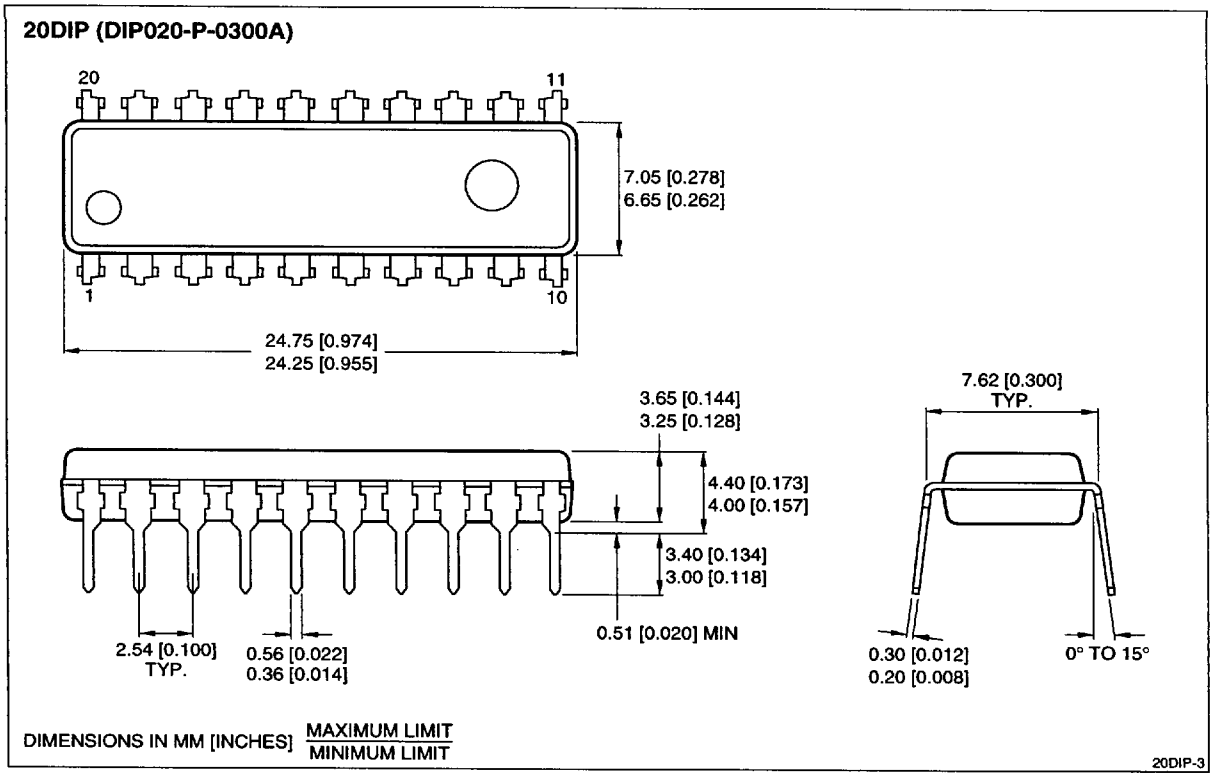
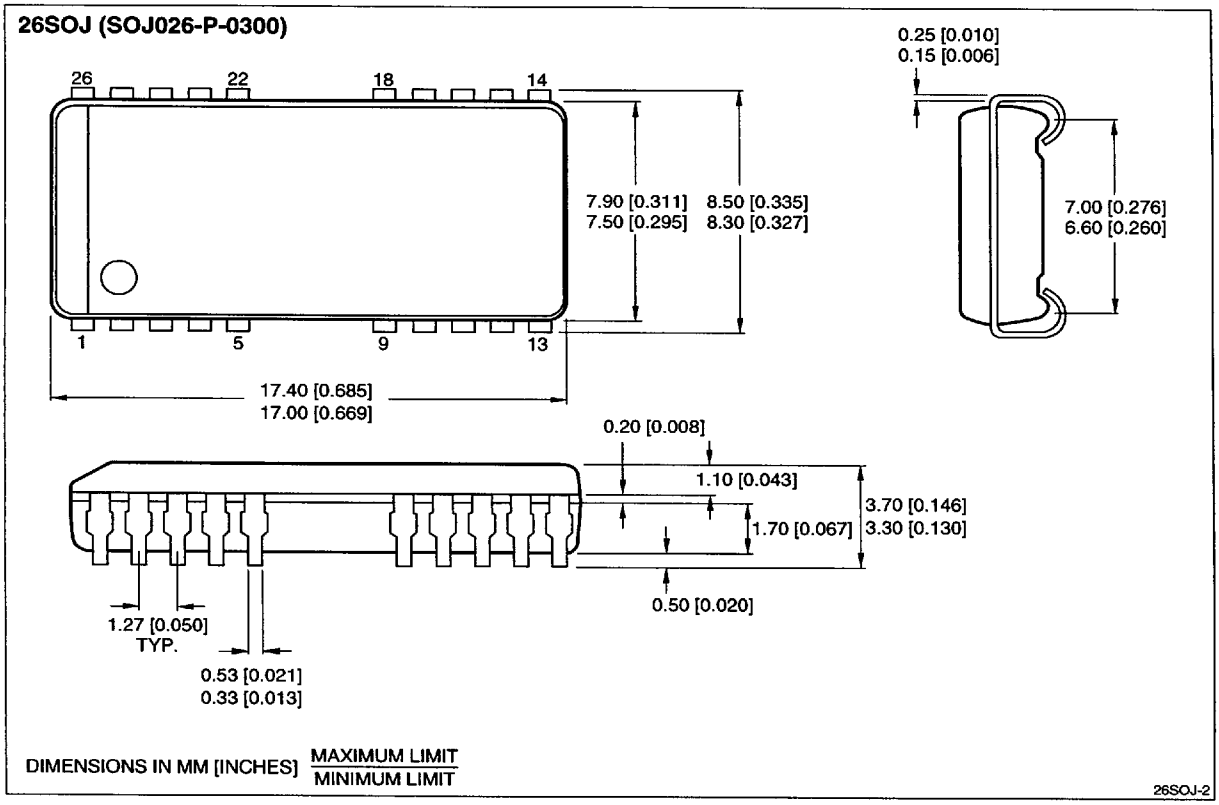


Figure 16. Hidden Refresh Cycle

PACKAGE DIAGRAMS

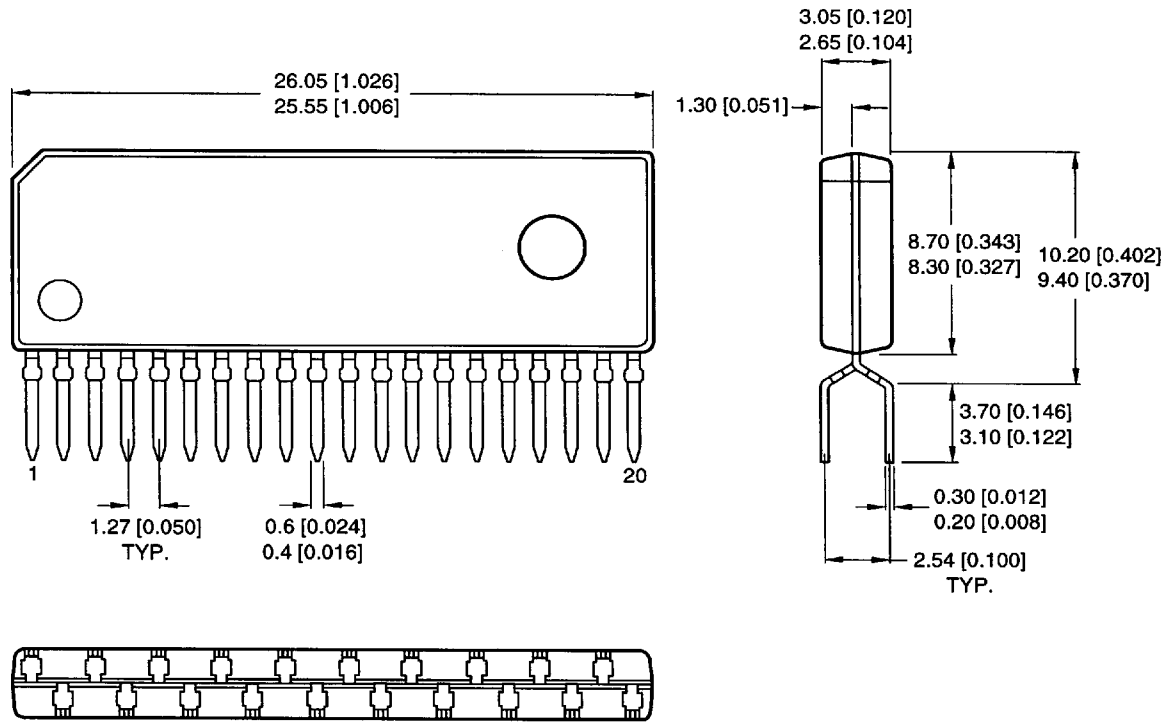


20-pin, 300-mil DIP



26-pin, 300-mil SOJ

20ZIP (ZIP020-P-0400)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

20ZIP-2

20-pin, 400-mil ZIP

ORDERING INFORMATION

LH64256B	X	- ##
Device Type	Package	Speed

- Speed: 70, 80 — Access Time (ns)
- Package: D — 20-Pin, 300-mil DIP (DIP020-P-0300A); K — 26-Pin, 300-mil SOJ (SOJ026-P-0300); Z — 20-Pin, 400-mil ZIP (ZIP020-P-0400)
- Device Type: CMOS 1M (256K x 4) Dynamic RAM

Example: LH64256BD-70 (CMOS 1M (256K x 4) Dynamic RAM, 70 ns, 20-Pin, 300-mil DIP)

64256-18