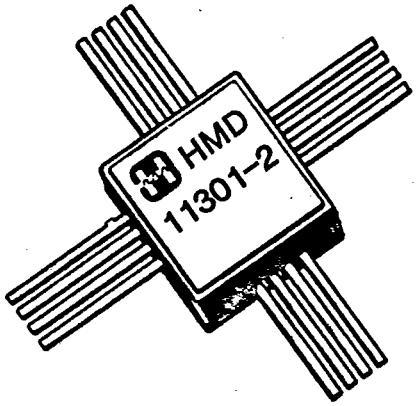
GaAs Digital IC
DIVIDE BY TWO/PRESCALER
HMD-11301-2 DC - 2.7 GHz OPERATION

PRELIMINARY PRODUCT DATA NOVEMBER 1986

HARRIS MICROWAVE SEMICONDUCTOR



TRUTH TABLE

CLEAR	SET	FUNCTION	
		Q	$\overline{Q}$
H	H	OUTPUTS ÷ 2	
L	H	L	H
H	L	H	L
L	L	H	H

FEATURES

- ☐ *Typical Input Clock Speed of 2.7 GHz*
- ☐ *Complementary ECL and GaAs Compatible Outputs*
- ☐ *Propagation Delay of 550 ps Typical*
- ☐ *Extended Temperature Range -55°C to +85°C*
- ☐ *50Ω Line Driving Capability*
- ☐ *$\overline{CE}$ Input can be used to fine-tune device performance*
- ☐ *Asynchronous Clear and Set Inputs*
- ☐ *Reliable Ti/Pt/Au Metallization System*
- ☐ *Negative Clock Edge Triggered*

GENERAL DESCRIPTION

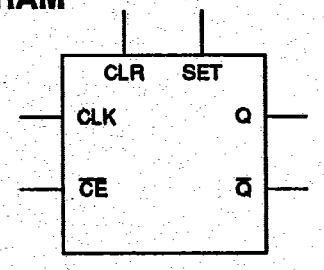
The HMD-11301-2 is a Gallium Arsenide Digital Integrated Circuit which has been designed by Harris Microwave Semiconductor to divide an input signal by two over a frequency range from DC to typically 2.7 GHz. The HMD-11301-2 clock input can be operated in an analog or digital mode. The HMD-11301-2 was designed specifically for frequency synthesizer and prescaler applications. It has a clear function to set the output lines to zero, and it can be used in conjunction with the HMD-11011-2 Divide by 10/11 to form a 2.7 GHz Divide by 20/22 Prescaler. Typical power dissipation is 1.5 W. The power supply requirements are V_{DD} = + 4.5 V, V_{SS} = - 3.5 V, $\overline{CE}$ ≈ - 1.3 V (optional), and ground. This device was designed for optimized temperature performance over a wide frequency range, and is available in a 16-pin hermetic flatpack.

* Available in die form; contact factory for details.
** Special selection of clock speed available; contact factory for details.

CIRCUIT APPLICATIONS

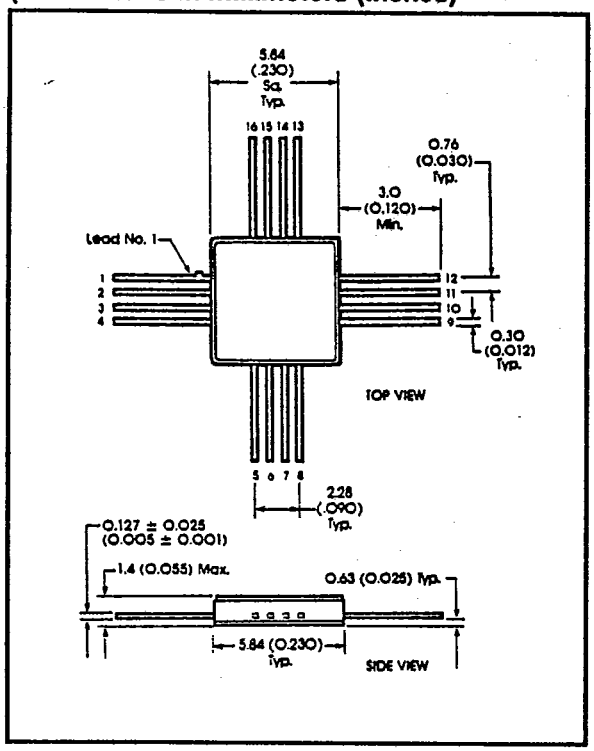
- ☐ Frequency Synthesizers
- ☐ Microwave Counters
- ☐ Satellite Receiver Systems
- ☐ Microwave Instrumentation
- ☐ High Speed Video Processing
- ☐ Prescaler for Variable Modulus Divider
- ☐ Synchronizer Circuits
- ☐ Radar Systems

LOGIC DIAGRAM



IC PACKAGE 2

(Dimensions in millimeters (inches)



PACKAGE/PIN CONFIGURATION

PIN NO.	SYMBOL	FUNCTION
1	NC	No Connection
2	NC	No Connection
3	CLK	Input Clock
4	GND	Ground (RF) **
5	$\overline{CE}$	Clock Enable
6	$-V_{SS}$	Supply Voltage
7	GND	Ground (DC)
8	$+V_{DD}$	Supply Voltage
9	Q	Data Output
10	Common	Common Output Connection *
11	$\overline{Q}$	Data Output
12	GND	Ground
13	CLR	Clear
14	SET	Set
15	NC	No Connection
16	NC	No Connection

* Connect the common output connection to ground for ECL level output.
** DC and RF grounds can be connected together.

PRODUCT RATINGS

SYMBOL	PARAMETERS	LIMITS MIN	LIMITS MAX[1]
V_{DD}	Drain to Supply Voltage	+ 4.3 V	+ 5.2 V
V_{SS}	Source Supply Voltage	- 4.0 V	- 3.0 V
I_{OH}	Output Current at Q/$\overline{Q}$		65 mA
P_{DISS}	Power Dissipation		1.8 W
T_{STG}	Storage Temperature Range	- 55°C	+ 150°C
T_{CASE}	Case Base Temperature Range	- 55°C	+ 85°C
I_{IN}	Input Current in CLK, $\overline{CE}$, CLR, SET		15 mA

NOTES: 1. Operation at conditions beyond maximum ratings may result in permanent damage.

DC CHARACTERISTICS: V_{DD} = +4.5 V, V_{SS} = -3.5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TYPICAL	UNITS	CONDITIONS, T_A = 25° C
I_{IH}	Input Current High	10	mA	$V_{IN} = V_{IH}$
I_{IL}	Input Current Low	100	µA	$V_{IN} = V_{IL}$
I_{DD}	Supply Current	150	mA	Input and Output Open
I_{SS}	Supply Current	125	mA	Input and Output Open
$\overline{CE}$	Voltage Freq. Tune	- 1.3	V	Open Circuit Potential (see Note)
V_{OH}	Output Logical High	- 0.8	V	Q Output into 50 Ω Load, Vpd -2.0 V to -3.5 V
V_{OL}	Output Logical Low	- 1.8	V	Q Output into 50 Ω Load, Vpd -2.0 V to -3.5 V
V_{TH}	Input Logic Threshold	- 1.1 to - 1.4	V	Input at 50 Ω and DC Coupled

NOTE: $\overline{CE}$ bias voltage is provided internally; however, a user available terminal is provided to fine-tune device performance. The clock enable is also used in the dual phase clock mode to enhance speed of operation; contact factory for applications assistance.

DYNAMIC CHARACTERISTICS:

V_{DD} = +4.5 V, V_{SS} = -3.5 V, V_{SET} = V_{CLR} = 0.0 V (Logical High) T_A = 25°C

SYMBOL	CHARACTERISTICS	LIMITS MIN	LIMITS TYPICAL	LIMITS MAX	UNITS
T_{PHL}, T_{PLH}	Propagation Delay		550		ps
Clock In	Maximum Clock Input Rate, Single Phase	2200	2700		MHz
Clock In	Maximum Clock Input Rate, Dual Phase		3000		MHz
T_{TLH}	Output Transition Time, Low to High (20% to 80%)		150		ps *
T_{THL}	Output Transition Time, High to Low (80% to 20%)		220		ps *

* Output Loading Capacitance = 2 pf