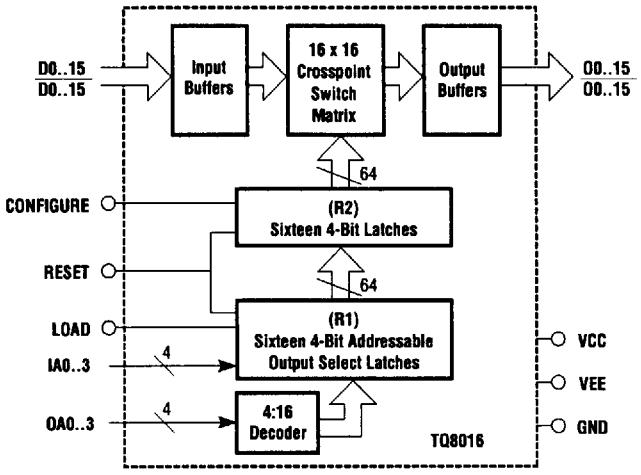
TQ8016

16 x 16 Digital Crosspoint Switch



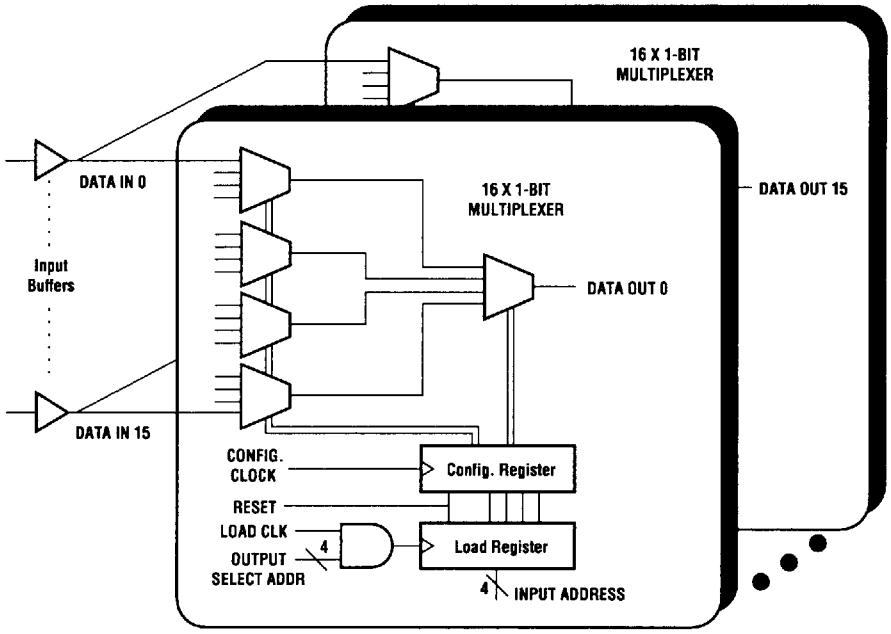
The TQ8016 is a 16 x 16 differential digital crosspoint switch capable of handling 1.3 Gbit/s data rate (min.). The high data rate and exceptional signal fidelity is made possible with TriQuint's fully differential Source-Coupled FET Logic (SCFL) standard cells. The symmetrical switching characteristic inherent in differential logic results in low signal skew and crosstalk for maximum signal fidelity.

The user can independently configure any switch output to any input, including an input chosen by another output. To configure the switch, the 4-bit output address (OA0..3) is decoded to enable the loading of the 4-bit input selection data (IA0..3) on the rising edge of the LOAD signal. The process is repeated until all desired connections are programmed. By bringing the CONFIGURE signal high, the contents of the Output Select Latches are transferred in parallel to a second row of 4-bit latches (R2), causing the switch reconfiguration. This double row architecture minimizes the time to completely reconfigure the switch since a new set of addresses can be loaded to the Output Select Latches (R1) while the switch is active (transmitting). At the time of reconfiguration, no data drop-out occurs for any output whose input connection does not change. For applications which do not require synchronous configuration of the switch, the LOAD and CONFIGURE inputs may be tied together.

Features

- *1.3 Gbits/s data rate (min.)*
- *Non-blocking architecture*
- *±200 ps delay match (one input to all outputs)*
- *ECL-level data inputs/outputs; CMOS-level control inputs*
- *Low crosstalk*
- *Fully differential data path*
- *Double row of output select latches minimizes reconfiguration time*
- *Available in 132-pin leaded chip carrier*

TQ8016 Architecture



Pin Descriptions

Pin Name	Levels	Description	Pin Name	Levels	Description
D0-D15	ECL	Differential Data Inputs	CONFIGURE	CMOS	Switch Reconfiguration
$\overline{D0\text{-}D15}$	ECL	Differential Data Inputs	RESET	CMOS	Pass-Through or Broadcast Mode
O0-O15	ECL	Differential Data Outputs	LOAD	CMOS	Loads Input Address
$\overline{O0\text{-}O15}$	ECL	Differential Data Outputs	GND	0 V	Ground Reference
IA0-IA3	CMOS	Input Address	VEE	-5 V	Power Supply
OA0-OA3	CMOS	Output Address	VCC	+5 V	Power Supply

Absolute Maximum Ratings[4]

Symbol	Parameter	Absolute Max. Rating	Notes
T_{STOR}	Storage Temperature	-65° C to +150° C	
T_J	Junction Temperature	-55° C to +150° C	
T_C	Case Temperature Under Bias	-55° C to +125° C	1
V_{CC}	Supply Voltage	0 V to +7 V	2
V_{EE}	Supply Voltage	-7 V to 0 V	2
V_{TT}	Load Termination Supply Voltage	V_{EE} to 0 V	3
V_{IN}	Voltage Applied to Any ECL Input; Continuous	V_{EE} -0.5 V to +0.5 V	
I_{IN}	Current Into Any ECL Input; Continuous	-1.0 mA to +1.0 mA	
V_{IN}	Voltage Applied to Any TTL/CMOS Input; Continuous	-0.5 V to V_{CC} +0.5 V	
I_{IN}	Current Into Any TTL/CMOS Input; Continuous	-1.0 mA to +1.0 mA	
V_{OUT}	Voltage Applied to Any ECL Output	V_{EE} -0.5 V to +0.5 V	3
I_{OUT}	Current From Any ECL Output; Continuous	-40 mA	
P_D	Power Dissipation per Output $P_{OUT} = (GND - V_{OUT}) \times I_{OUT}$	50 mW	

Notes: 1. T_C is measured at case top.
2. All voltages specified with respect to GND, defined as 0V.
3. Subject to I_{OUT} and power dissipation limitations.
4. Absolute maximum ratings, as detailed in this table, are the ratings beyond which the device's performance may be impaired and/or permanent damage to the device may occur. Functionality and/or adherence to electrical specifications is not implied when the device is subjected to conditions that exceed, singularly or in combination, the operating range specified in the Recommended Operating Conditions table, below.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
T_C	Case Operating Temperature	0	25	85	°C	1
GND	Ground Reference Voltage		0		V	
V_{CC}	Supply Voltage	4.5		5.5	V	
V_{EE}	Supply Voltage	-5.5		-4.5	V	
V_{TT}	Load Termination Supply Voltage		-2.0		V	2
R_{LOAD}	Output Termination Load Resistance		50		Ω	2

Notes: 1. T_C measured at case top. Use of adequate heatsink is required.
2. The V_{TT} and R_{LOAD} combination is subject to maximum output current and power restrictions.

DC Characteristics[1] $T_C = 0°C$ to $85°C$, $V_{CC} = 4.5$ V to 5.5 V, $V_{EE} = -5.5$ V to -4.5 V, GND = 0 V, unless otherwise indicated.

Symbol	Parameter	Min	Typ	Max	Units	Test Cond.	Notes
V_{IH}	ECL Input Voltage High	-1100		-500	mV		
V_{IL}	ECL Input Voltage Low	V_{TT}		-1500	mV		
I_{IH}	ECL Input Current High			+30	µA	$V_{IH} = 0.7$ V	
I_{IL}	ECL Input Current Low			-30	µA	$V_{IL} = -2.0$ V	
V_{ICM}	ECL Input Common Mode Voltage	-1500		-1100	mV		
V_{IDIF}	ECL Input Differential Voltage (P-P)	400		1200	mV		
V_{IH}	CMOS Input Voltage High	3.5		V_{CC}	V		
V_{IL}	CMOS Input Voltage Low	0		1.5	V		
I_{IH}	CMOS Input Current High			+100	µA	$V_{IH} = V_{CC}$	
I_{IL}	CMOS Input Current Low	-100			µA	$V_{IL} = 0$ V	
V_{OCM}	ECL Output Common Mode	-1500		-1100	mV		
V_{ODIF}	ECL Output Differential Voltage	600			mV		
V_{OH}	ECL Output Voltage High	-1000		-600	mV		
V_{OL}	ECL Output Voltage Low	V_{TT}		-1600	mV		
I_{OH}	ECL Output Current High	20	23	27	mA		
I_{OL}	ECL Output Current Low	0	5	8	mA		
I_{CC}[2]	Power Supply Current		15	20	mA		
I_{EE}[2]	Power Supply Current		730	950	mA		

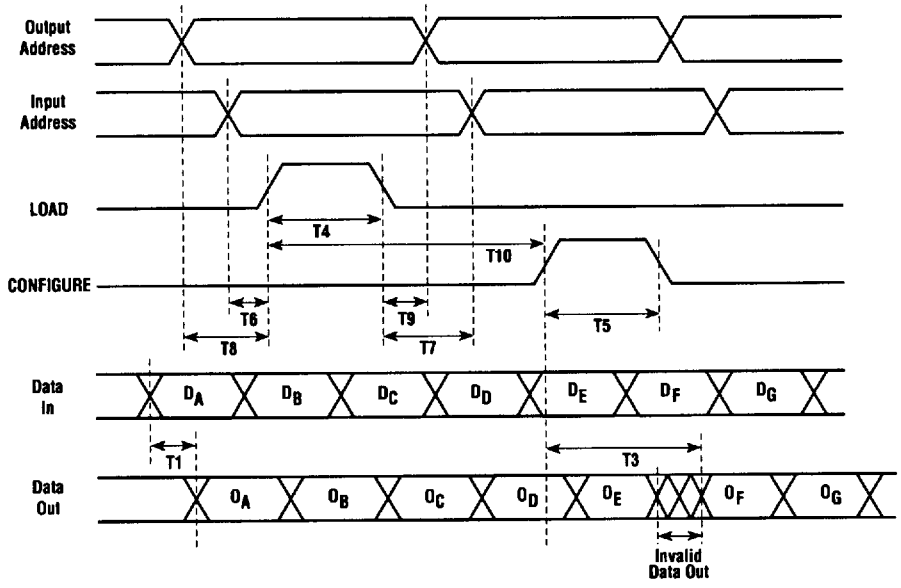
Notes: 1. Test conditions unless otherwise indicated: $V_{TT} = -2.0$ V, $R_{LOAD} = 50\,\Omega$ to V_{TT}.
2. Positive current is defined as flowing into the device and negative current as flowing out of the device. I_{CC} typically flows into the device and I_{EE} flows out of the device.

AC Characteristics[1]

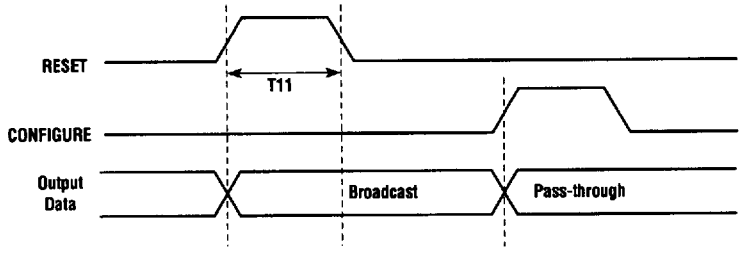
Symbol	Parameter	Min	Typ	Max	Units	Notes
F_C[1]	Maximum Input Frequency	1.3			Gbit/s	
T_1	Data In (Di) to Data Out (Oi) Delay		1200		ps	
T_2	Propagation Delay Match (one input to all outputs)		±200		ps	
T_3	CONFIGURE to Data Out (Oi) Delay			5	ns	
T_4	LOAD Pulse Width	10			ns	
T_5	CONFIGURE Pulse Width	10			ns	
T_6	IAi to LOAD High Setup Time	0			ns	
T_7	LOAD to IAi Low Hold Time	5			ns	
T_8	OAi to LOAD High Setup Time	5			ns	
T_9	LOAD to OAi Low Hold Time	5			ns	
T_{10}	Load ↑ to CONFIGURE ↑	0			ns	
T_{11}	RESET Pulse Width	10			ns	
$T_{R,F}$	Output Rise or Fall Time		250	400	ps	2

Notes: 1. Test conditions: $V_{TT} = -2.0$ V, $R_{LOAD} = 50\,\Omega$ to V_{TT}; ECL inputs: $V_{IH} = -1.1$ V; $V_{IL} = -1.5$ V; CMOS inputs: $V_{IH} = 3.5$ V, $V_{IL} = 1.5$ V; ECL Outputs: $V_{OH} \geq -1.0$ V, $V_{OL} \leq -1.6$ V; ECL inputs rise and fall times ≤ 1 ns; CMOS inputs rise and fall times ≤ 20 ns
2. Rise and fall times are measured at the 20% and 80% points of the transition from V_{OL} max to V_{OH} min.

Timing Diagram

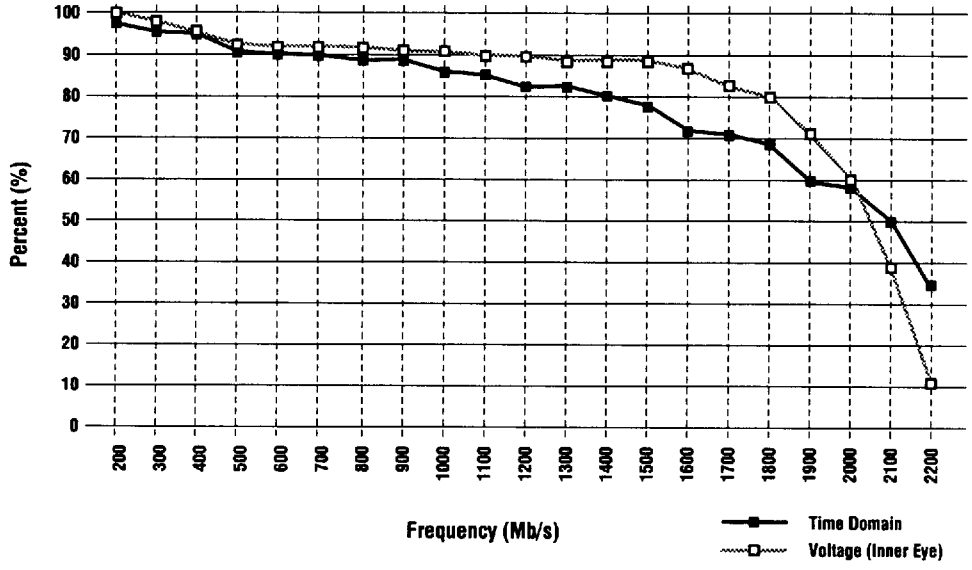


Timing Diagram



Notes: 1. *LOAD input must remain LOW to insure correct programming of the switch*
2. *"Broadcast" is defined as data input 0 to all data outputs (0..15).*
3. *"Pass-through" is defined as data input 0 to data output 0, data input 1 to data output 1, etc.*

AC Performance Measurements
(Percent Recoverable "Eye" vs. Frequency 16 x 16)



Typical Error-Free Area

The above graph shows the typical error-free area of a 2^23 Pseudo-Random Bit Stream "eye" pattern. Data is provided for both time and voltage domains of the differential DIN0 to DOUT0 data path for various data rates. An interference pattern was applied to all other inputs in parallel to induce worst-case cross talk.

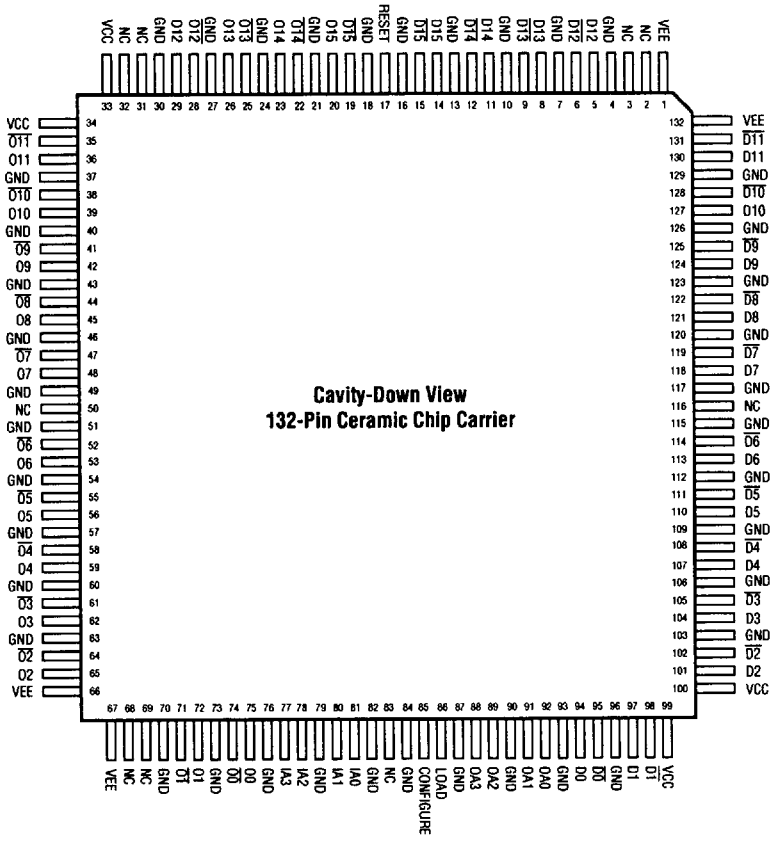
For the time domain, Peak-to-Peak Jitter was measured at the eye crossing and an error-free percentage value was computed using the following formula:

(Data_Period - PPJitter) x 100 / Data_Period

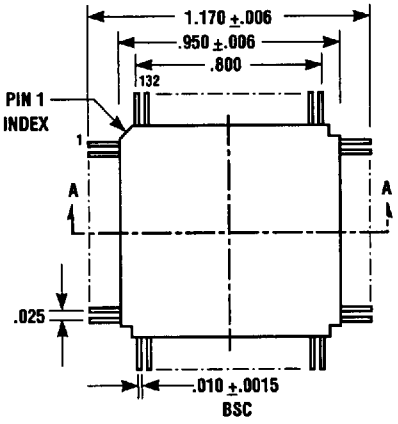
Voltage values are referenced to an initial inner eye measurement at 400 MBs. Subsequent percentage values were computed using the following formula:

V_{INNER} x 100 / V_{INNER} @ 400 MBs

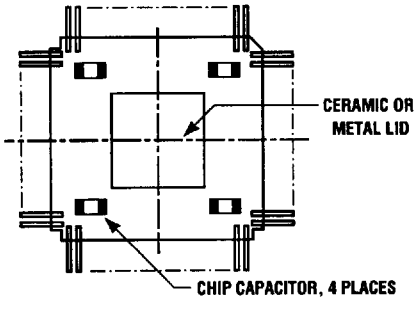
Pinout



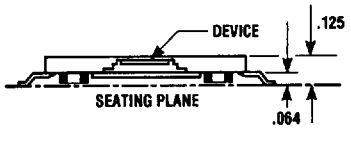
Mechanical Dimensions – TOP View



BOTTOM View



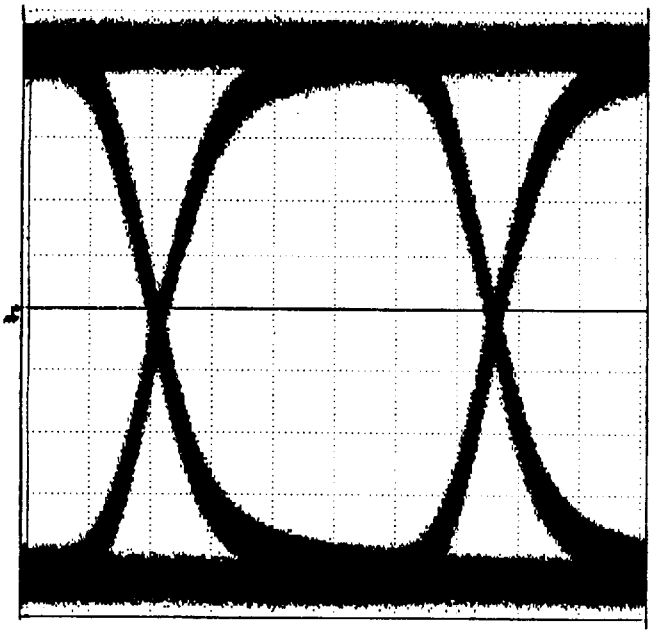
Section A-A



1200 MBs Data "Eye" Pattern

Differential Waveform Characteristics
(OUT - $\overline{OUT}$)

Channel	0
Frequency	1200 MBs
Rise Time (20% - 80%)	195 ps
Fall Time (20% - 80%)	195 ps
Jitter (Peak-to-Peak)	40 ps
Time/Division	125 ps
Volts/Division	250 mV



Time/Div: 150 ps

Ordering Information

TQ8016 –

M = 132-Pin Ceramic Package
D = Die

Section 6 - Packaging

Thermal Resistance Information

Power Dissipation Calculations

The maximum power dissipation that an IC can tolerate is determined by the thermal impedance characteristics of the package. The equation to find the allowable power dissipation at a given ambient operating temperature is:

$$P_D = (T_J - T_A) / \theta J_A, \text{ where:}$$

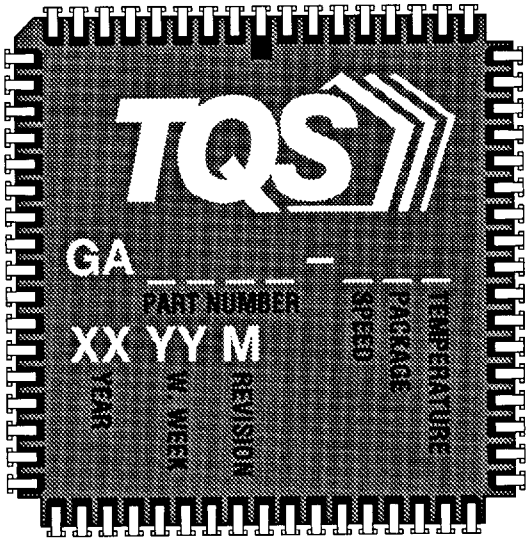
P_D = power dissipation at ambient operating temperature
T_J = maximum junction operating temperature (150°C is typically used)
T_A = maximum ambient operating temperature (free air)
θJ_A = typical thermal resistance of junction to ambient (°C/W)

Packaging Notes

Unless otherwise indicated, all thermal impedances listed are typical range values or values in still air for the package only. These impedances will vary when additional heat sinking capability is provided through PCB solder attachment or air flow.

Device Markings

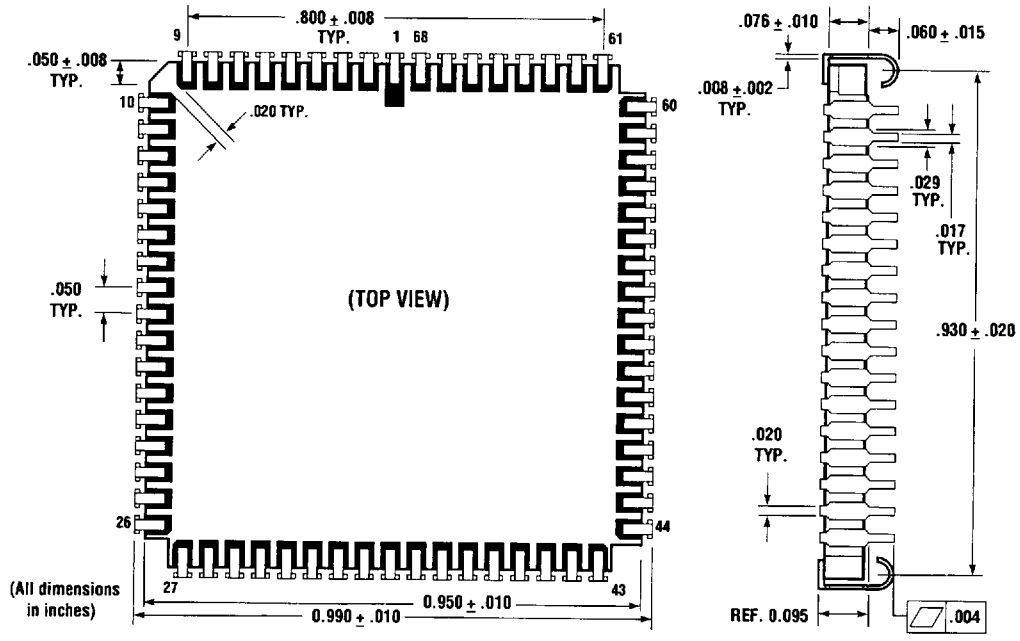
TriQuint's Standard Device Markings



Package Outlines

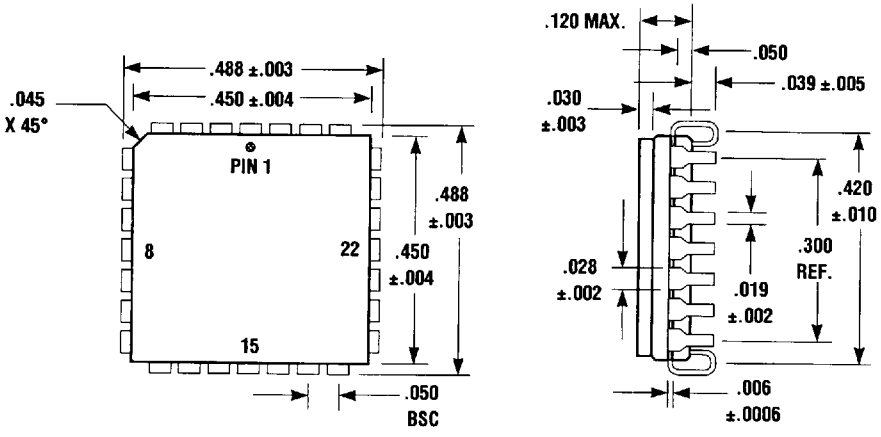
68-Pin J-Lead (CLCC) Package

Packaging for: GA9011, GA9012 (θJ_A = 25°C/Watt)



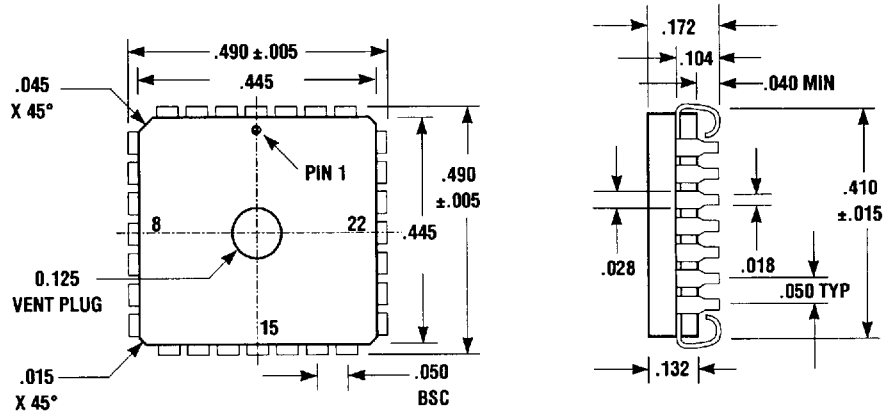
28-Pin J-Lead CerQuad Package

Packaging for: GA9101, GA9102 (θJ_A = 60°C/Watt)



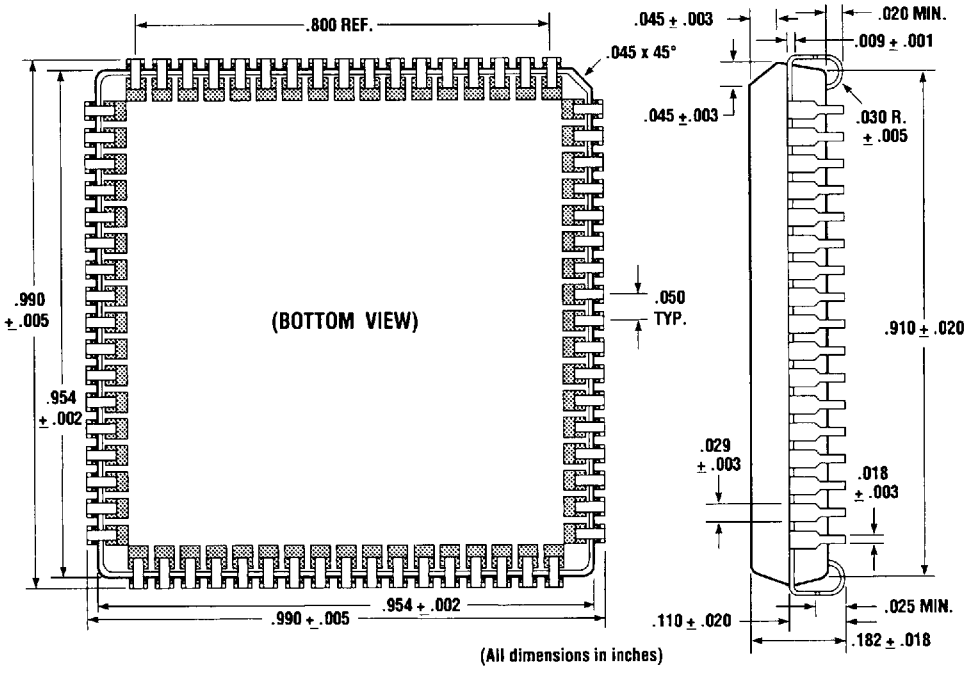
28-Pin J-Lead MQuad Package

Packaging for: GA9101, GA9102 (θJ_A = 42°C/Watt)



68-Pin PLCC Package

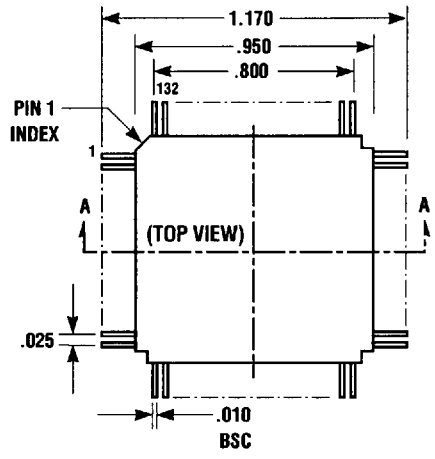
Packaging for: GA9103, GA9104 (θJ_A = 47°C/Watt)

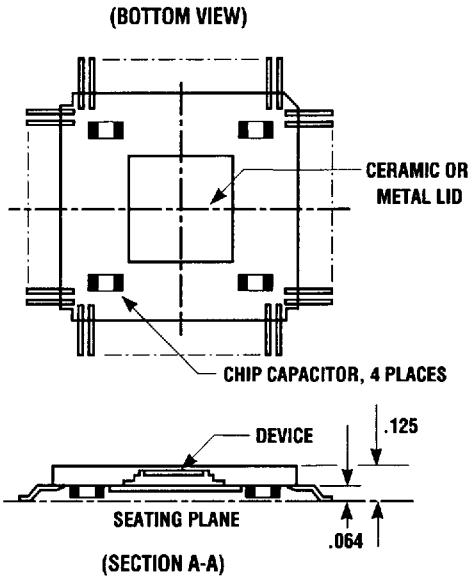


(All dimensions in inches)

132-Pin Leaded Ceramic Chip Carrier

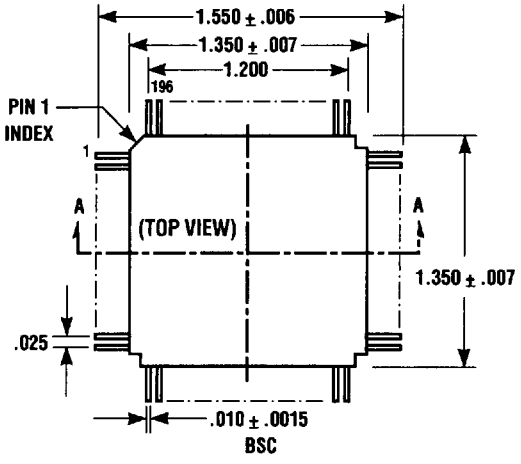
Packaging for: TQ8016 (Heat sink required, θJ_C = 8°C/Watt)

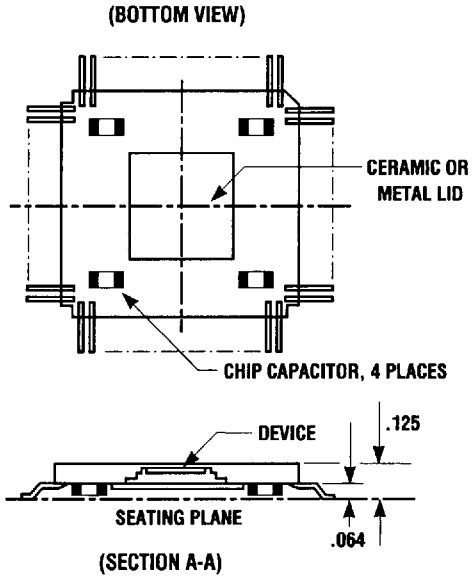




196-Pin Leaded Ceramic Chip Carrier

Packaging for: TQ8032 (Heat sink required, θJ_C = 8°C/Watt)





TriQuint SEMICONDUCTOR