PLESSEY Semiconductors

ADVANCE INFORMATION

T-77-07-05

MV1740

MAC TELETEXT DECODER

The MV1740 is the Teletext chip for the Nordic VLSI C/D/D2 MAC Packet receiver chipset.

The MV1740 is a single chip Teletext decoder capable of decoding VBI and MAC packet Teletext as well as normal terrestrial Teletext for 625 line systems. With dual page acquisition circuits, and direct memory addressing, the current selected page can always be kept live while the second acquisition circuit stores linked or other pages. The control of the MV1740 is via the I²C Bus with the configuration chain being used to select data configurations and codes.

FEATURES

- Non-display packets stored for linked page operation, video programming, and other advanced uses.
- Low external component count.
- Can decode MAC packets, D2MAC VBI and terrestrial World System Teletext.
- Multi-language capability for European languages .
- Up to 254 display pages stored, using two low cost 200ns DRAMs.
- High resolution characters 16 by 10 dot matrix.
- On chip Descrambler.
- Displays microcomputer generated pages.

DESCRIPTION OF SIMPLIFIED BLOCK DIAGRAM

PACKET RECEPTION AND TIMING

The packet header control, provides for packet reception and timing for packet processing. Each incoming packet has a header with a 10 bit address, one bit indicating in which subframe it is located, and a two bit continuity index. The packet header of each packet is compared with the contents of the configuration chain, and packets which match address and subframe are sorted out. The packet type byte is used to indicate whether the text packets are scrambled.

DESCRAMBLER

Descrambler synchronisation can be achieved at the start of new frames. All three different levels of access-control described in the MAC standard [1] are supported;

Free access, unscrambled:

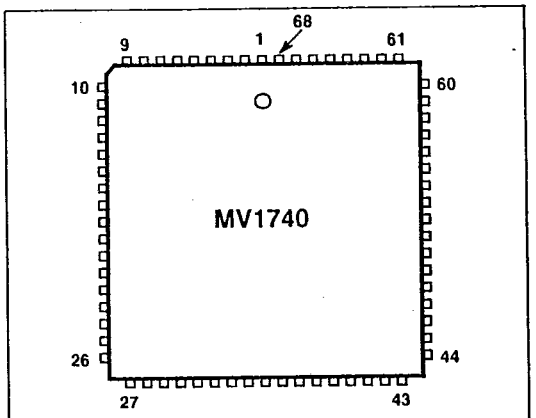
The Teletext data is delivered unchanged.

Free access, scrambled:

The Teletext data is descrambled with a local control word stored in the receiver.

Conditional access, scrambled:

The Teletext data is descrambled with a regenerated control word from the encryption system.



Pin	Function	Pin	Function
1	VDD	35	VSS
2	VSS	36	VDD
3	NC	37	TCR
4	SIC	38	BLANK
5	NC	39	RED
6	TTV	40	GREEN
7	VAL	41	BLUE
8	SIV	42	YOP
9	CSTRB	43	CSO
10	CDATAIN	44	A9
11	EFCNT	45	D1
12	NC	46	VSS
13	CLK1	47	$\overline{A8}$
14	PDATA	48	$\overline{CAS}$
15	NC	49	$\overline{D0}$
16	VSS	50	$\overline{WR}$
17	VDD	51	$\overline{A6}$
18	NC	52	$\overline{RAS}$
19	ODATA	53	VDD
20	STRB42	54	A3
21	STRB90	55	A0
22	GSTRB	56	A4
23	CDATAOUT	57	A2
24	VSS	58	A5
25	$\overline{XTO}$	59	A1
26	$\overline{XTI}$	60	A7
27	$\overline{XCK}$	61	VDD
28	$\overline{RESET}$	62	I2C SCL
29	SYNCI/O	63	$\overline{I2C\ SDA}$
30	DATAI/O	64	$\overline{EVENT}$
31	EXT	65	$\overline{SE}$
32	BLC	66	TEST
33	WLC	67	VBIDAT
34	VIDEO	68	CLKD2

Fig.1 Pin connections - top view

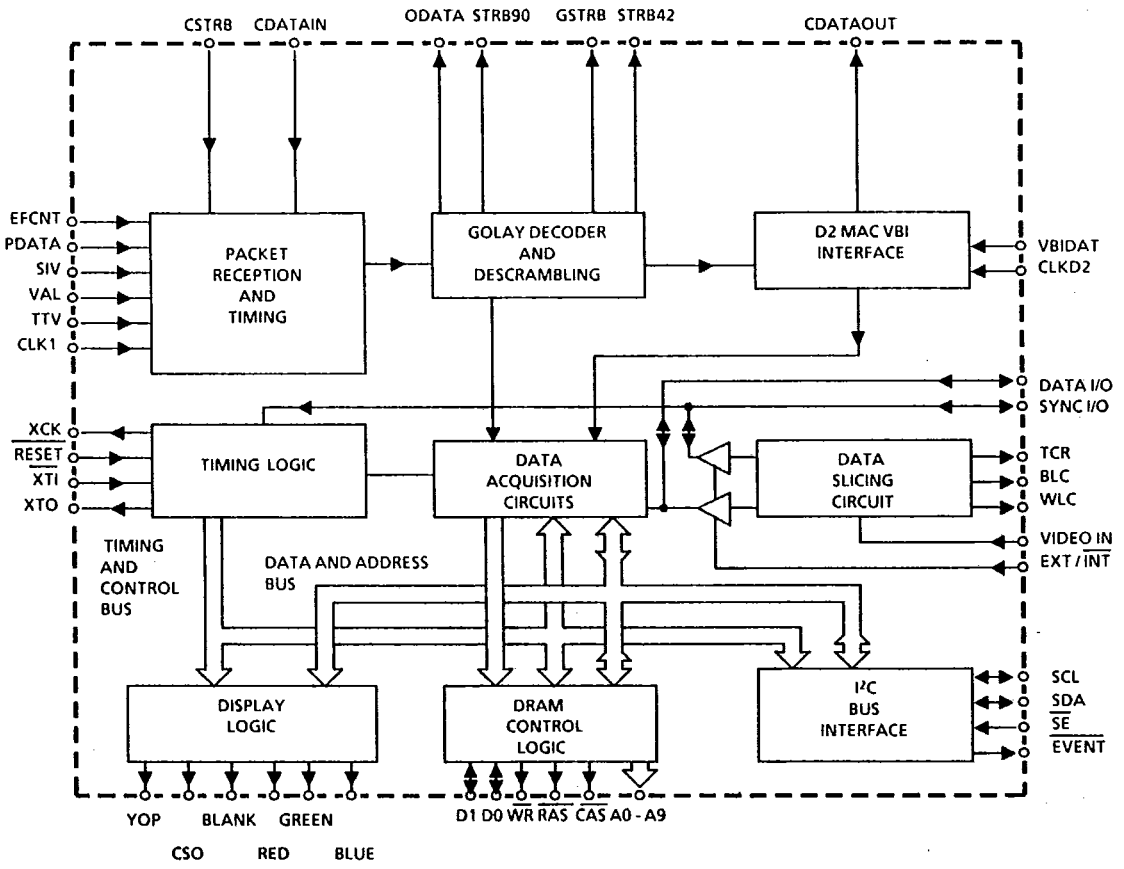


Figure 2. MV1740 Block Diagram

The signal EFCNT is the most significant bit in a frame counter, and it is used to resynchronise the descrambler. The other bits of the frame counter may be supplied by the configuration chain, to assure fast recovery after change of channel or power-up. The signal SIV starts an update of the descrambling system for each frame. The control word for the descrambling is provided by the configuration chain.

GOLAY DECODER

The Golay decoder receives MAC packets (all except header and PT byte) from the descrambler and corrects up to three errors in 12 information bits of each Golay word (24,12).

DATA ACQUISITION CIRCUIT

The MV1740 has dual acquisition circuits to ensure that the viewed page can always be kept live while the second acquisition circuit stores linked or other pages. The data acquisition circuits can accept data from one of three sources:

1: Parallel data from the internal Golay decoder.
2: D2MAC VBI serial data.
3: Video signal, data extracted using internal data slicer.

After Hamming Code checking and correction, the data is latched into the appropriate registers and compared with the internal programmable registers, as set up by the controlling microprocessor, to check for the desired magazine and page. The Teletext data is stored in two external DRAMS controlled completely by the MV1740.

I²C BUS INTERFACE

The MV1740 can be addressed on the I²C bus as either a slave transmitter or a slave reciever

The MV1740 has twelve read registers and nineteen write registers controlled via the I²C Bus. These registers control data acquisition and display. They are also used to inform the microprocessor of details of the received Teletext data. The register structure of the MV1740 allows the microprocessor to quickly read the Event and Page Receive registers, which hold the information on the page being currrently received.

TIMING LOGIC

The internal timing of the MV1740 is based on a single 27.75MHz crystal. To enable the MV1740 to be used with microprocessor generated text, a composite synchronisation pulse is generated on-chip if an external one is not available .

DRAM CONTROL LOGIC T-77-07-05

The display memory uses two low cost DRAMs which are controlled by the MV1740, including all the necessary refresh cycles. Refresh occurs during the line flyback period on all ten address lines. The two DRAMs may be either: 64K x 1, 256K x 1, or 1M x 1 giving 14, 62, or 254 displayable pages in memory, (a display page consists of packets 0 to 25). In addition there are two pages of store for non-display packets. These two pages will store two versions of packets 29 and 30 and any mix of packets 26, 27, or 28 up to a total maximum of 23 packets per acquisition circuit. It is also possible for the MV1740 to use two 4Mbyte DRAMs if the extra address lines are externally controlled.

DISPLAY LOGIC

The MV1740 display is controlled via four write registers. Any of the stored pages in DRAM may be displayed. The features controlled include :

Which acquisition circuit is displayed;
Language displayed;
Control of display of the header;
Display of TEXT, PICTURE, or MIX;
Display of boxes of either text or picture;
Reveal of text hidden by "conceal" control codes;
Cursor control;
The display of rows 25 and 26;
Double height display of,
- Top half of text,
- Middle half of text,
- Bottom half of text.

Rows 25 & 26 can be displayed under software control. The contents of these rows will be optionally written by packets X/24 and X/25 dependent on the status of a register bit. A row zero write inhibit bit in a register will prevent the transmitted data in the header packet writing to memory, so that the microprocessor may process packet 8/30 data and write its own header line at the top of the screen.

THE CONFIGURATION CHAIN

The configuration chain is effectively a long shift register running through all circuits which are to be configured from the microprocessor. Several functions of the MV1740 are controlled by the configuration chain. The packet control block needs the MAC packet addresses and indication of which subframe (or both) to select MAC packets from. The configuration chain also provides control words for descrambling.

The seven least significant bits of the frame count (FCNT) and one bit indicating the update of the descrambling after a change of service or power up are placed in the configuration chain.

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ABSOLUTE MAXIMUM RATINGS
(Referenced to V_{SS})

DC Supply voltage V_{DD}	-0.3V to +7V
Input voltage	-0.3V to V_{DD} +0.3V
Storage temperature range	-55°C to +125°C
Ambient operating temperature	0°C to +70°C

ELECTRICAL CHARACTERISTICS
Test conditions (unless otherwise stated)
T_{amb} = 0°C to +70°C, V_{DD} = +4.75V to +5.25V

Characteristic	Value		Units	Conditions
	Min.	Max.		
Low input voltage	V_{SS}	1.2	V	
High input voltage	3.4	V_{DD}	V	
Low output voltage		0.4	V	I_{OL} = 10mA
High output voltage	V_{DD} -0.4		V	I_{OH} = -10mA
Clock 1 frequency	1	21	MHz	

(ref.1) MAC packet family specifications EBU No. TECH 3258-E