

SANYO

No. ※5085A

LC322271J, M, T-70/80**2 MEG (131072 words × 16 bits) DRAM
Fast Page Mode, Byte Write****Preliminary****Overview**

The LC322271J, M and T is a CMOS dynamic RAM operating on a single 5 V power source and having a 131072 words × 16 bits configuration. Equipped with large capacity capabilities, high speed transfer rates and low power dissipation, this series is suited for a wide variety of applications ranging from computer main memory and expansion memory to commercial equipment.

Address input utilizes a multiplexed address bus which permits it to be enclosed in a compact plastic package of SOJ 40-pin, SOP 40-pin, and TSOP 44-pin. Refresh rates are within 8 ms with 512 row address (A0 to A7, A8R) selection and support Row Address Strobe (RAS)-only refresh, Column Address Strobe (CAS)-before-RAS refresh and hidden refresh settings. There are functions such as fast page mode, read-modify-write and byte write. The pin assignment follows the JEDEC 1 M DRAM (65536 words × 16 bits, 1CAS/2WE) standard.

Features

- 131072 words × 16 bits configuration.
- Single 5 V ± 10% power supply.
- All input and output (I/O) TTL compatible.
- Supports fast page mode, read-modify-write and byte write.
- Supports output buffer control using early write and Output Enable ($\overline{OE}$) control.
- 8 ms refresh using 512 refresh cycles.
- Supports RAS-only refresh, CAS-before-RAS refresh and hidden refresh.
- Follows the JEDEC 1 M DRAM (65536 words × 16 bits, 1CAS/2WE) standard.
- RAS access time/column address time/CAS access time/cycle time/power dissipation

• **Package:**

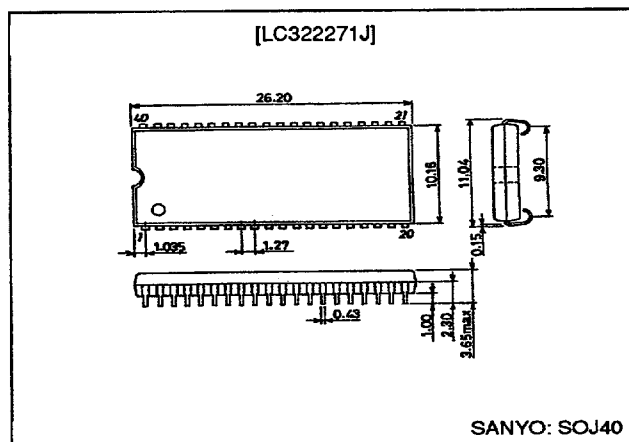
SOJ 40-pin (400 mil) plastic package : LC322271J

SOP 40-pin (450 mil) plastic package: LC322271M

TSOP 44-pin (400 mil) plastic package : LC322271T

Package Dimensions

unit: mm

3200-SOJ40

Parameter	LC322271J, M, T	
	-70	-80
RAS access time	70 ns	80 ns
Column address access time	35 ns	45 ns
CAS access time	20 ns	30 ns
Cycle time	130 ns	150 ns
Power dissipation (max.)	During operation	688 mW
	During standby	633 mW
	5.5 mW (CMOS level)/11 mW (TTL level)	

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32896HA (OT)/33195TH (OT) No. 5085-1/29

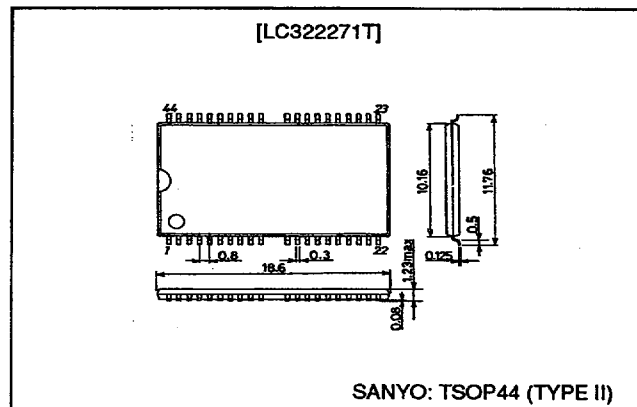
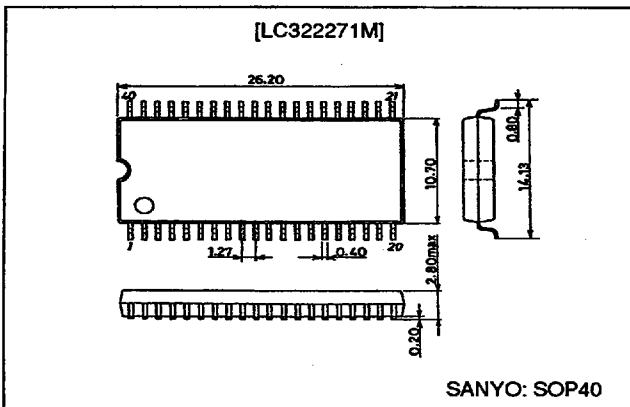
Package Dimensions

unit: mm

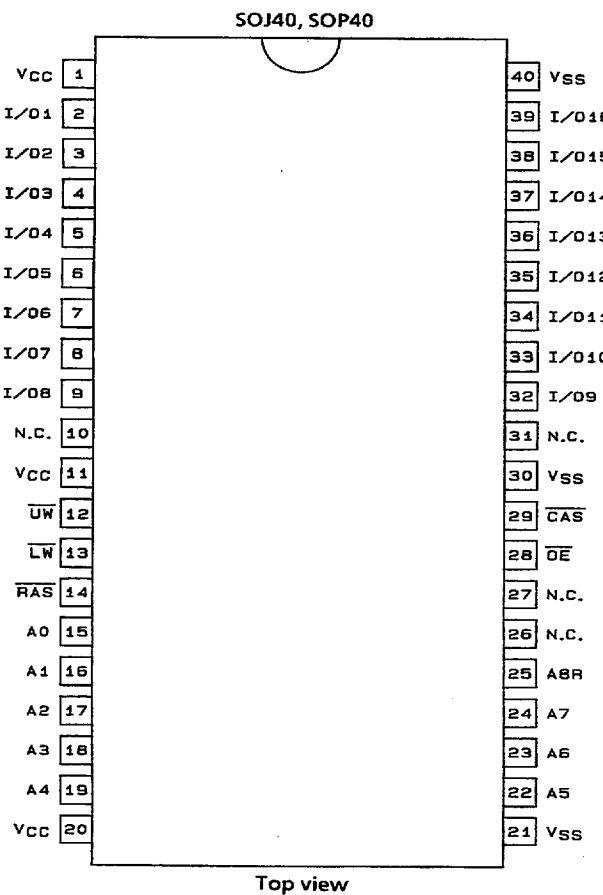
3195-SOP40

unit: mm

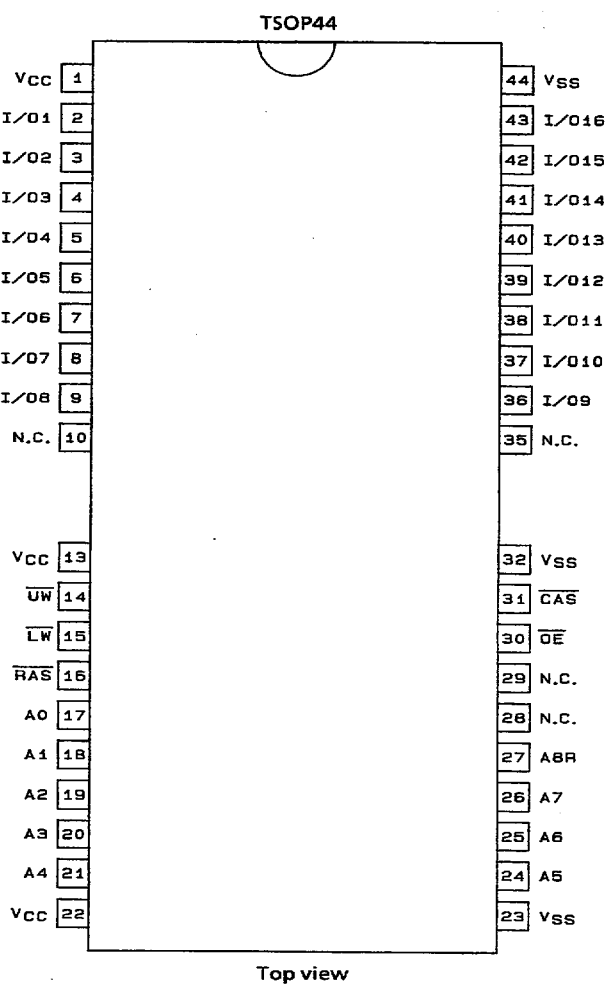
3207-TSOP44



Pin Assignments

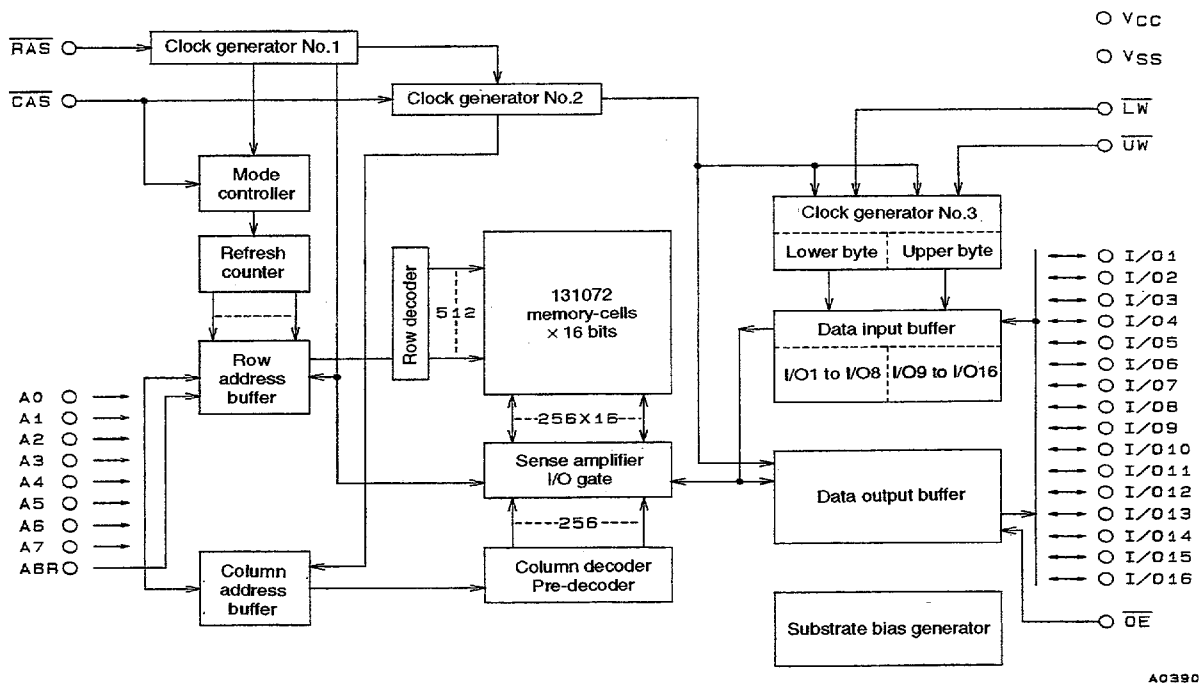


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Block Diagram



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Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Maximum supply voltage	$V_{CC \text{ max}}$	-1.0 to +7.0	V	1
Input voltage	V_{IN}	-1.0 to +7.0	V	1
Output voltage	V_{OUT}	-1.0 to +7.0	V	1
Allowable power dissipation	LC322271J, M LC322271T	$P_d \text{ max}$	800 700	mW 1
Output short-circuit current	I_{OUT}	50	mA	1
Operating temperature range	T_{opr}	0 to +70	°C	1
Storage temperature range	T_{stg}	-55 to +150	°C	1

Note: 1. Stresses greater than the above listed maximum values may result in damage to the device.

LC322271J, M, T-70/80

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	min	typ	max	Unit	Note
Power supply voltage	V _{CC}	4.5	5.0	5.5	V	2
Input high level voltage	V _{IH}	2.4		6.5	V	2
Input low level voltage (A0 to A7, A8R, RAS, CAS, UW, LW, OE)	V _{IL}	-1.0*		+0.8	V	2
Input low level voltage (I/O1 to I/O16)	V _{IL}	-0.5*		+0.8	V	2

Note: 2. All voltages are referenced to V_{SS}.
*: -2.0 V when pulse width is less than 20 ns.

DC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5 V ± 10%

Parameter	Symbol	Conditions	LC322271J, M, T				Unit	Note
			-70		-80			
			min	max	min	max		
Operating current (Average current during operation)	I _{CC1}	RAS, CAS, address cycling: t _{RC} = t _{RC} min		125		115	mA	3, 4, 5
Standby current	I _{CC2}	RAS = CAS = V _{IH}		2		2	mA	
RAS-only refresh current	I _{CC3}	RAS cycling, CAS = V _{IH} : t _{RC} = t _{RC} min		125		115	mA	3, 5
Fast page mode current	I _{CC4}	RAS = V _{IL} , CAS, address cycling: t _{PC} = t _{PC} min		115		90	mA	3, 4, 5
Standby current	I _{CC5}	RAS = CAS = V _{CC} - 0.2 V		1		1	mA	
CAS-before-RAS refresh current	I _{CC6}	RAS, CAS cycling: t _{RC} = t _{RC} min		125		115	mA	3
Input leakage current	I _{IL}	0 V ≤ V _{IN} ≤ 6.5 V, pins other than test pin = 0 V	-10	+10	-10	+10	μA	
Output leakage current	I _{OL}	D _{OUT} disable, 0 V ≤ V _{OUT} ≤ 5.5 V	-10	+10	-10	+10	μA	
Output high level voltage	V _{OH}	I _{OUT} = -2.5 mA	2.4		2.4		V	
Output low level voltage	V _{OL}	I _{OUT} = 2.1 mA		0.4		0.4	V	

Note: 3. All current values are measured at minimum cycle rate. Since current flows immoderately, if cycle time is longer than shown here, current value becomes smaller.
4. I_{CC1} and I_{CC4} are dependent on output loads. Maximum values for I_{CC1} and I_{CC4} represent values with output open.
5. Address change is less than or equal to one time during RAS = V_{IL}. Concerning I_{CC4}, it is less than or equal to one time during 1 cycle (t_{PC}).

AC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5 V ± 10% (Notes 6, 7 and 8)

Parameter	Symbol	-70		-80		Unit	Note
		min	max	min	max		
Random read, write cycle time	t _{RC}	130		150		ns	
Read-write/read-modify-write cycle time	t _{RWC}	190		200		ns	
Fast page mode cycle time	t _{PC}	45		55		ns	
Fast page mode read-write/read-modify-write cycle time	t _{PRWC}	95		100		ns	
RAS access time	t _{RAC}		70		80	ns	9, 14, 15
CAS access time	t _{CAC}		20		30	ns	9, 14
Column address access time	t _{AA}		35		45	ns	9, 15
CAS precharge access time	t _{CPA}		40		50	ns	9
Output low-impedance time from CAS low	t _{CLZ}	0		0		ns	9
Output buffer turn-off delay time	t _{OFF}	0	20	0	20	ns	10
Rise, fall time	t _T	3	50	3	50	ns	
RAS precharge time	t _{RP}	50		60		ns	
RAS pulse width	t _{RAS}	70	10000	80	10000	ns	
RAS pulse width for fast page mode cycle only	t _{RASP}	70	100000	80	100000	ns	

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Parameter	Symbol	-70		-80		Unit	Note
		min	max	min	max		
RAS hold time	t _{RS} H	20		30		ns	
CAS hold time	t _{CS} H	70		80		ns	
CAS pulse width	t _{CAS}	20	10000	30	10000	ns	
RAS to CAS delay time	t _{RCD}	25	50	25	50	ns	14
RAS to column address delay time	t _{RAD}	17	35	17	35	ns	15
CAS to RAS precharge time	t _{CRP}	10		10		ns	
CAS precharge time	t _{CP}	10		10		ns	
Row address setup time	t _{ASR}	0		0		ns	
Row address hold time	t _{RAH}	12		12		ns	
Column address setup time	t _{ASC}	0		0		ns	
Column address hold time	t _{CAH}	15		20		ns	
Column address hold time referenced to RAS	t _{AR}	50		60		ns	
Column address to RAS lead time	t _{RAL}	40		45		ns	
Read command setup time	t _{RCS}	0		0		ns	
Read command hold time referenced to CAS	t _{RCH}	0		0		ns	11
Read command hold time referenced to RAS	t _{RRH}	0		0		ns	11
Write command hold time	t _{WCH}	15		15		ns	
Write command hold time referenced to RAS	t _{WCR}	50		60		ns	
Write command pulse width	t _{WP}	15		15		ns	
Write command to RAS lead time	t _{RWL}	25		25		ns	
Write command to CAS lead time	t _{CWL}	20		20		ns	
Data input setup time	t _{DS}	0		0		ns	12
Data input hold time	t _{DH}	15		20		ns	12
Data input hold time referenced to RAS	t _{DHR}	50		60		ns	
Refresh time	t _{REF}		8		8	ms	
Write command setup time	t _{WCS}	0		0		ns	13
CAS to UW, LW delay time	t _{CWD}	50		50		ns	13
RAS to UW, LW delay time	t _{RWD}	100		100		ns	13
Column address to UW, LW delay time	t _{AWD}	65		65		ns	13
CAS precharge UW, LW delay time for fast page mode cycle only	t _{CPWD}	70		70		ns	13
CAS setup time for CAS-before-RAS	t _{CSR}	10		10		ns	
CAS hold time for CAS-before-RAS	t _{CHR}	15		15		ns	
RAS precharge CAS active time	t _{RPC}	10		10		ns	
CAS precharge time for CAS-before-RAS counter test	t _{CPT}	40		40		ns	
RAS hold time referenced to OE	t _{ROH}	15		15		ns	
OE access time	t _{OEA}		20		25	ns	9
OE delay time	t _{OED}	15		15		ns	
OE output buffer turn-off delay time	t _{OEZ}	0		0	15	ns	10
OE command hold time	t _{OEH}	20		20		ns	
Data input to CAS delay time	t _{DZC}	0		0		ns	16
Data input to OE delay time	t _{DZO}	0		0		ns	16
Masked write setup time	t _{MCS}	0		0		ns	
Masked write hold time referenced to RAS	t _{MRH}	0		0		ns	
Masked write hold time referenced to CAS	t _{MCH}	0		0		ns	

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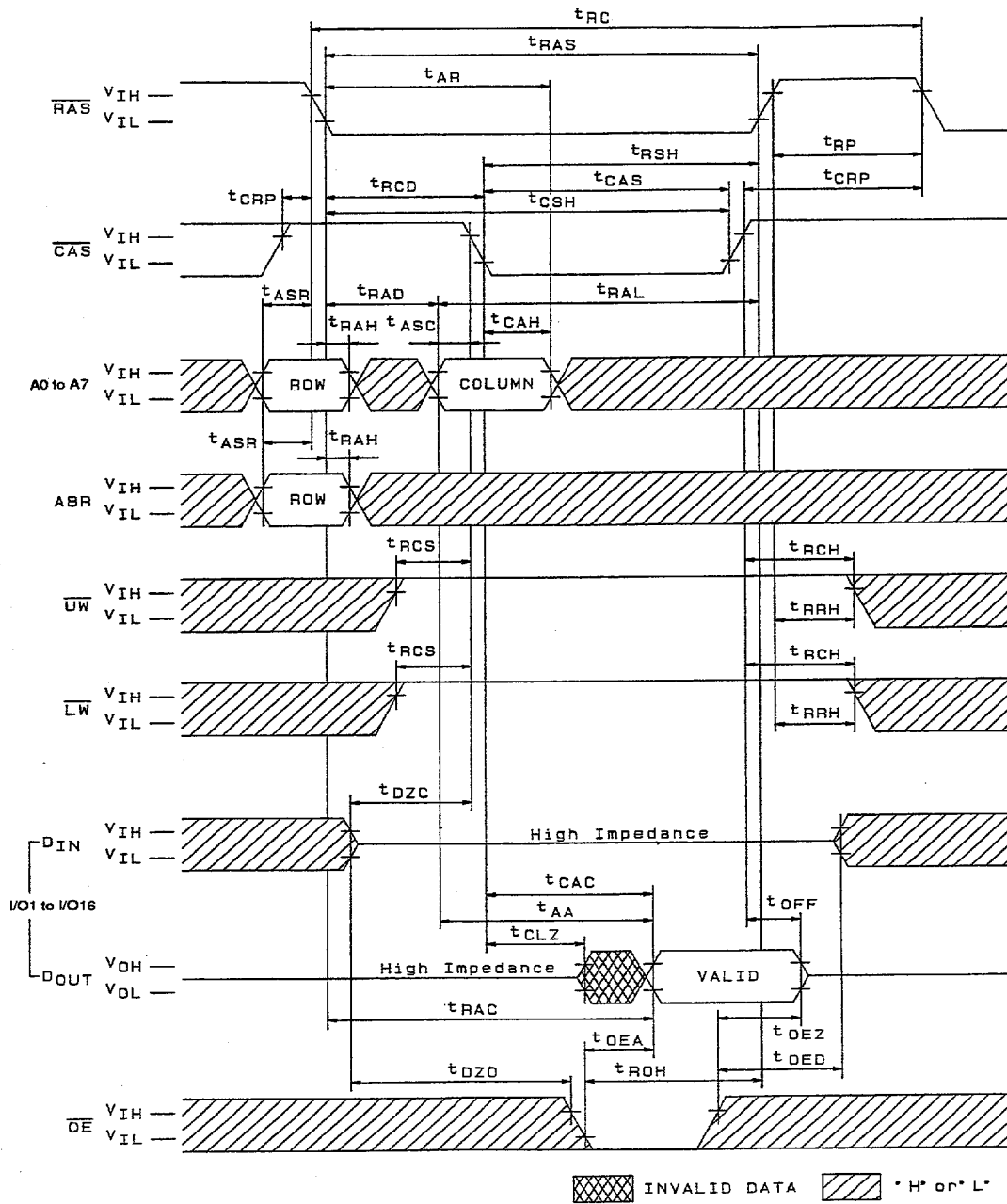
Input/Output Capacitance at $T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5\text{ V} \pm 10\%$

Parameter	Symbol	min	max	Unit	Note
Input capacitance (A0 to A7, A8R, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{UW}}$, $\overline{\text{LW}}$, $\overline{\text{OE}}$)	C_{IN}		7	pF	
Input/Output capacitance (I/O1 to I/O16)	C_{IO}		7	pF	

- Note:
6. An initial pause of 200 μs is required after power-up followed by eight $\overline{\text{RAS}}$ -only refresh cycles before proper device operation is achieved. In case of using refresh counter, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles instead of eight $\overline{\text{RAS}}$ -only refresh cycles are required.
 7. Measured at $t_r = 5\text{ ns}$.
 8. When measuring input signal timing, V_{IH} (min) and V_{IL} (max) are used for reference points. In addition, rise and fall time are defined between V_{IH} and V_{IL} .
 9. Measured using an equivalent of 50 pF and one standard TTL loads.
 10. t_{OFF} (max) and t_{OEZ} (max) are defined as the time until output voltage can no longer be measured when output switches to a high impedance condition.
 11. Operation is guaranteed if either t_{RRH} or t_{RCH} is satisfied.
 12. These parameters are measured from the falling edge of $\overline{\text{CAS}}$ for an early-write cycle, and from the falling edge of $\overline{\text{UW}}$ and $\overline{\text{LW}}$ for a read-write/read-modify-write cycle.
 13. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters for memory in that they specify the operating mode. If $t_{\text{WCS}} \geq t_{\text{WCS}}$ (min), the cycle switches to an early-write cycle and output pins switch to high impedance throughout the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}$ (min), $t_{\text{RWD}} \geq t_{\text{RWD}}$ (min), $t_{\text{AWD}} \geq t_{\text{AWD}}$ (min) and $t_{\text{CPWD}} \geq t_{\text{CPWD}}$ (min) for fast page mode cycle only, the cycle switches to a read-write/read-modify-write cycle and data output equal information in the selected cells. If neither of the above timings are satisfied, output pins are in an undefined state.
 14. t_{RCD} (max) is not a restrictive operating parameter but instead represents the point at which the access time t_{RAC} (max) is guaranteed. If $t_{\text{RCD}} \geq t_{\text{RCD}}$ (max), access time is determined according to t_{CAC} .
 15. t_{RAD} (max) is not a restrictive operating parameter but instead represents the point at which the access time t_{RAC} (max) is guaranteed. If $t_{\text{RAD}} \geq t_{\text{RAD}}$ (max), access time is determined according to t_{AA} .
 16. Operation is guaranteed if either t_{DZC} or t_{DZO} is satisfied.

Timing Chart

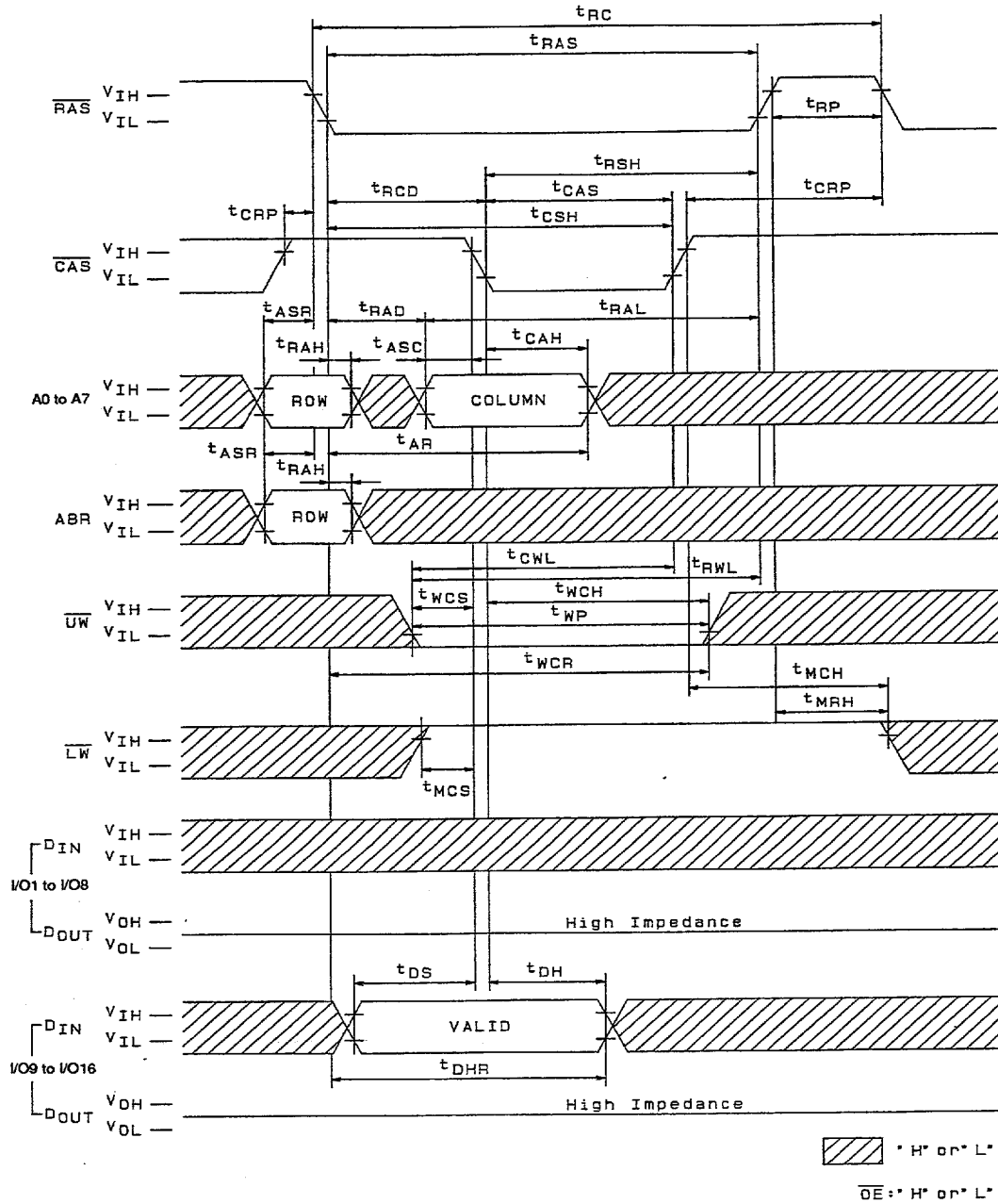
Read Cycle



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Upper Byte Early Write Cycle



A02909



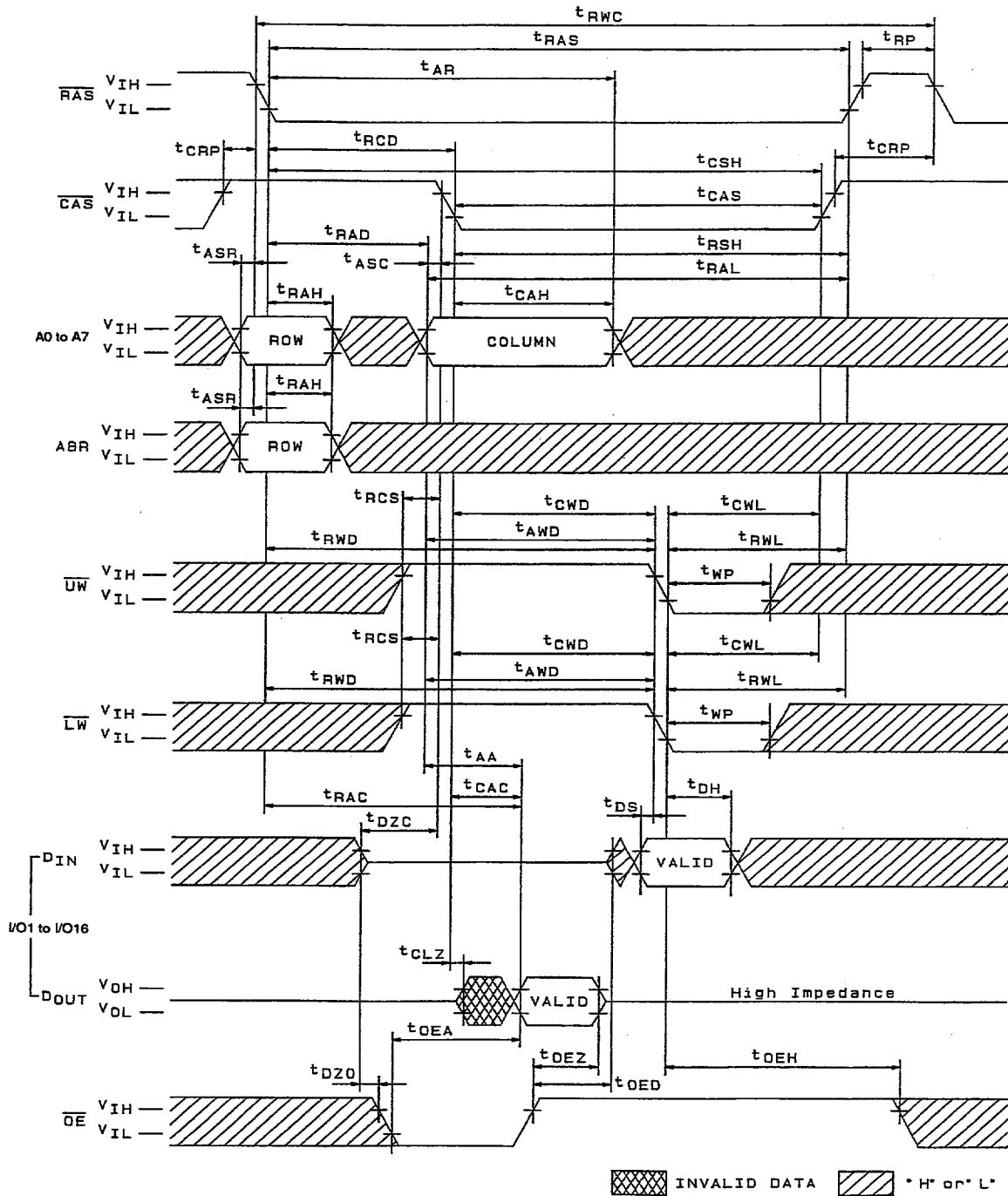
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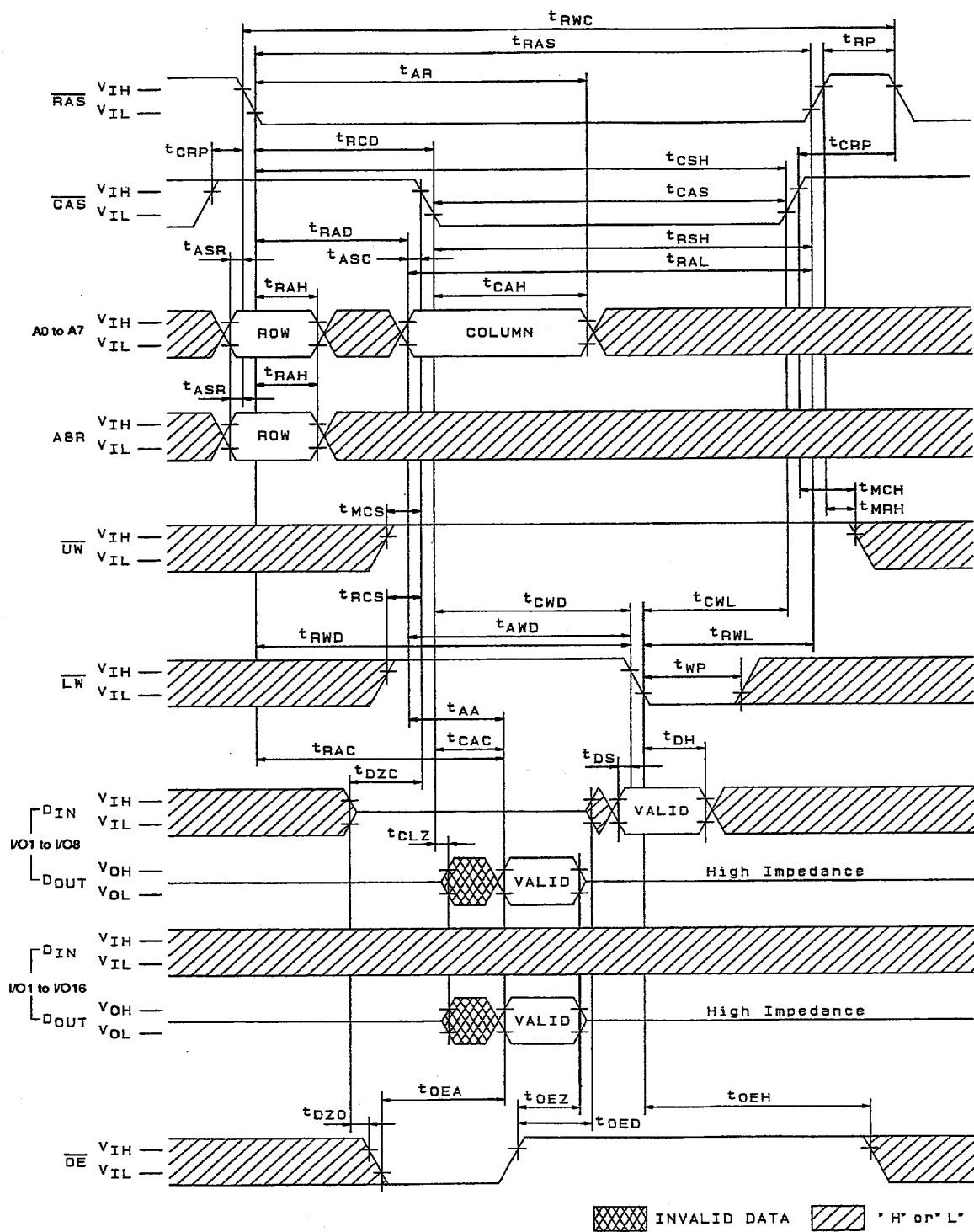


Read-Modify-Write Cycle



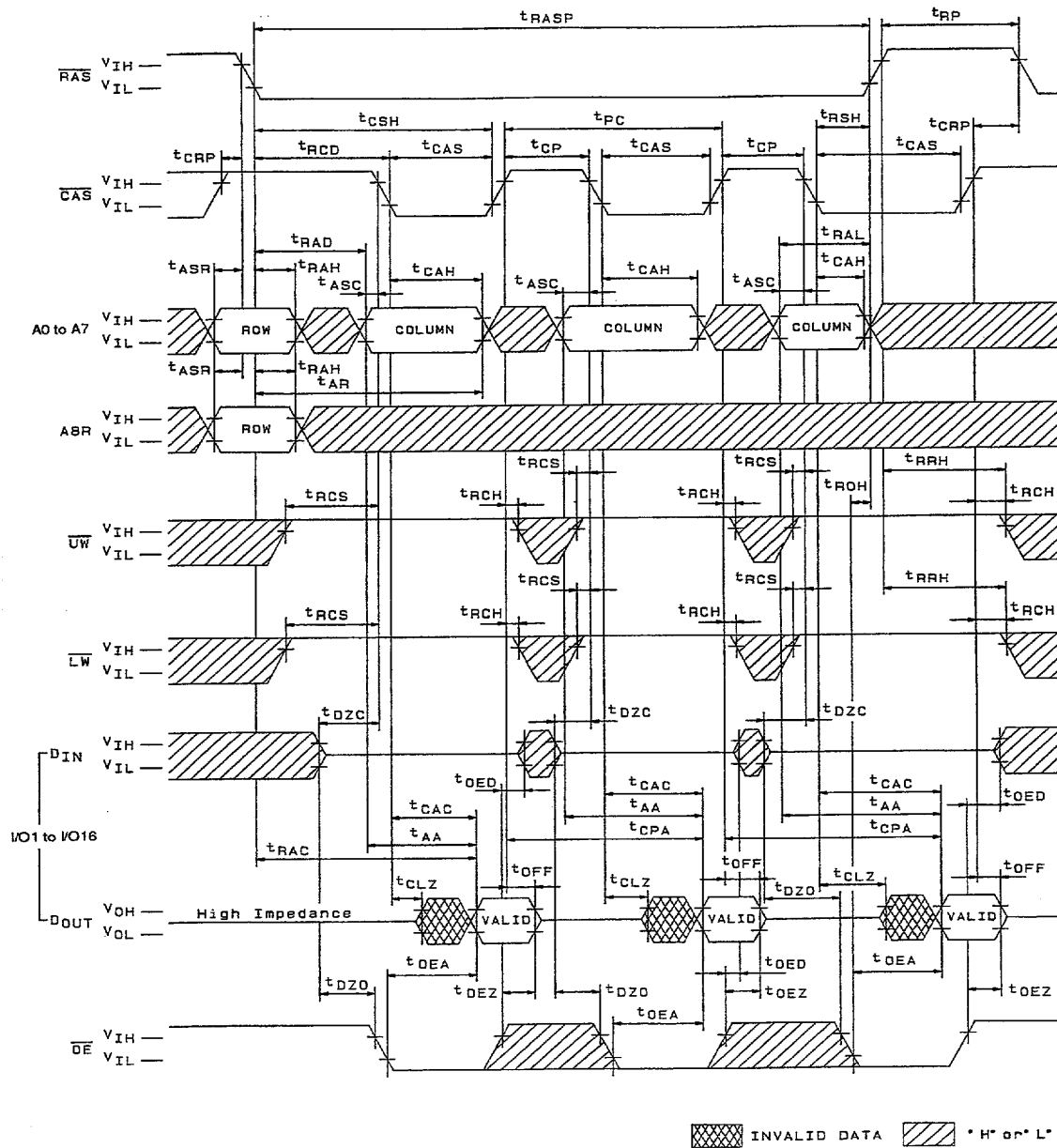
A02914

Read-Modify Lower Byte Write Cycle



A02916

Fast Page Mode Read Cycle



A02917





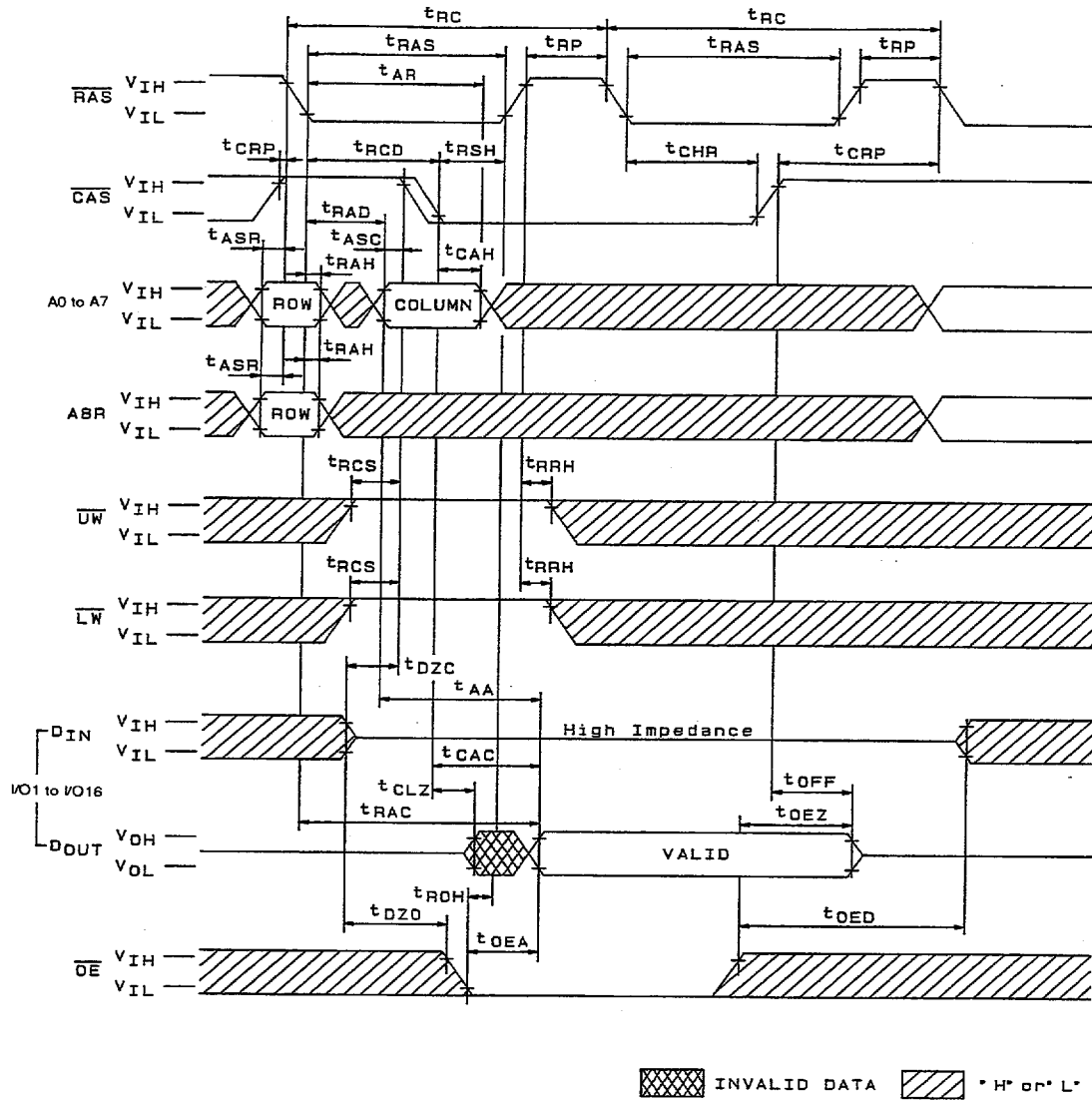






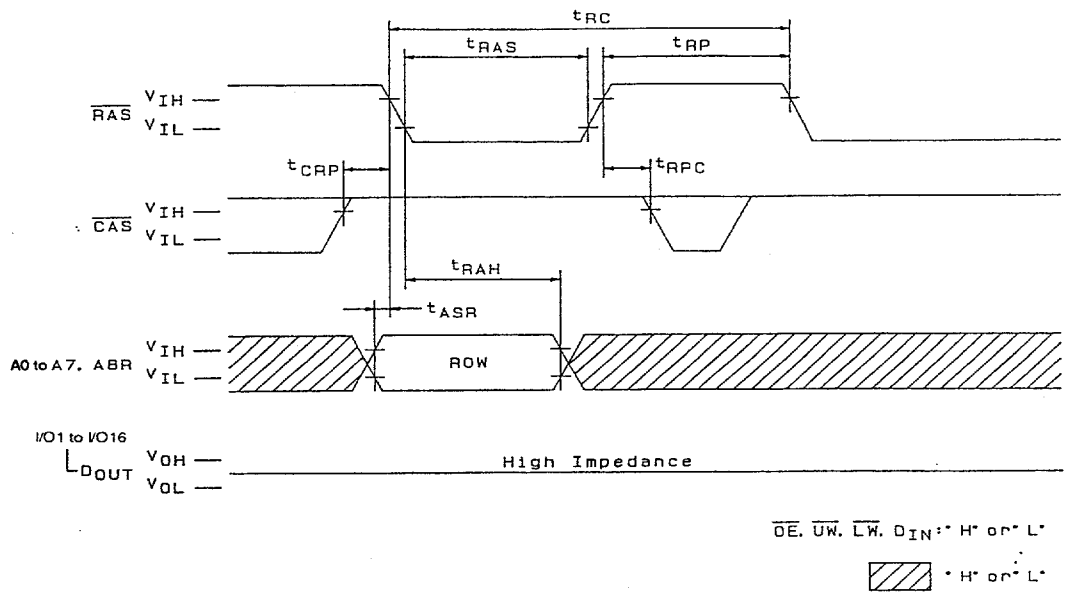


Hidden Refresh Cycle



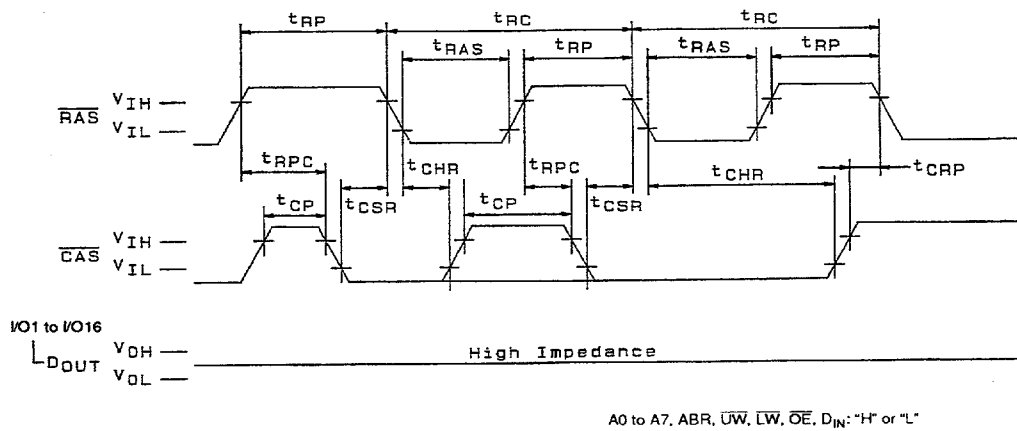
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RAS-Only Refresh Cycle



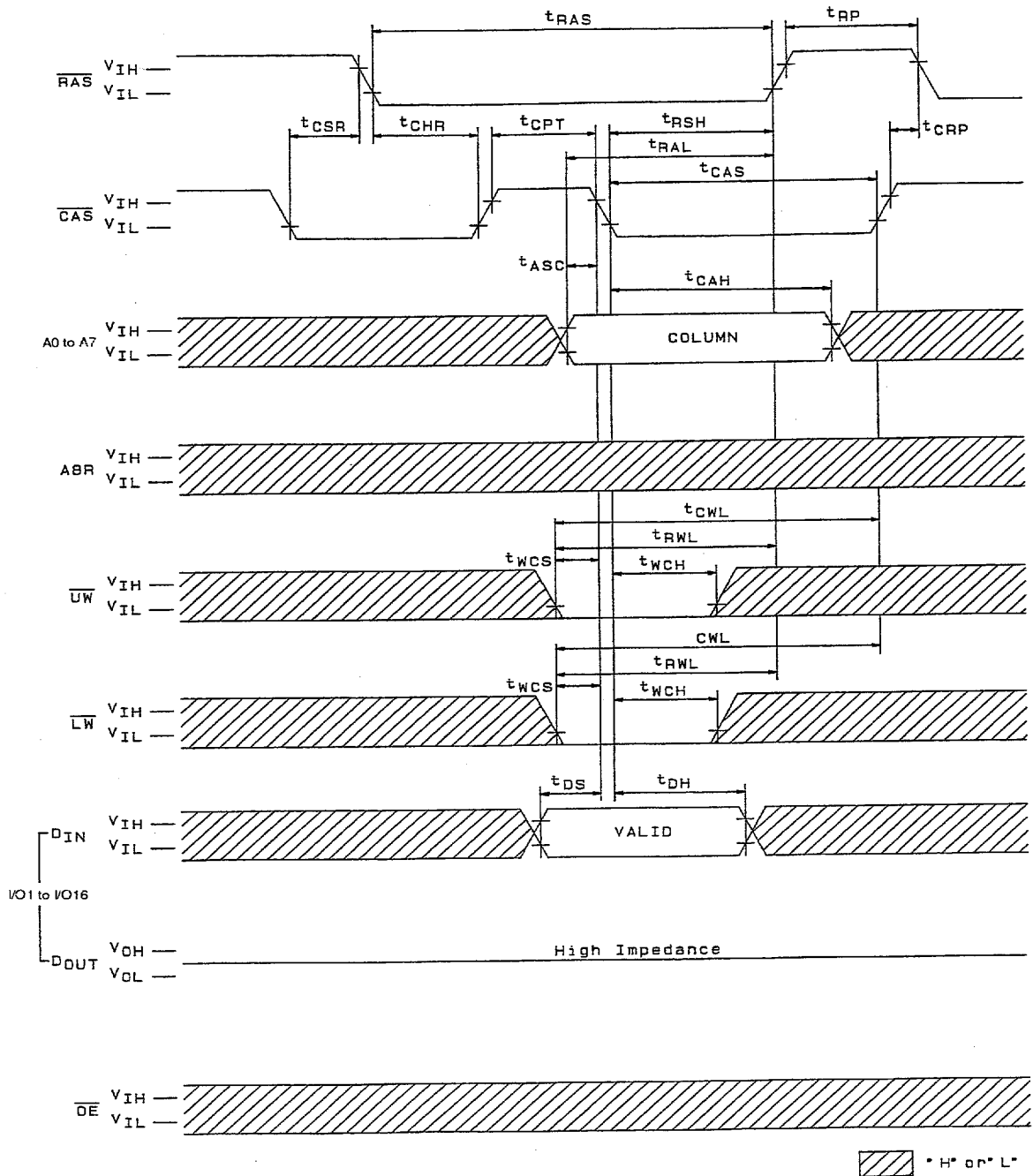
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CAS-Before-RAS Refresh Cycle



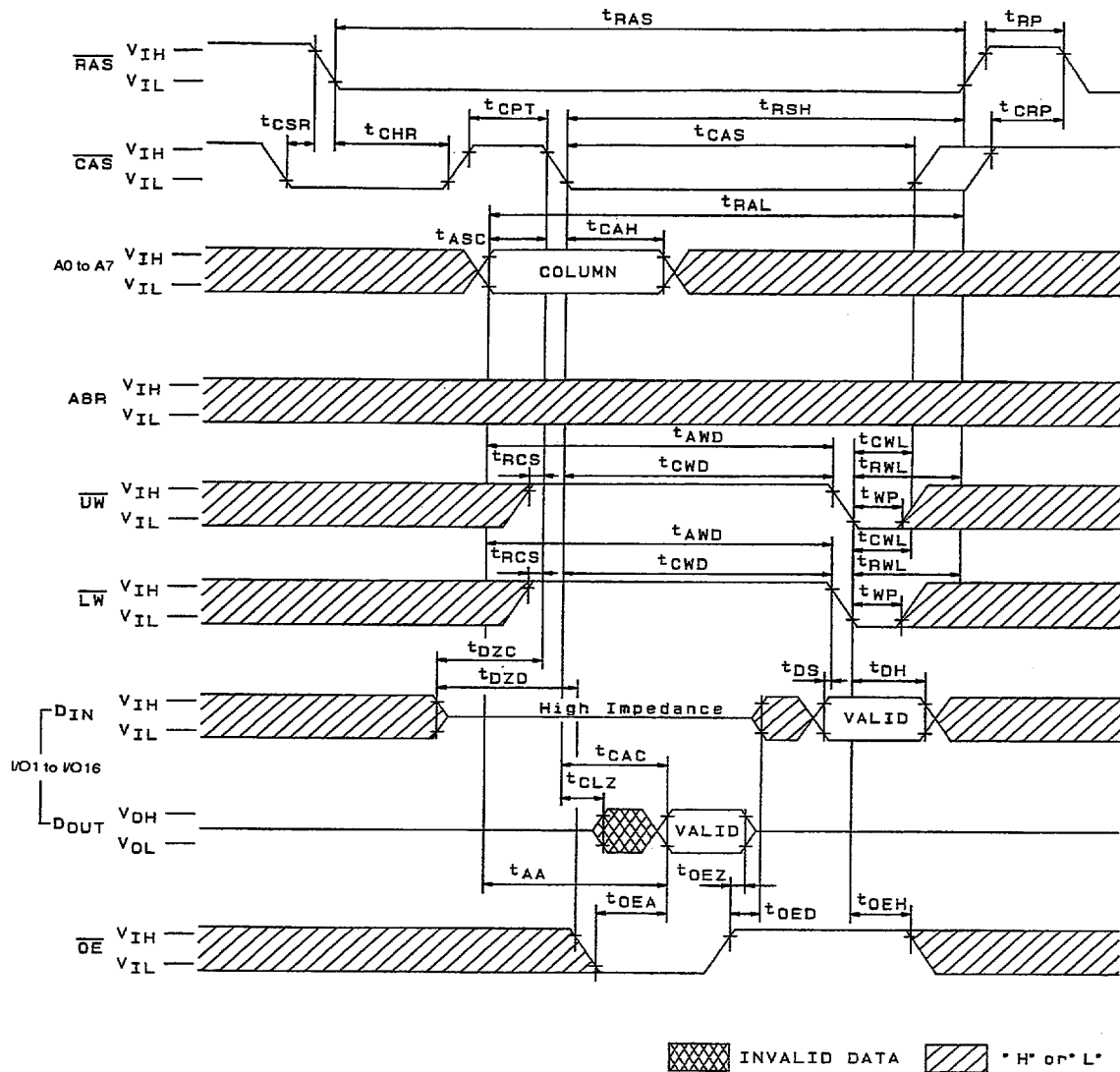
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CAS-Before-RAS Refresh Counter Test Cycle (Write)



A0292B

CAS-Before-RAS Refresh Counter Test Cycle (Read-Modify-Write)



A02929