HOLTEK

HT6116-7LL
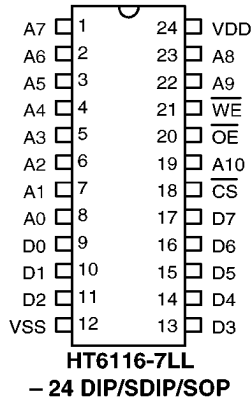## CMOS 2K×8-Bit SRAM

Features

- Single 5V power supply
- Low power consumption
  - Operating: 180mW (Typ.)
  - Standby: 5µW (Typ.)
- 70ns (Max.) high speed access time
- Power down by pin $\overline{CS}$
- Memory expansion by pin $\overline{OE}$
- Common I/O using tri-state outputs
- TTL compatible interface levels
- Fully static operation
- Pin-compatible with standard 2K×8 bits of EPROM/MASK ROM
- 24-pin DIP/SDIP/SOP package
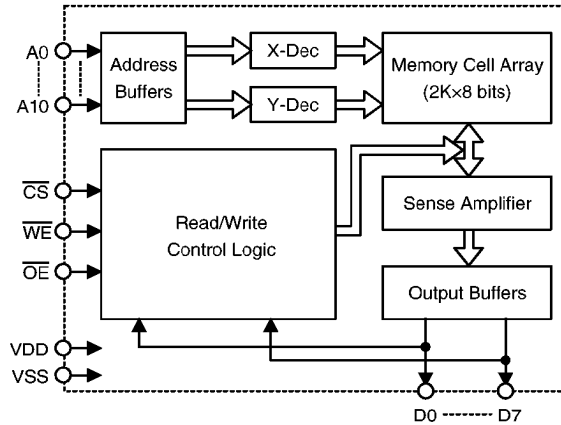
General Description

The HT6116-7LL is a 16,384-bit static random access memory organized as 2048 words by 8 bits and operates from a single 5-volt power supply. It is built with HOLTEK's high performance CMOS 0.8µm SPDM process. Six-transistor full CMOS memory cell provides low standby current and high-reliability. Inputs and tri-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Pin Assignment

A7	1	24 VDD
A6	2	23 A8
A5	3	22 A9
A4	4	21 $\overline{WE}$
A3	5	20 $\overline{OE}$
A2	6	19 A10
A1	7	18 $\overline{CS}$
A0	8	17 D7
D0	9	16 D6
D1	10	15 D5
D2	11	14 D4
VSS	12	13 D3

HT6116-7LL
− 24 DIP/SDIP/SOP

Block Diagram

Pin Description

Pin No.	Pin Name	I/O	Description
1~8, 19, 22, 23	A0~A10	I	Address input pins
21	$\overline{WE}$	I	Write enable signal pin
20	$\overline{OE}$	I	Output enable signal pin
18	$\overline{CS}$	I	Chip select signal pin
9~11, 13~17	D0~D7	I/O	Data input and output signal pins
24	VDD	I	Positive power supply
12	VSS	I	Negative power supply

Absolute Maximum Ratings*

VDD to GND ....–0.3V to +7.0V

IN, IN/OUT Voltage to GND, V_T ....–0.3V to V_{CC}+0.5V

Operating Temperature, T_{opr} ....–40°C to +85°C

Storage Temperature (Plastic), T_{stg} ....–55°C to +125°C

Temperature Under Bias, T_{bias} ....–10°C to +85°C

Power Dissipation, P_T 1.0W

* Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(V_{DD}=5V±10%, GND=0V, Ta=–40°C to 85°C)

Symbol	Parameter		Min.	Typ.*	Max.	Unit
V_{DD}	Operating Voltage	—	4.5	5.0	5.5	V
I_{DD1}	Operating Current	T_{CYC}=Min. Cycle, I_{OUT}=0mA	—	—	45	mA
I_{DD2}		T_{CYC}=1μs, $I_{I/O}$=0mA			15	
I_{SB1}	Standby Current	$\overline{CS}$=V_{IH}	—	—	10	mA
I_{SB2}		$\overline{CS}$>=V_{DD}-0.2V, V_{IN}>=V_{DD}-0.2V or V_{IN}<=0.2V			50	μA
V_{OL}	Output Low Voltage	I_{OL}=4mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH}=–1.0mA	2.4	—	—	V
V_{IL}	Input Low Voltage	—	–0.3	—	0.8	V

Symbol	Parameter		Min.	Typ.*	Max.	Unit
V_{IH}	Input High Voltage	—	2.2	—	V_{DD}+0.3	V
I_{LI}	Input Leakage Current	V_{DD}=5.5V, V_{IN}=GND to V_{DD}	—	—	1	μA
I_{LO}	Output Leakage Current	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH}, V_{OUT}=GND to V_{DD}	—	—	1	μA

*V_{DD}=5V, Ta=25°C

A.C. Characteristics

(V_{DD}=5V±10%, Ta=–40°C to 85°C)

Read cycle

Symbol	Item	Min.	Typ.	Max.	Unit
t_{RC}	Read Cycle Time	70	—	—	ns
t_{AA}	Address Access Time	—	—	70	ns
t_{ACS}	Chip Select Access Time	—	—	70	ns
t_{OE}	Output Enable to Output Valid	—	—	40	ns
t_{OH}	Outputs Hold from Address Change	5	—	—	ns
t_{CLZ}	Chip Select to Outputs in Low Z	10	—	—	ns
t_{OLZ}	Output Enable to Outputs in Low Z	10	—	—	ns
t_{CHZ}	Chip Disable to Outputs in High Z	0	—	30	ns
t_{OHZ}	Output Disable to Outputs in High Z	0	—	30	ns

Note: 1. A read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$

2. t_{CHZ} and t_{OHZ} are specified by the time when data out is floating

Write cycle

Symbol	Item	Min.	Typ.	Max.	Unit
t_{WC}	Write Cycle Time	70	—	—	ns
t_{CW}	Chip Select to End of Write	35	—	—	ns
t_{AW}	Address Valid to End of Write	50	—	—	ns
t_{AS}	Address Setup Time	0	—	—	ns
t_{WP}	Write Pulse Width	25	—	—	ns
t_{WR}	Write Recovery Time	0	—	—	ns
t_{DW}	Data to Write Time Overlap	20	—	—	ns
t_{DH}	Data Hold from Write Time	0	—	—	ns
t_{OW}	Outputs active from End of Write	5	—	—	ns

| Symbol	Item	Min.	Typ.	Max.	Unit
t_{OHZ}	Output Disable to Outputs in High Z	0	—	40	ns
t_{WHZ}	Write to Outputs in High Z	0	—	50	ns

Note: 1. A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$
     2. $\overline{OE}$ may be both high and low in a write cycle
     3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last
     4. t_{WP} is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$
     5. t_{WR}, t_{DW} and t_{DH} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first
     6. t_{WHZ} is specified by the time when DATA OUT is floating, not defined by output level
     7. When I/O pins are data output mode, don't force inverse signals to those pins

A.C. Test Conditions

Item	Condition
Input Pulse Level	0V to 3V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
Output Load	See Figures below
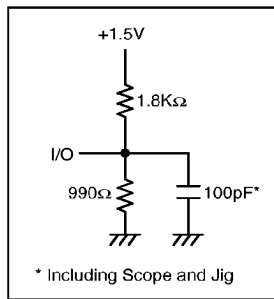
Output Load
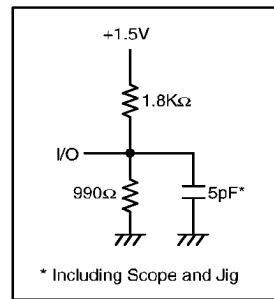
Output Load for
t_{CLZ}, t_{OLZ}, t_{OHZ}, t_{WHZ} and t_{OW}
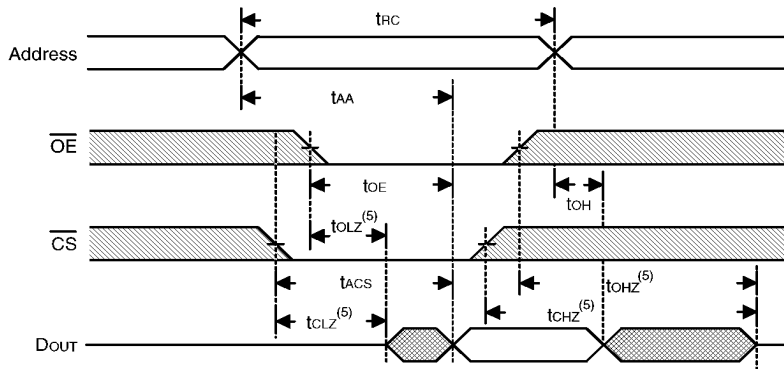
Operation Truth Table

All relations between $\overline{WE}$, $\overline{OE}$ and $\overline{CS}$ can be described as the following truth table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	D0~D7
H	X*	X	Standby	High-Z
L	L	H	Read	Dout
L	H	H	Read	High-Z
L	X	L	Write	Din

* X: Don't Care, Logical High or Low

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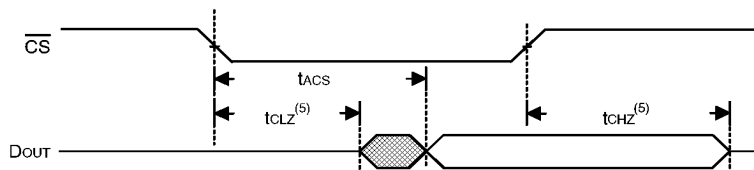
Timing Diagrams
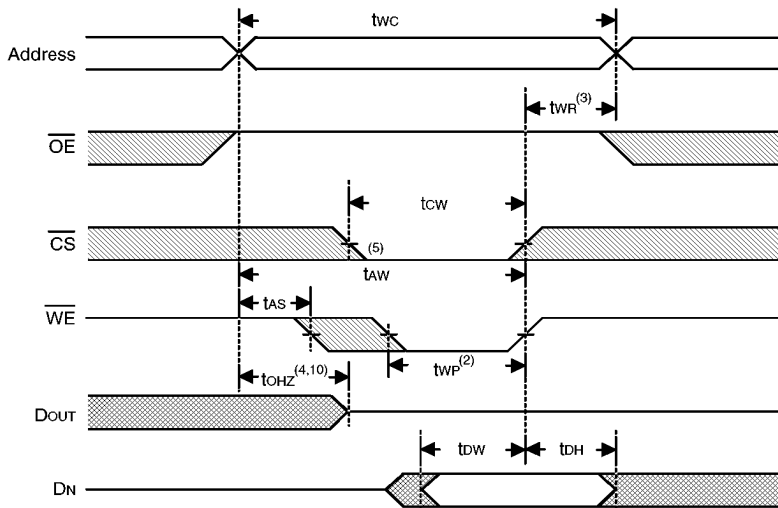
Read cycle 1 [1]
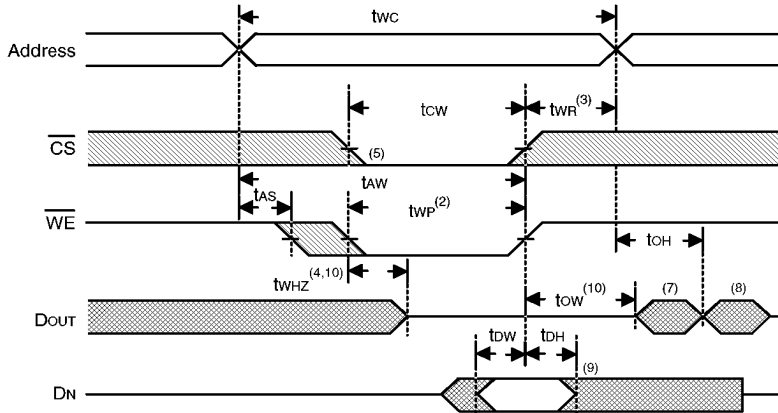

Read cycle 2 [1, 2, 4]
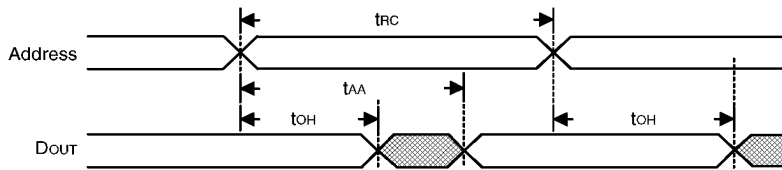
Read cycle 3 [1, 3, 4]

Notes: (1) $\overline{WE}$ is high for Read cycle

(2) Device is continuously enabled, $\overline{CS}=V_{IL}$

(3) Address is valid prior to or coincident with the $\overline{CS}$ transition low.

(4) $\overline{OE}=V_{IL}$

(5) Transition is measured±500mV from the steady state.

Write cycle 1 [(1)]

Write cycle 2 [(1, 6)]

Notes: (1) $\overline{WE}$ must be high during all address transitions.

(2) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

(3) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.

(4) During this period, I/O pins are in the output state, so the input signals of the opposite phase to the outputs must not be applied.

(5) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.

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(6) $\overline{OE}$ is continuously low ($\overline{OE}$=V$_{IL}$).

(7) D$_{OUT}$ is at the same phase of the write data of this write cycle.

(8) D$_{OUT}$ is the read data of the next address.

(9) If $\overline{CS}$ is low during this period, I/O pins are in the output state; then the data input signals of the opposite phase to the outputs must not be applied to them.

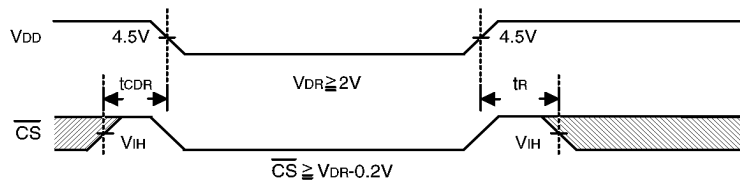(10) Transition is measured $\pm$ 500mV from the steady state.

Data Rentention Characteristics

(Ta=–40°C to 85°C)

Symbol	Parameter	Conditions	Min.	Max.	Unit
V$_{DR}$	V$_{DD}$ for Data Retention	$\overline{CS}$ ≥ V$_{DD}$-0.2V	2	5.5	V
I$_{CCDR}$	Data Retention Current	V$_{DD}$=3V, $\overline{CS}$ ≥ V$_{DD}$-0.2V V$_{IN}$ ≥ V$_{DD}$-0.2V or V$_{IN}$ ≤ 0.2V	—	50	μA
t$_{CDR}$	Chip Disable Data Retention Time	See Retention Timing	0	—	ns
t$_R$	Operation Recovery Time	See Retention Timing	t$_{RC}$*	—	ns

*t$_{RC}$=Read Cycle Time

Low V$_{DD}$ Data Retention Timing

Characteristic Curves

I_{DD} vs V_{DD} (Ta=25°C)

I_{DD} vs Ta (V_{DD}=5V)

I_{STB} vs V_{DD} (Ta=25°C)

I_{STB} vs Ta (V_{DD}=5V)

t_{AA} vs V_{DD} (Ta=25°C)

t_{AA} vs Ta (V_{DD}=5V)

Access Time t_{ACS} (Normalized)

t_{ACS} vs V_{DD} (Ta=25°C)

Supply Voltage V_{DD} (V)

t_{ACS} vs Ta (V_{DD}=5V)

Access Time t_{ACS} (Normalized)

Ambient Temperature Ta (°C)

t_{OE} vs V_{DD} (Ta=25°C)

Access Time t_{OE} (Normalized)

Supply Voltage V_{DD} (V)

t_{OE} vs Ta (V_{DD}=5V)

Access Time t_{OE} (Normalized)

Ambient Temperature Ta (°C)

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