4M (512K x 8-bit) Flash Memory

■ DESCRIPTION

The Hitachi HN28F4001 is a 4-Megabit CMOS Flash Memory organized as 524,288 x 8-bit. The HN28F4001 is capable of in-system electrical chip and block erasure and reprogramming.

The HN28F4001 programs and erases data with a 12 V V_{PP} supply and a 5 V V_{CC} supply. The HN28F4001 conforms to the JEDEC Standard Dual-Supply EEPROM Command Set. Its Automatic Commands do not require complicated external control to program or erase data because of its automatic verify programming, chip erase and block erase functions.

The block architecture of the HN28F4001 segments the device into 32 blocks of 16KBytes each. This feature allows the user to erase and reprogram one random block of data and more than one block of data simultaneously.

Hitachi's HN28F4001 is offered in JEDEC-Standard Byte-Wide EPROM pinouts in 32-lead SOP and TSOP packages. This allows an easy upgrade from the HN28F101, 1 Megabit Flash Memory, as well as socket replacement with Mask ROMs. The HN28F4001 TSOP is offered in both standard and reverse bend pinouts.

■ FEATURES

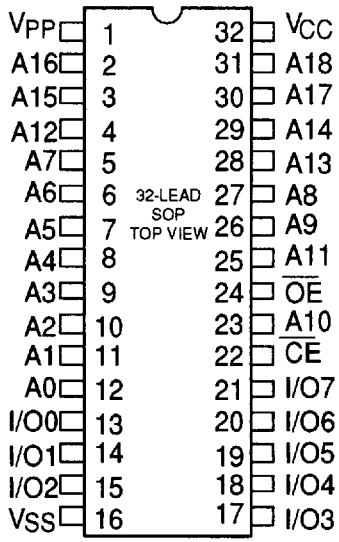
- Dual Power Supply:
  - V_{CC} = 5 V ± 10%
  - V_{PP} = 12.0 V ± 0.6 V (Erase/Program)
- Fast Access Times:
  - 150 ns/170 ns (max)
- Low Power Dissipation:
  - Read Current: 15 mA (typ)
  - Standby Current: 1 µA (typ)
- Automatic Byte Programming:
  - Programming Time: 40 µs/Byte (typ)
  - Address, Data, Control Latch Function
  - Internal Automatic Program Verify
  - Data Polling Function
- Automatic Chip and Block Erase:
  - Erase Time: 4 sec (typ)
  - Internal Pre-Write and Erase Verify
  - Status Polling Function
- Block Architecture:
  - Block Size: 16KBytes x 32 Blocks
  - Simultaneous Erase of Multiple Blocks
- Erase Endurance:
  - 10,000 times (min)
- Pin Arrangement:
  - JEDEC Standard Byte-Wide EPROM
  - Mask ROM Compatible
- Packages:
  - 32-lead Plastic SOP
  - 32-lead Plastic TSOP (Type I)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN28F4001FP-15	150 ns	32-lead Plastic SOP
HN28F4001FP-17	170 ns	(FP-32D)
HN28F4001T-15	150 ns	32-lead Plastic TSOP
HN28F4001T-17	170 ns	(TFP-32D)
HN28F4001R-15	150 ns	32-lead Plastic TSOP
HN28F4001R-17	150 ns	(TFP-32DR)
		Reverse bend

■ PIN ARRANGEMENT

HN28F4001FP Series



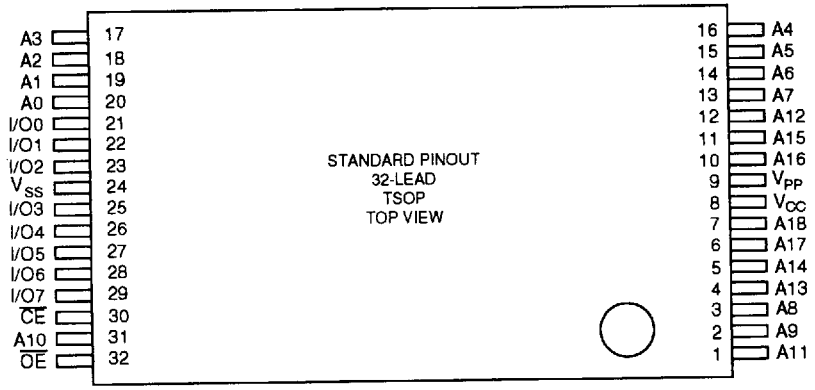
(PinD32.HN28F4001)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{18}	Address
I/O_0 - I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground

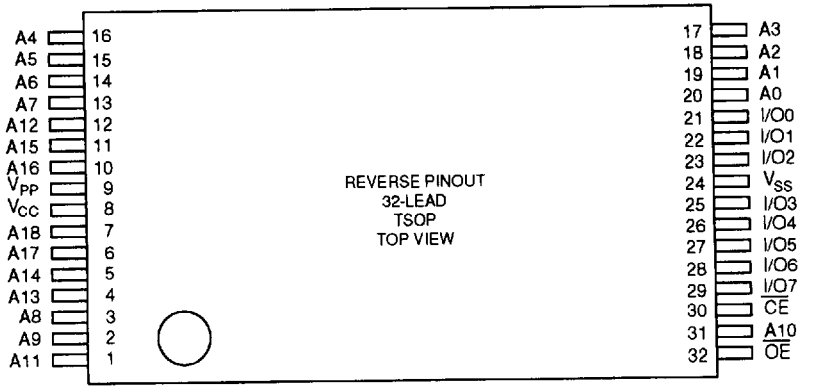
■ PIN ARRANGEMENT (continued)

HN28F4001T Series



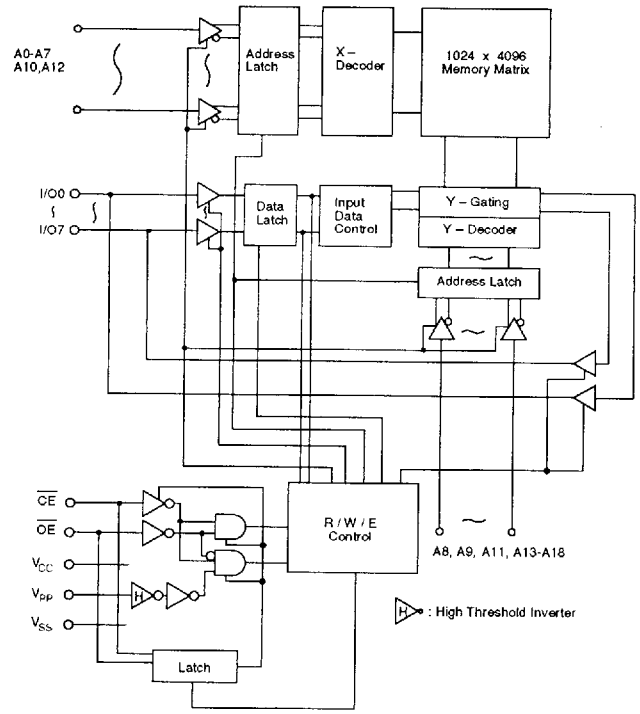
(PinT132.HN28F4001T)

HN28F4001R Series



(PinT132.HN28F4001R)

■ BLOCK DIAGRAM



(BD.HN28F4001)

■ MODE SELECTION

Mode		$\overline{CE}$	$\overline{OE}$	A_9	A_0	V_{PP}	I/O_0 to I/O_7
Read	Read	V_{IL}	V_{IL}	A_9	A_0	V_{SS} to V_{cc} [6]	D_{OUT}
	Output Disable	V_{IL}	V_{IH}	X	X	V_{SS} to V_{cc}	High-Z
	Standby	V_{IH}	X	X	X	V_{SS} to V_{cc}	High-Z
	Identifier [1]	V_{IL}	V_{IL}	V_H [2]	V_{IL}	V_{SS} to V_{cc}	Code"07"
		V_{IL}	V_{IL}	V_H [2]	V_{IH}	V_{SS} to V_{cc}	Code"80"
Command Program	Read [3,5]	V_{IL}	V_{IL}	A_9	A_0	V_{PP}	D_{OUT}
	Standby	V_{IH}	X	X	X	V_{PP}	High-Z
	Write [4]	V_{IL}	V_{IH}	A_9	A_0	V_{PP}	D_{IN}

Notes:
1. Device Identifier Code can be output in Command Program Mode. Refer to Command Address and Data Input Table.
2. $11.4\ V \leq V_H \leq 12.6\ V$
3. Data can also be read when 12 V is applied to V_{PP}. Device Identifier Code can be output by Command Inputs. See Device Identifier Mode Description Table for more details.
4. Refer to Command Address and Data Input Table. Data is programmed, erased, or verified after inputting Commands.
5. Status of Programming and Erase can be verified in this mode. Status Outputs on I/O_7. I/O_0 to I/O_6 are in high impedance states.
6. X = Don't Care. $V_{PP} = 0V$ to V_{CC}.

■ COMMAND ADDRESS AND DATA INPUT

Command	Bus Cycles Required	First Cycle			Second Cycle		
		Operation Mode [1]	Address [2]	Data [3]	Operation Mode [1]	Address [2]	Data [3]
Read (Memory) [4]	1	Write	X	00H	Read	RA	D_{OUT}
Read Identifier Codes	2	Write	X	90H	Read	IA	ID
Set-up Chip Erase/ Chip Erase [5]	2	Write	X	20H	Write	X	20H
Set-up Block Erase/ Block Erase [8]	2	Write	X	60H	Write	BA	60H
Erase Verify [5]	2	Write	EVA	A0H	Read	X	EVD
Setup Auto Chip Erase/ Auto Chip Erase [6]	2	Write	X	30H	Write	X	30H
Setup Auto Block Erase/ Auto Block Erase [9]	2	Write	X	20H	Write	BA	D0H
Setup Program/Program [7]	2	Write	X	40H	Write	PA	PD
Program Verify [7]	2	Write	PA	C0H	Read	X	PVD
Setup Auto Program/ Auto Program [10]	2	Write	X	10H	Write	PA	PD
Reset	1 or 2	Write	X	FFH	Write[11]	X	FFH[11]

Notes:
1. Refer to Command Program Mode in Mode Selection about operation mode.
2. Refer to Device Identifier Mode. IA = Identifier Address, PA = Programming Address, EVA = Erase Verify Address, RA = Read Address, BA = Block Address. Addresses are latched on the rising edge of chip-enable pulse.
3. Refer to Device Identifier Mode. PA are latched by Programming Command. ID = Identifier Output Code, PD = Programming Data, PVD = Programming Verify Output Data, EVD = Erase Verify Output Data.
4. Command latch default value when applying 12 V to V_{PP} is "00H". Device is in Read Mode after V_{PP} is set to 12 V (before other Command is input).
5. All data in the chip is erased. Erase data according to the Manual Chip Erase Flowchart.
6. All data in the chip is erased. Data is automatically programmed to 00H and erased by internal logic circuitry. External Manual Erase Verify is not required. Erasure completion must be verified by Status Polling on I/O_7.
7. Program data according to the Manual Programming Flowchart.
8. Block data indicated by BA is erased. Erase data according to the Manual Block Erase Flowchart.
9. Block data indicated by BA is erased. Data is automatically programmed to 00H and erased by internal logic circuitry. External Manual Erase Verify is not required. Erasure completion must be verified by Status Polling on I/O_7.
10. One Byte of data is programmed. Data is programmed automatically by internal logic circuit. External program verify is not required. Program completion must be verified by Data Polling on I/O_7.
11. Write Reset Command twice to exit from program setup state or auto verify program setup state. Write it once to exit from others. The Reset Command is not valid during the following:
    (1) Standby time (t_{ET}) during Manual Erase.
    (2) Erase time (t_{AETC}, t_{AETB}) during Automatic Erase.
    (3) Programming time (t_{AVT}) after inputting setup command (10H) in Auto Verify Programming.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +14.0	V
A_9 Voltage [1,2]	V_{ID}	-0.6 to +13.5	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range [3]	T_{STG}	-65 to +125	°C
Storage Temperature Under Bias	T_{BIAS}	-10 to +80	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN}, V_{OUT} and V_{ID} min = -2.0V for pulse width ≤ 20 ns.
3. Device storage temperature range before programming.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Capacitance	C_{IN}	-	4	6	pF	V_{IN} = 0 V
Output Capacitance	C_{OUT}	-	10	12	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = V_{SS} to V_{CC}
Operating V_{CC} Current	I_{CC1}	-	3	30	mA	I_{OUT} = 0 mA, f = 1 MHz
	I_{CC2}	-	15	50	mA	I_{OUT} = 0 mA, f = 6.7 MHz
Standby V_{CC} Current	I_{SB1}	-	0.2	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	-	1	20	µA	$\overline{CE}$ = V_{CC} ± 0.3V
V_{PP} Current	I_{PP1}	-	1	20	µA	V_{PP} = 5.5 V
Input Voltage [3]	V_{IL}	-0.5 [1]	-	0.8 [3]	V	
	V_{IH}	2.2 [3]	-	V_{CC} + 0.5 [2]	V	
Output Voltage	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns. V_{IL} min = -2.0 V for pulse width ≤ 20 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns. If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.
3. Only defined for DC and long cycle function test. V_{IL} max = 0.4 and V_{IH} min = 3.0 V for AC function test.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

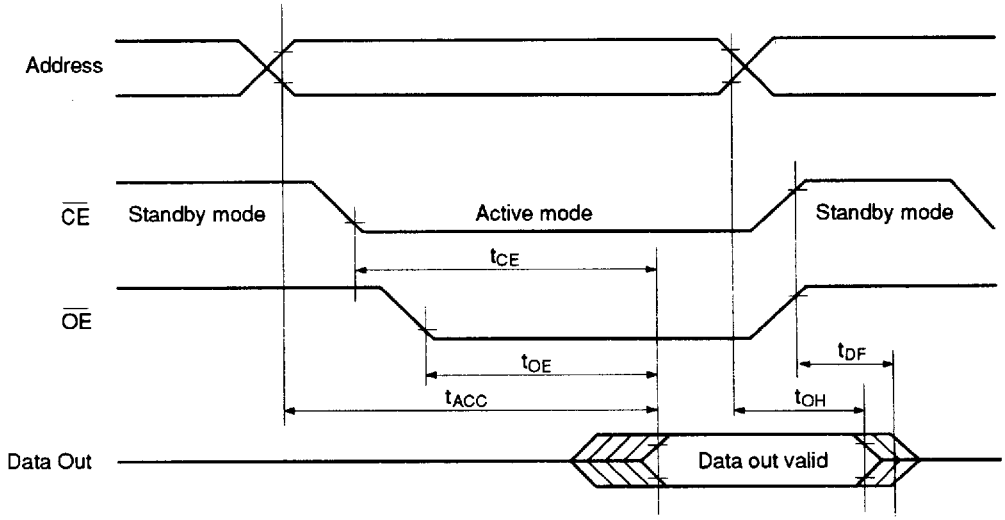
Test Conditions

- Input pulse levels: 0.4 V / 3.0 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0 V

Item	Symbol	HN28F4001-15 Min.	HN28F4001-15 Max.	HN28F4001-17 Min.	HN28F4001-17 Max.	Unit	Test Conditions
Address Access Time	t_{ACC}	-	150	-	170	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	150	-	170	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	70	-	70	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z[1]	t_{DF}	0	50	0	60	ns	$\overline{CE}$ = V_{IL} or $\overline{OE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	5	-	5	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



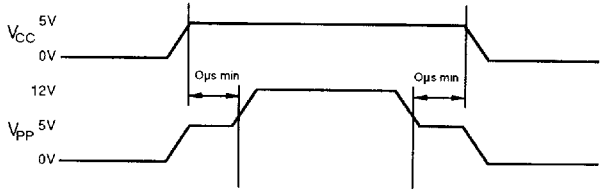
(TD.R.HN28F4001)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING AND ERASE OPERATIONS

(V_{CC} = 5V ± 10%, V_{PP} = 12.0 V ± 0.6 V, T_a = 0 to +70°C)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Leakage Current		I_{LI}	-	-	2	µA	$V_{IN} = V_{SS}$ to V_{CC}
Output Leakage Current		I_{LO}	-	-	2	µA	$V_{OUT} = V_{SS}$ to V_{CC}
Operating V_{CC} Current	Read	I_{CC1}	-	3	30	mA	I_{OUT} = 0 mA, f = 1 MHz
		I_{CC2}	-	15	50	mA	I_{OUT} = 0 mA, f = 6.7 MHz
	Program	I_{CC3}	-	7	30	mA	Programming
	Erase	I_{CC4}	-	15	30	mA	Erasing
	Program Verify	I_{CC5}	-	3	15	mA	Programming Verify
	Erase Verify	I_{CC6}	-	3	15	mA	Erase Verify
Standby V_{CC} Current		I_{SB1}	-	0.3	1	mA	$\overline{CE} = V_{IH}$
		I_{SB2}	-	40	200	µA	$\overline{CE} = V_{CC} \pm 0.3$ V
V_{PP} Current	Read	I_{PP1}	-	80	200	µA	V_{PP} = 12.6 V
	Program	I_{PP2}	-	13	50	mA	Programming
	Erase	I_{PP3}	-	40	80	mA	Automatic Erase
	Program Verify	I_{PP4}	-	1	10	mA	Programming Verify
	Erase Verify	I_{CC5}	-	0.5	10	mA	Erase Verify
Input Voltage		V_{IL}	-0.5 [5]	-	0.8 [7]	V	
		V_{IH}	2.2 [7]	-	V_{CC} + 0.5 [6]	V	
Output Voltage		V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA
		V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes: 1. V_{CC}/V_{PP} power on/off timing: V_{CC} must be applied before or simultaneously with V_{PP}, and removed after or simultaneously with V_{PP}. These conditions must be satisfied at power on and off caused by power failure to the device.



2. V_{PP} must not exceed 14 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12 V.
4. When $\overline{CE} = V_{IL}$, do not change V_{PP} from V_{IL} to 12 V or 12 V to V_{IL}.
5. V_{IL} min = -1.0 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed. Read operation can not be guaranteed.
7. Only defined for DC and long cycle function test. V_{IL} max = 0.4 and V_{IH} min = 3.0 V for AC function test.

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING AND ERASE OPERATIONS

(V_{CC} = 5V ± 10%, V_{PP} = 12.0 V ± 0.6 V, T_a = 0 to 70°C)

Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0V

Item	Symbol	HN28F4001-15 Min.	HN28F4001-15 Max.	HN28F4001-17 Min.	HN28F4001-17 Max.	Unit	Test Condition
V_{PP} Setup Time	t_{VPS}	100	-	100	-	ns	
Output Enable Setup Time	t_{OES}	100	-	100	-	ns	
$\overline{OE}$ / $\overline{CE}$ Setup Time after Command Write	t_{OESA} t_{CESA}	6 6	- -	6 6	- -	µs µs	
Chip Enable Hold Time	t_{CEH}	60	-	60	-	ns	
Chip Enable Pulse Width	t_{CEP}	60	-	60	-	ns	
Address Setup Time	t_{AS}	50	-	50	-	ns	
Address Hold Time	t_{AH}	20	-	20	-	ns	
Data Setup Time	t_{DS}	50	-	50	-	ns	
Data Hold Time	t_{DH}	20	-	20	-	ns	
$\overline{CE}$ / $\overline{OE}$ Setup Time before Status Polling	t_{CESP} t_{OESP}	120 120	- -	120 120	- -	ns ns	
$\overline{CE}$ / $\overline{OE}$ Setup Time before Command Write	t_{CESC} t_{OESC}	100 100	- -	100 100	- -	ns ns	
$\overline{CE}$ / $\overline{OE}$ Setup Time before Verify	t_{CESV} t_{OESV}	6 6	- -	6 6	- -	µs µs	
$\overline{CE}$ to Output Delay in Verify	t_{CEV}	-	300	-	300	ns	$\overline{OE}$ = V_{IL}
V_{PP} Hold Time	t_{VPH}	100	-	100	-	ns	
Total Auto Chip Erase Time	t_{AETC}	-	30	-	30	s	
Total Auto Block Erase Time	t_{AETB}	-	30	-	30	s	
Total Auto Verify Programming Time	t_{AVT}	10	2000	10	2000	µs	
Standby Time Before Programming	t_{PPW}	25	-	25	-	µs	
Erase Standby Time	t_{ET}	0.95	-	0.95	-	ms	
Block Address Load Cycle	t_{BALC}	0.12	3	0.12	3	µs	
Block Address Load Time	t_{BAL}	10	-	10	-	µs	

Notes:
1. $\overline{CE}$ and $\overline{OE}$ must be fixed high during V_{PP} transition from 5 V to 12 V or from 12 V to 5 V.
2. Except for sending a Command Program, a Read operation at V_{PP} = 12 V is similar to a Read operation at V_{PP} = V_{CC}.
3. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

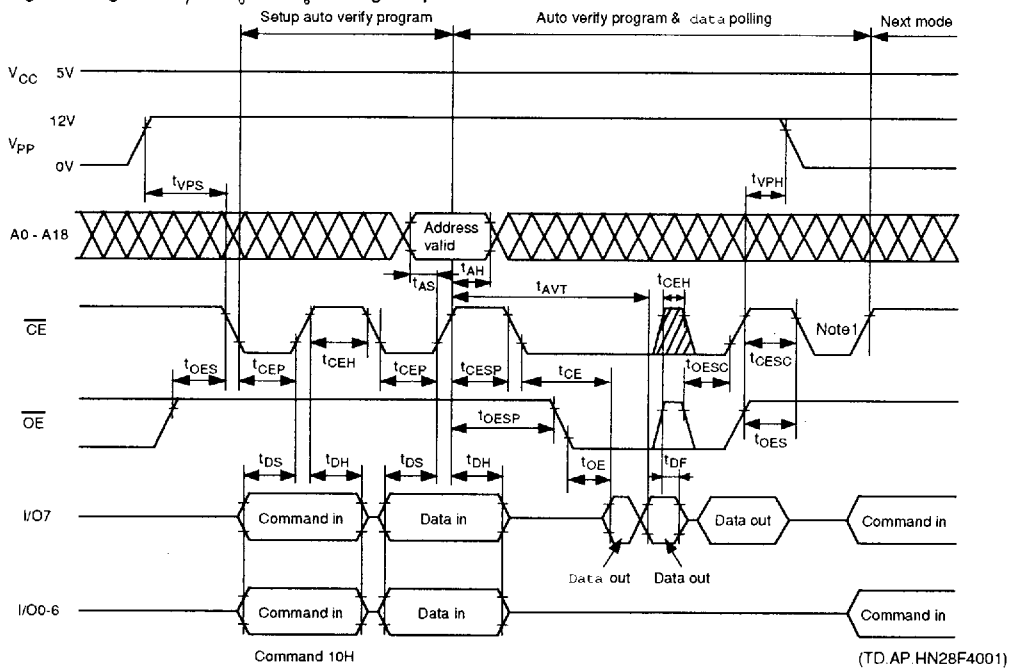
■ PROGRAMMING AND ERASE TIME [1]

	Mode	Min.	Typ.	Min.	Unit
Block (16KB) Erase Time	Automatic [2]	-	4	30	s
	Manual [3,4]	-	1	30	s
Chip (512KB) Erase Time	Automatic	-	4	30	s
	Manual [3,4]	-	1	30	s
Block (16KB) Erase Time	Automatic	-	0.7	33 [7]	s
	Manual [4,5]	-	1	30	s

Notes:
1. These values are the same for all read access versions.
2. Automatic Block Erase does not depend on the number of blocks erased simultaneously.
3. Excludes pre-write process before Erasure and Verify process (6 µs x 16KB or 512KB).
4. Excludes system overhead.
5. Minimum Byte Program time = 31 µs (25 µs Program + 6 µs Verify).
6. T_a = 25°C, V_{PP} = 12V, V_{CC} = 5V.
7. Theoretical value calculated from t_{AVT} max. 2 ms x 16KB = 33 seconds.
8. Theoretical value calculated from Manual Programming Flowchart. (25 µs + 6 µs) x 100 times x 16KB = 51 seconds.

■ AUTOMATIC PROGRAMMING TIMING WAVEFORM

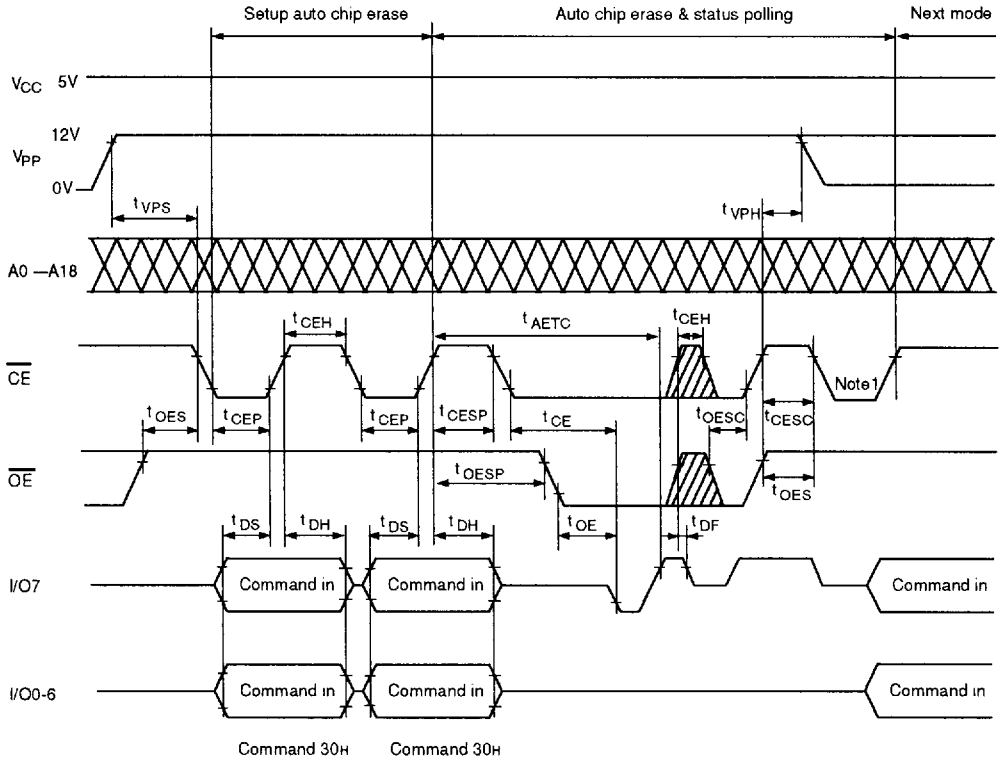
One Byte of data is programmed. External programming verification is not required because these operations are executed automatically by internal control circuitry. Programming completion can be verified by $\overline{\text{Data}}$ Polling after the Automatic Programming starts. Device outputs reverse input data during auto programming on I/O_7. I/O_0 to I/O_6 are high impedance.



Notes:
1. To exit from Data Polling in the Automatic Programming Mode, write the next Command. Example: Write Reset Command or Read Command to read data after programming.
2. During Program Time (t_{AVT}) after writing Setup Auto Verify Programming Command (10H), the device does not accept any Commands, including Reset.

■ AUTOMATIC CHIP ERASE TIMING WAVEFORM

The fast Automatic Chip Erase algorithm shown in the following timing waveform can be applied. All of the data in the chip is erased. External pre-write and erase verify are not required because the cells are pre-written and data is erased automatically by internal control circuitry. Erasure completion can be verified by Status Polling after the Automatic Erase starts. The device outputs V_{OL} level during erasure and V_{OH} level after erasure on I/O_7. I/O_0 to I/O_6 are high impedence.



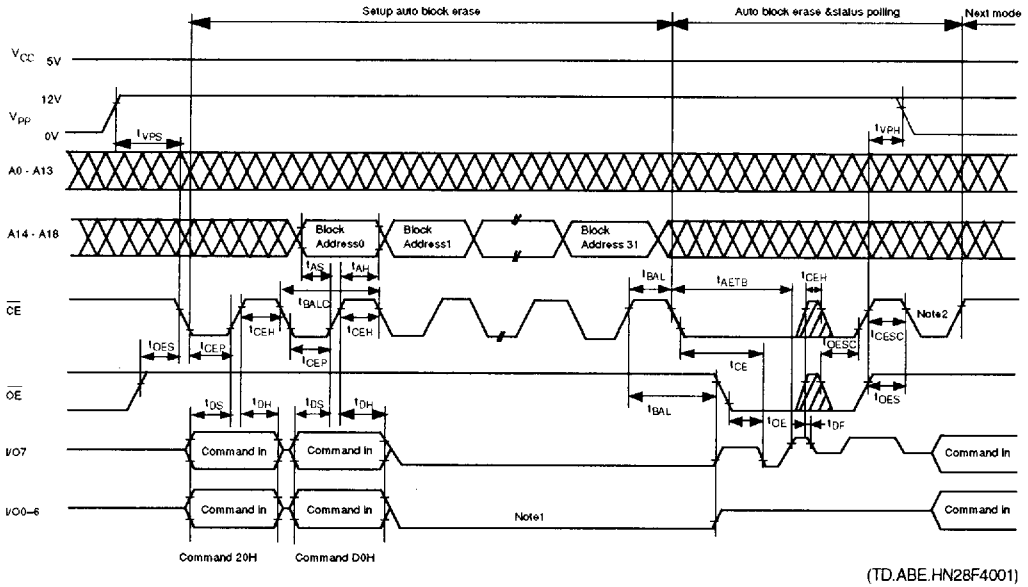
(TD.ACE.HN28F4001)

Notes: 1. To exit from Status Polling in the Automatic Chip Erase Mode, write the next Command. Example: Write Reset Command or Read Command to read data after it has been erased.
2. During Erase Time (t_{AETC}), the device does not accept any Commands, including Reset.

■ AUTOMATIC BLOCK ERASE TIMING WAVEFORM

All of the data in the block (16KBytes) indicated by A_{14} to A_{18} is erased. External pre-write and erase verify is not required because the cells are pre-written and data in the block is erased automatically by internal control circuitry. Erasure completion can be verified by Status Polling after the automatic erase starts. The device outputs V_{OL} level during erasure and V_{OH} level after erasure on I/O_7. I/O_0 to I/O_6 are high impedence.

As indicated below, a single random block or any combination of multiple blocks can be erased simultaneously.

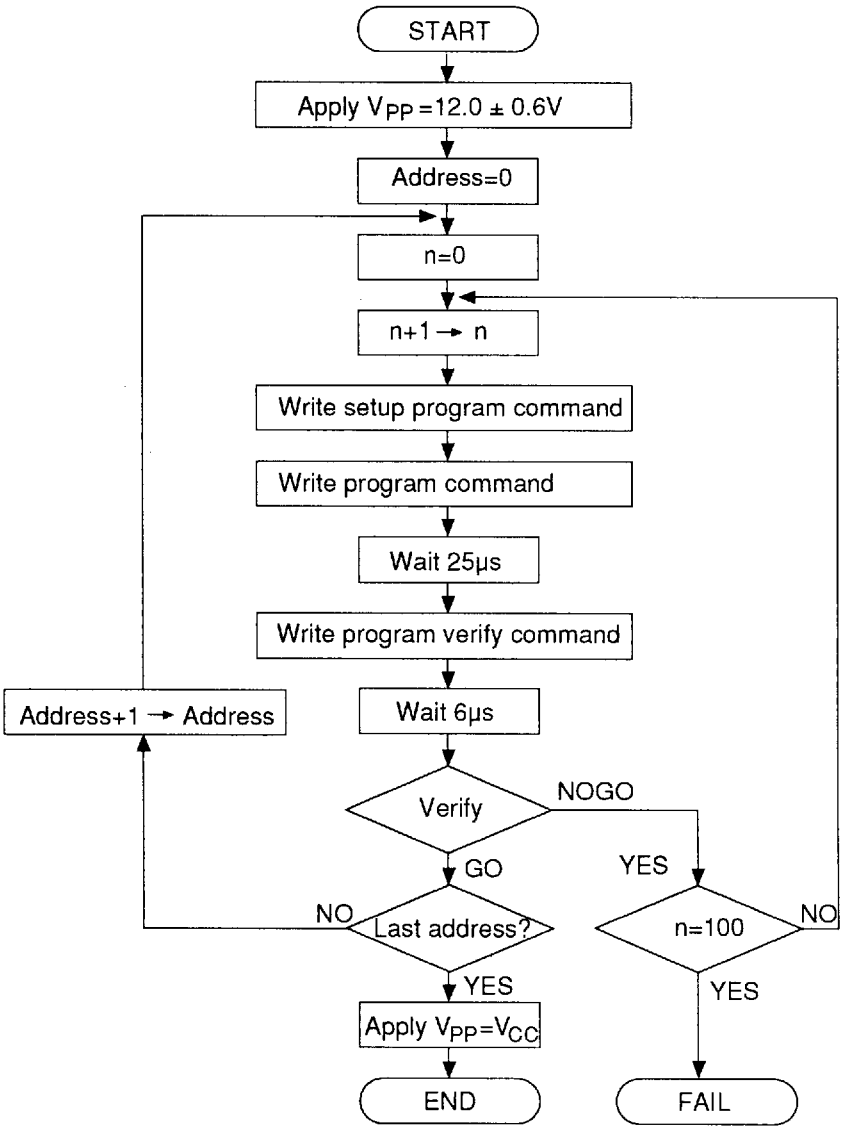


(TD.ABE.HN28F4001)

Notes:
1. I/O_0 to I/O_7 must not be held at FFH (V_{IH} level) when inputting Block addess from A_{14} to A_{18} after writing Command D0H. (Set V_{IL} is shown in the above figure). If FFH is held, the device will Reset and change to the Read Mode.
2. To exit from Status Polling mode, write the next Command.
3. During Block Erase Time (t_{AETB}), the device does not accept any Commands, including Reset.

■ MANUAL PROGRAMMING FLOWCHART

The HN28F4001 can be programmed with the fast, high-reliability programming algorithm shown in the following flowchart. This algorithm provides fast programming time without any voltage stress to the device or deterioration in reliability of programmed data.

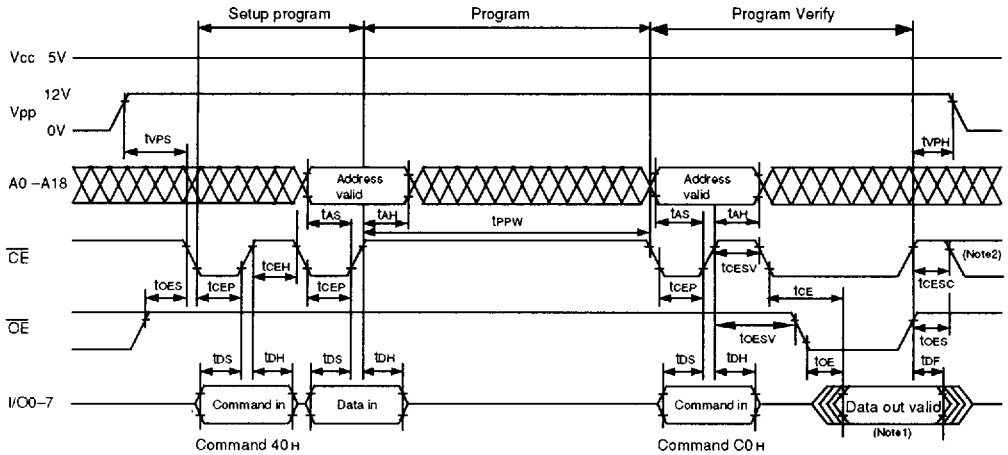


(FC.P.HN28F4001)

Note: In case two or more devices are programmed simultaneously, the following steps should be applied to avoid over-programming the verified device:

1. Setup Program Command: Write FFH
2. Program Command: Write FFH
3. Program Verify Command: Write 00H
4. Program Verify Address: Read Address

■ MANUAL PROGRAMMING TIMING WAVEFORM



(TD.MP.HN28F4001)

Notes: 1. The data output level during program verification may result in an intermediate level between V_{OH} and V_{OL} due to insufficient programming.

2. After reading Program Verify data ($\overline{CE}$ and $\overline{OE}$ turn from V_{IL} level to V_{IH} level), write the next Command to read, program, erase and program verify.
Example: Write Program Verify Command or set Program Verify address to verify next address continuously.

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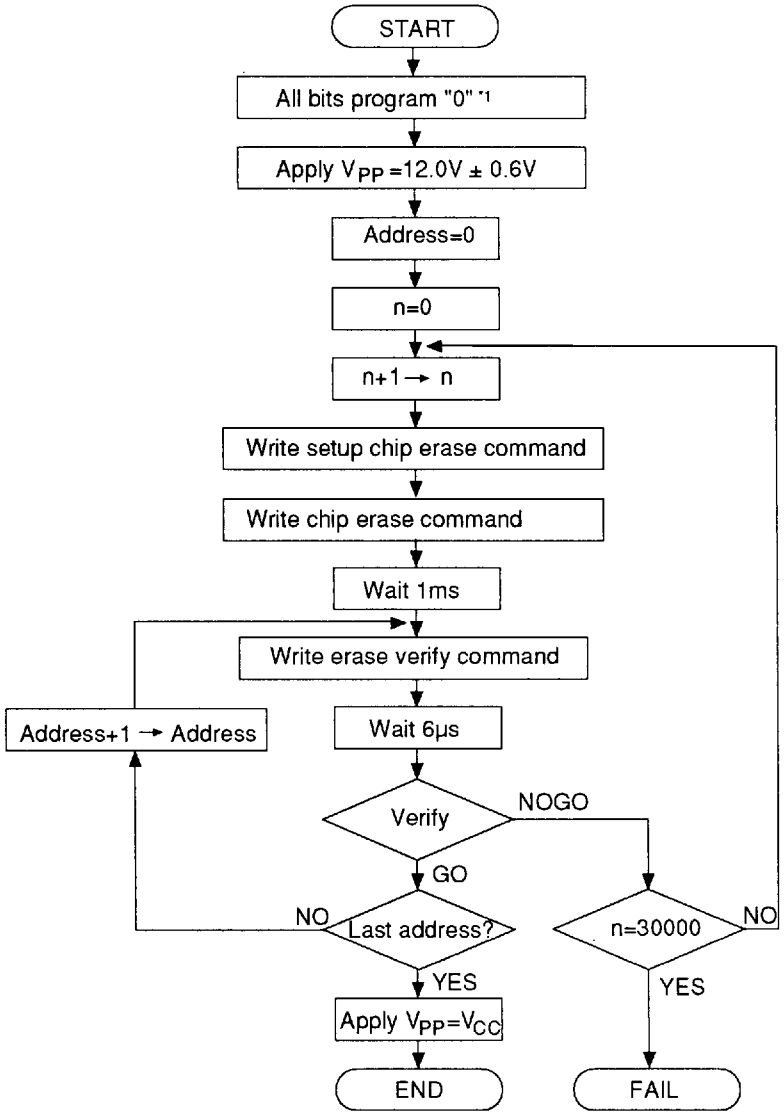
■ MANUAL CHIP ERASE FLOWCHART

The HN28F4001 can be erased with the fast, high-reliability chip erase algorithm shown in the following flowchart. This algorithm provides a fast erase time without any voltage stress to the device or deterioration in data reliability.

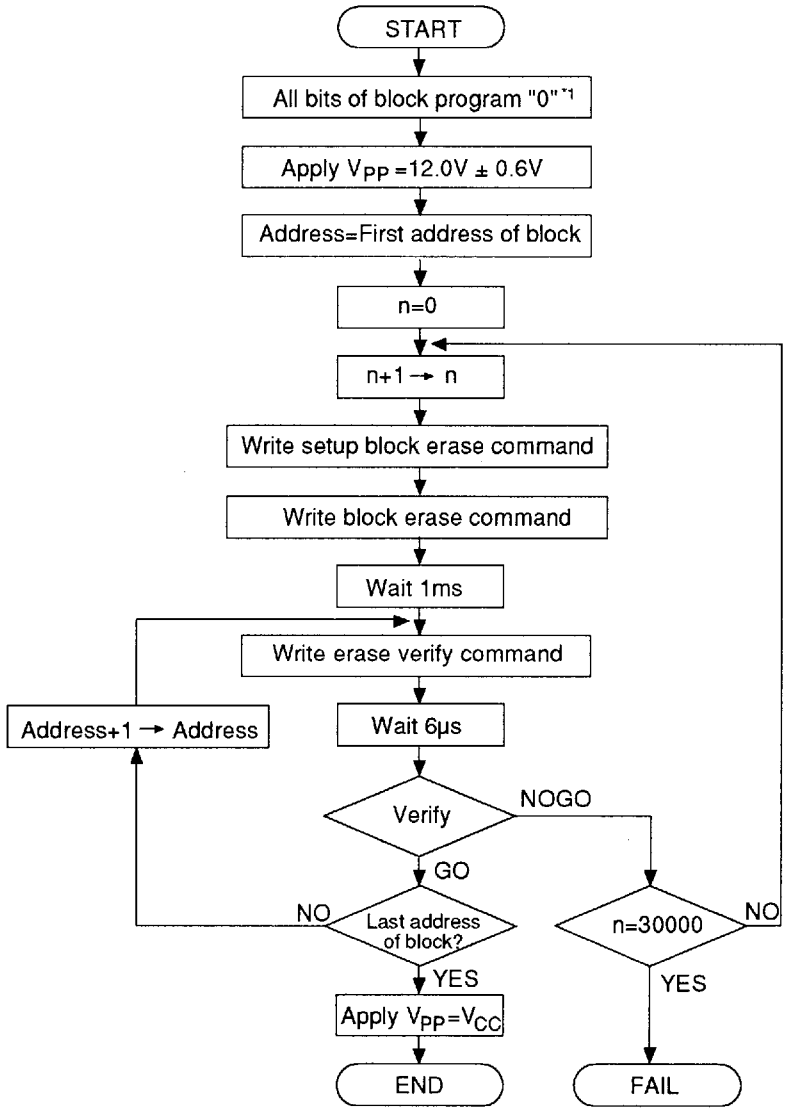


(FC.CE.HN28F4001)

Note: 1. Program data according to Manual Programming Flowchart.
2. In case two or more devices are erased simultaneously, the following steps should be applied to avoid over-erasing the verified device:
   1. Setup Erase Command: Write FFH
   2. Erase Command: Write FFH
   3. Erase Verify Command: Write 00H
   4. Erase Verify Address: Read Address

■ MANUAL BLOCK ERASE FLOWCHART

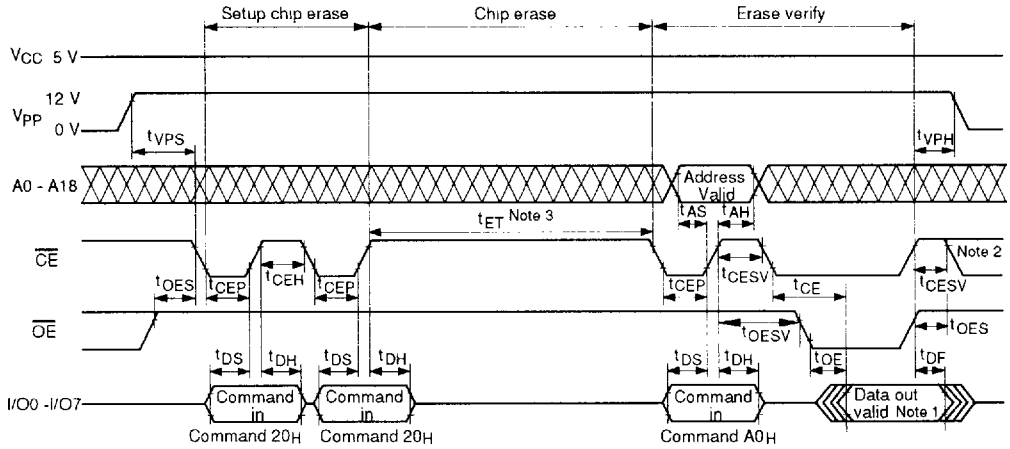
The HN28F4001 can be erased with the fast, high-reliability block erase algorithm shown in the following flowchart. This algorithm provides a fast block (16KBytes) erase time without any voltage stress to the device or deterioration in data reliability.



(FC.BE.HN28F4001)

Note: 1. Program data according to Manual Programming Flowchart.
2. In case two or more devices are erased simultaneously, the following steps should be applied to avoid over-erasing the verified device:
   1. Setup Erase Command: Write FFH
   2. Erase Command: Write FFH
   3. Erase Verify Command: Write 00H
   4. Erase Verify Address: Read Address

■ MANUAL CHIP ERASE TIMING WAVEFORM

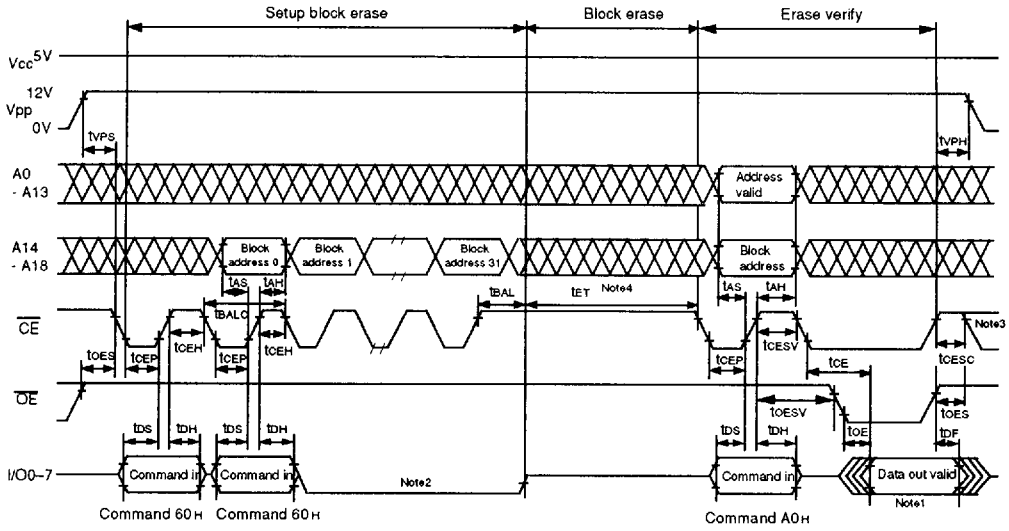


(TD.CE.HN28F4001)

Notes:
1. The data output level during erase verification may result in an intermediate level between V_{OH} and V_{OL} due to insufficient erasing.
2. After reading Erase Verify data ($\overline{CE}$ and $\overline{OE}$ turn from V_{IL} level to V_{IH} level), write the next Command to read, program, erase and program verify.
   Example: Write Erase Verify Command or set Erase Verify address to verify next address continuously.
3. During Standby Erase Time (t_{ET}), the device does not accept any Commands, including Reset.

■ MANUAL BLOCK ERASE TIMING WAVEFORM

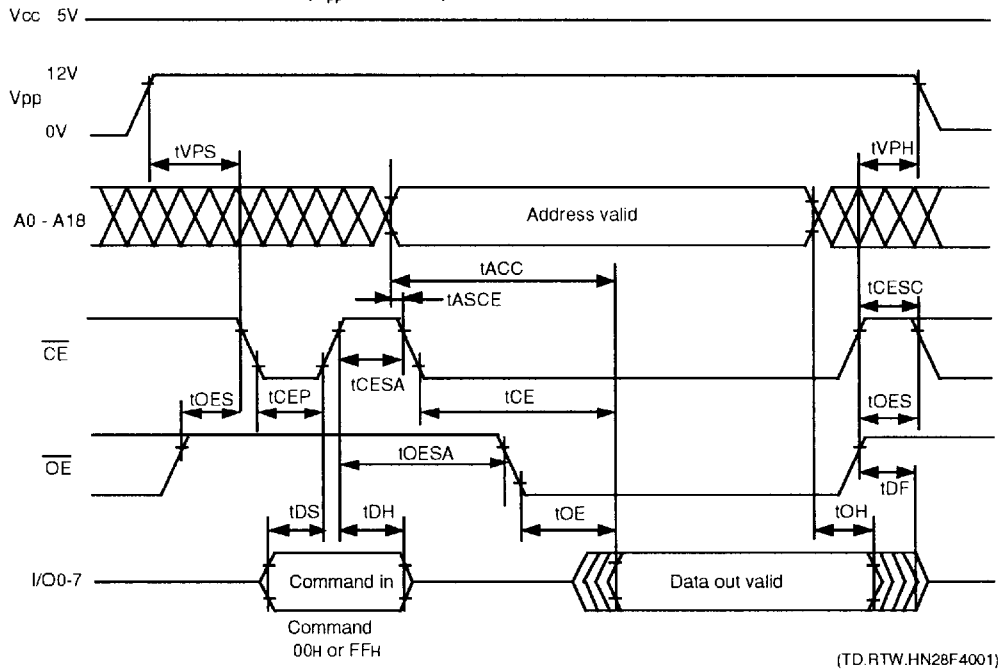
As indicated below, a single random block or any combination of multiple blocks can be erased simultaneously.



(TD.BE.HN28F4001)

Notes:
1. The data output level during erase verification may result in an intermediate level between V_{OH} and V_{OL} due to insufficient erasing.
2. I/O_0 to I/O_7 must not be held at FFH (V_{IH} level) when inputting Block addess from A_{14} to A_{18} after writing Command 60H twice. (Set V_{IL} is shown in the above figure). If FFH is held, the device will Reset and change to the Read Mode.
3. After reading Erase Verify data ($\overline{CE}$ and $\overline{OE}$ turn from V_{IL} level to V_{IH} level), write the next Command to read, program, erase and program verify.
   Example: Write Erase Verify Command or set Erase Verify address to verify next address continuously.
4. During Standby Erase Time (t_{ET}), the device does not accept any Commands, including Reset.

■ READ TIMING WAVEFORM (V_{PP} APPLIED)



Notes: 1. When 12V is applied to V_{PP}, programmed data might be destroyed by the voltage fluctuation of the supplu voltage, such as a large V_{CC} ramp. To suppress voltage fluctuation of V_{CC}, insertion of a bypass capacitor is recommended.

■ DEVICE IDENTIFIER MODE DESCRIPTION

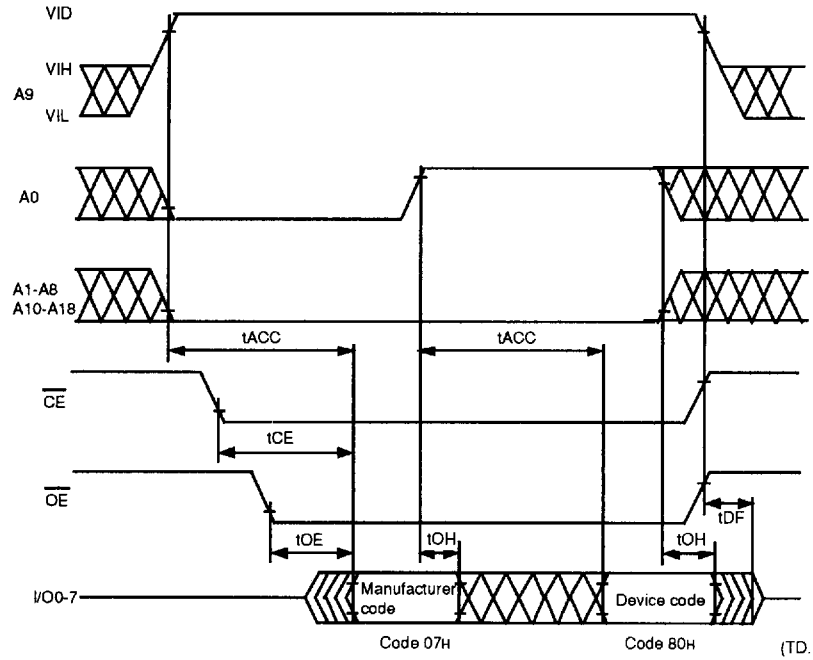
The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

■ HN28F4001 SERIES IDENTIFIER CODE

Identifier	A_0	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	1	0	0	0	0	0	0	0	80

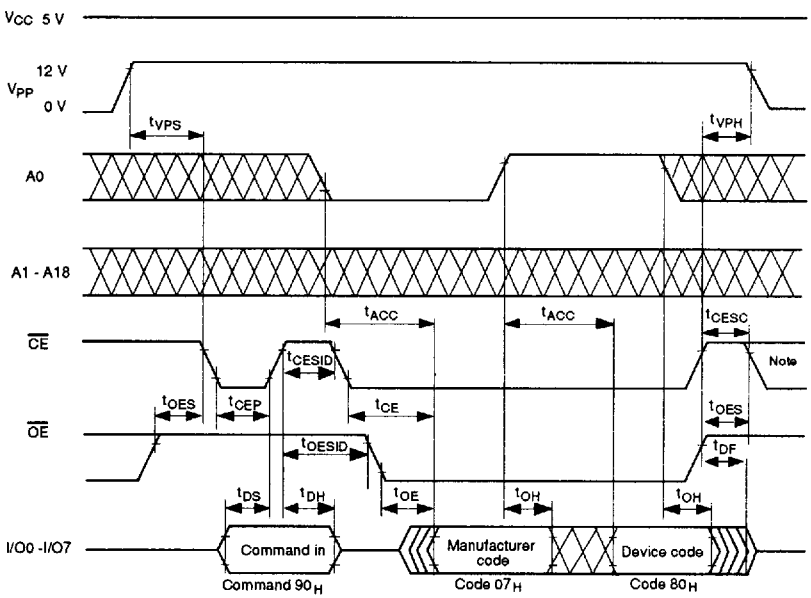
Notes: 1. Device identifier code can be read out by applying 12.0 V ± 0.5 V to A9 when $V_{PP} = V_{CC}$, or inputting Command while V_{PP}=12 V.
2. $V_{CC} = V_{PP}$=5.0 V ± 10% when applying 12 V to A9.
V_{CC} =5.0 V ± 10% and V_{PP}=12.0 V ± 0.6 V in command inputs.
3. A1 to A8, A10 to A18, $\overline{CE}$, and $\overline{OE}$ = V_{IL}.

■ IDENTIFIER CODE READ TIMING WAVEFORM (V_{PP} = V_{SS} to V_{CC})



(TD.ID1.HN28F4001)

■ IDENTIFIER CODE READ TIMING WAVEFORM (V_{PP} = 12V)



(TD.ID2.HN28F4001)

Note: 1. To exit from the Identifier Code Read mode, write the next Command.