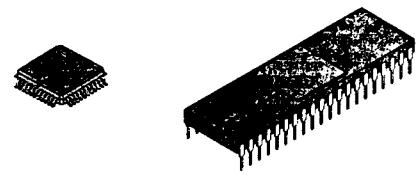
SONY CXA1146Q/D /CXA1156Q/D

8bit 160/300MSPS Triple VIDEO DAC

Advance Information

Note : This specification is subject to change.

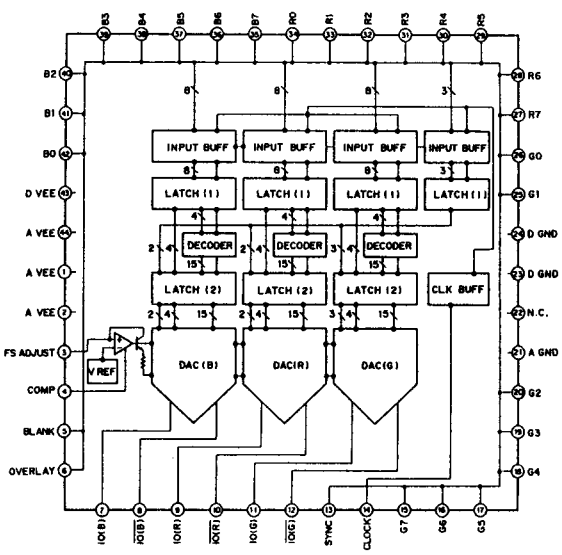
44 pin QFP (Ceramic) 40 pin DIP (Ceramic)



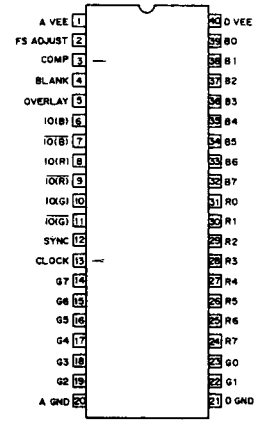
Features

- 160/300MHz update rate
- 8-bit RGB
- Sync., Blank and Overlay
- 25 Ω/37.5 Ω Load
- I (+), I (−) outputs
- RS-343A Compatible Output
- ECL 100K and 10K Compatible Inputs
- −5.5 to −4.2 Volt Power Supply
- Package − QFP, DIP (To be available)

CXA1146Q/CXA1156Q − QFP
(Quad Flat Pack) version
Pin Configuration (Top View)
Block Diagram



CXA1146D/CXA1156D − DIP version
(To be available)
Pin Configuration (Top View)



(Pin Replacable with TDC1318 and Bt109.)

AE89676 − ST

Absolute Maximum Ratings (Ta = 25°C)

	Rating	Unit
V_{EE}	−7 to +0.5	V
Input voltage, Digital	V_{EE} to +0.5	V
Input voltage, Reference	V_{EE} to +0.5	V
Output current, I (+), I (−)	50	mA
Storage temperature	−65 to +150	°C

Operating Conditions

Symbol	Item		Min.	Typ.	Max.	Unit
V_{EE}	Supply voltage		−4.2	−5.2	−5.5	V
tpw1	CLK pulse width High	CXA1146	3.0			ns
		CXA1156	1.5			
tpw0	CLK pulse width Low	CXA1146	3.0			ns
		CXA1156	1.5			
ts	Set up time	CXA1146	1.5			ns
		CXA1156	1.0			
th	Hold time		0			ns
V_{IL}	Input voltage logic Low				−1.49	V
V_{IH}	Input voltage logic High		−1.05			V
I_{REF}	Reference current			1.6		mA
Tc	Case temperature		−55		125	°C

Electrical Characteristics (CXA1146)　　(V_{EE} = − 5.2V, Ta = 25°C)

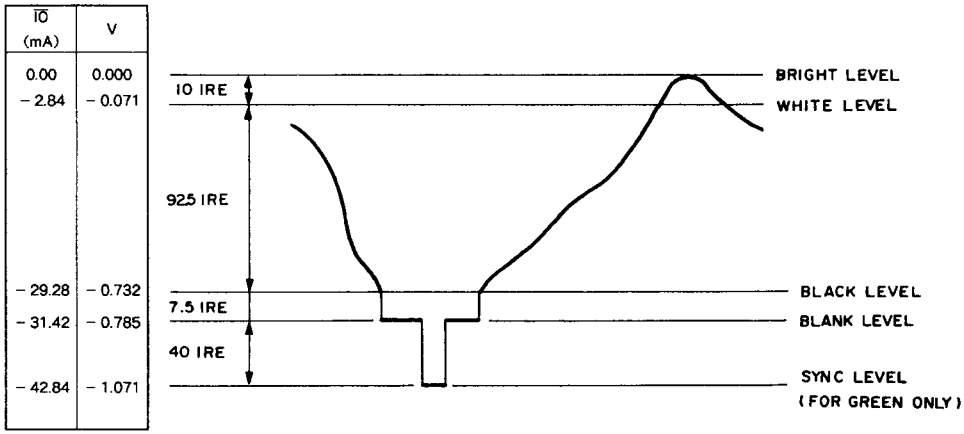
Item	Symbol	Min.	Typ.	Max.	Unit
Supply current	I_{EE}		− 200		mA
Compliance voltage output (+)	Vocp	− 1.2		1.5	V
Compliance voltage output (−)	Vocn	− 1.2		1.5	V
Equiv. output resistance	Ro	50			kΩ
Equiv. output capacitance	Co		10		pF
Max. output current output (+)	Iop	− 44			mA
Max. output current output (−)	Ion	− 44			mA
Input current logic Low	I_{IL}		20		μA
Input current logic High	I_{IH}		20		μA
Max. conversion rate	Fs	160			MHz
CLOCK to output delay	td		2.0		ns
Current settling time	tset			5.0	ns
Rise time, Current	tr			2.0	ns
Fall time, Current	t_f			2.0	ns
Integral linearity error	E_{LI}			± 1/2	LSB
Differential linearity error	E_{LD}			± 1/2	LSB
Output offset current	I_{OF}			10.0	μA
Absolute gain error	E_G			7.0	% of F.S.
Gain error tempco.	T_{CG}		0		% of F.S./°C
Differential phase	DP			1.0	degree
Differential gain	DG			2.0	%
Glitch energy	GE		1.3		LSB • nsec

Electrical Characteristics (CXA1156) (VEE = − 5.2V, Ta = 25 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply current	I_{EE}		− 300		mA
Compliance voltage output (+)	Vocp	− 1.2		1.5	V
Compliance voltage output (−)	Vocn	− 1.2		1.5	V
Equiv. output resistance	Ro	50			k Ω
Equiv. output capacitance	Co		10		pF
Max. output current output (+)	Iop	− 44			mA
Max. output current output (−)	Ion	− 44			mA
Input current logic Low	I_{IL}		40		μA
Input current logic High	I_{IH}		40		μA
Max. conversion rate	Fs	300			MHz
CLOCK to output delay	td		1.0		ns
Current settling time	tset			2.5	ns
Rise time, Current	tr			1.0	ns
Fall time, Current	t_f			1.0	ns
Integral linearity error	E_{LI}			± 1/2	LSB
Differential linearity error	E_{LD}			± 1/2	LSB
Output offset current	I_{OF}			10.0	μA
Absolute gain error	E_G			7.0	% of F.S.
Gain error tempco.	T_{CG}		0		% of F.S./℃
Differential phase	DP			1.0	degree
Differential gain	DG			2.0	%
Glitch energy	GE		1.3		LSB • nsec

Pin Descriptions

Pin Name	Description
BLANK	Control pin for composite blank. Logic "1" sets the D/A output to the blanking level. The output is delivered with the rising edge of CLOCK. The voltage level for the pin is ECL compatible.
SYNC	Control pin for composite sync. Logic "1" sets the D/A output to have composite sync level only for green. The sync is delivered with the rising edge of CLOCK. The voltage level for the pin is ECL compatible.
OVERLAY	Control pin for overlay. Logic "1" forced the D/A output to the overlay voltage level. The overlay is delivered with the rising edge of CLOCK. The voltage level for the pin is ECL compatible.
R0 – R7 G0 – G7 B0 – B7	Data inputs for red, green and blue, respectively. R0, G0 and B0 are for least significant bit. These inputs level are ECL compatible.
CLOCK	Clock input pin. ECL compatible.
$I_{O(R)}$, $\overline{I_{O(R)}}$ $I_{O(G)}$, $\overline{I_{O(G)}}$ $I_{O(B)}$, $\overline{I_{O(B)}}$	Current outputs for red, green and blue. Complementary outputs. These can directly drive doubly-terminated 75 Ω and 50 Ω loads.
FS ADJUST	Control pin for full-scale. The scale is set by a resistor (Rset) connected between this pin and AGND. The relation between Rset and R_L which is current output load is the following : Rset = 1.24V/ ((661mV/R_L) × (16/255)) Ohms
COMP	Compensation pin. This provides compensation for internal amplifier built-in.



* In case of doubly-terminated 50 Ω load.

Fig. 1. Composite Video Level

Description	$\overline{IO}$ (mA)	OVERLAY	SYNC	BLANK	D/A Input Data
OVERLAY	0.00	1	0	0	$ × ×
WHITE	– 2.84	0	0	0	$ FF
DATA		0	0	0	data
BLACK	– 29.28	0	0	0	$ 00
BLANK	– 31.42	×	0	1	$ × ×
SYNC	– 42.84	×	1	×	$ × ×

Table 1. Video Output Truth Table

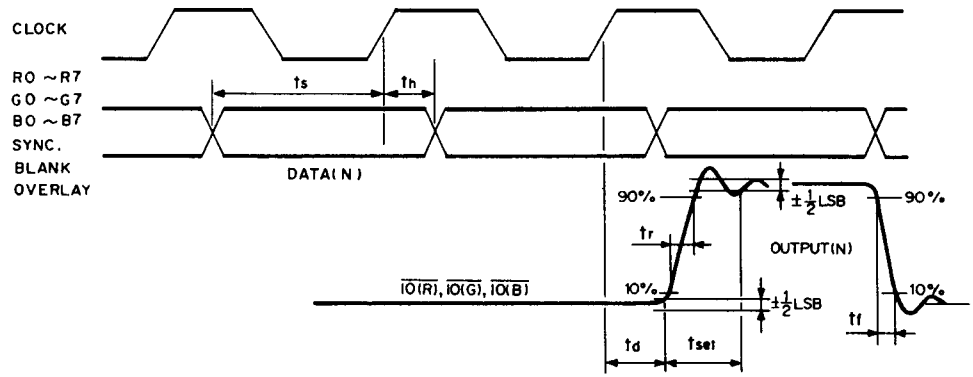


Fig. 2. Timing Diagram

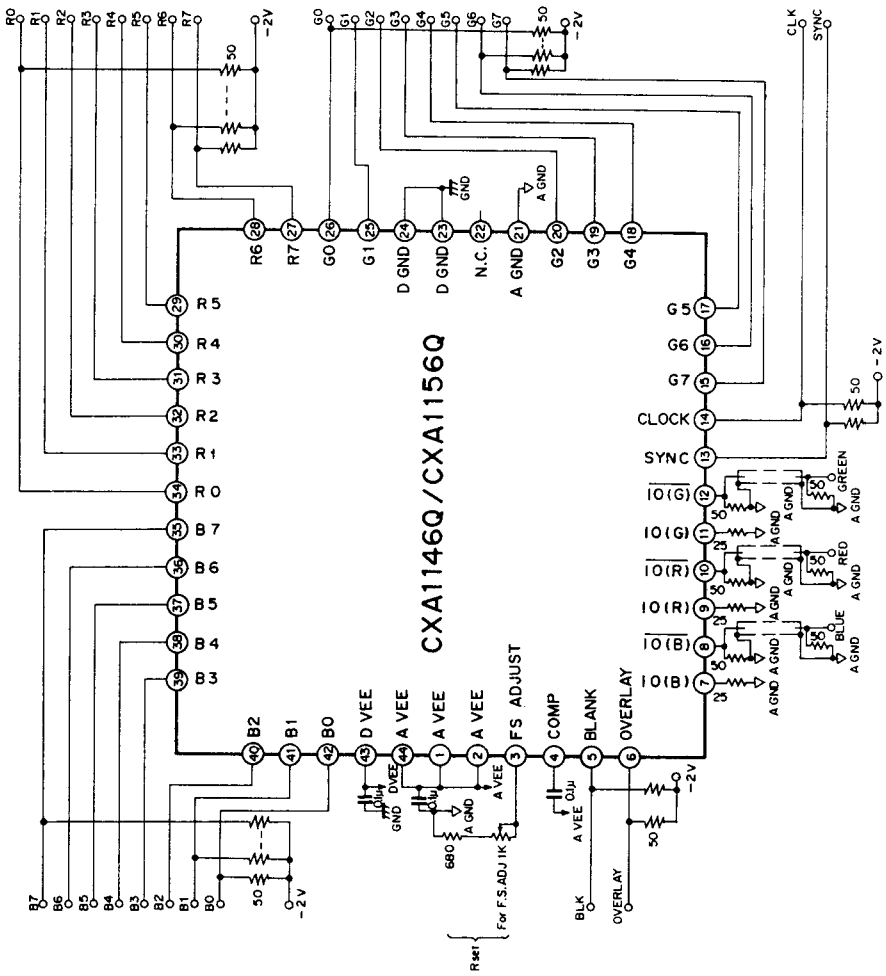
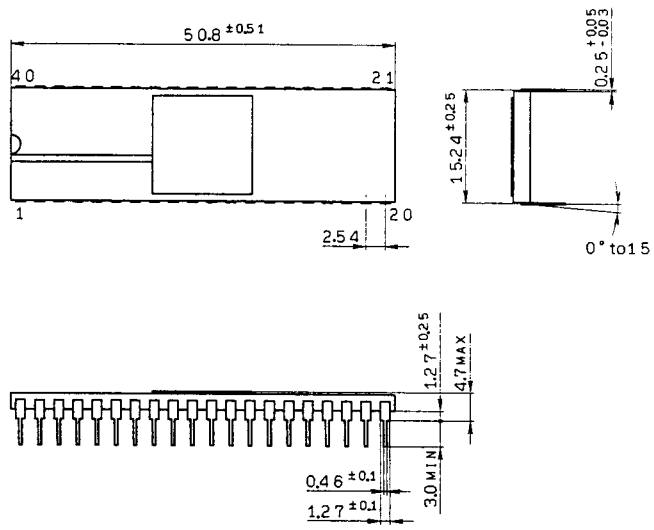


Fig. 3. Typical Circuit Connection

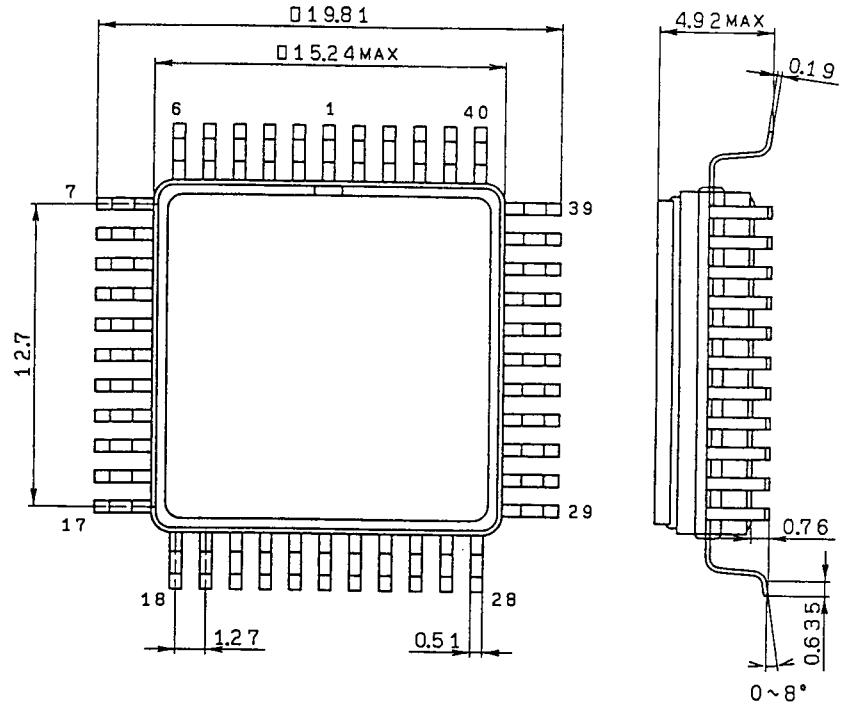
Package Outline Unit : mm

CXA1146D/CXA1156D 40 pin DIP (Ceramic) 600mil



DIP-40C-01

CXA1146Q/CXA1156Q 44 pin QFP (Ceramic) 50mil



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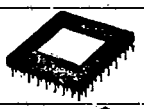
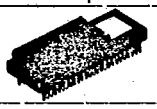
Sony Package Product Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	DIP	DUAL IN LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		SIP	SINGLE IN LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		ZIP	ZIG ZAG IN LINE PACKAGE		P	2.54mm (100MIL) Zig Zag inline	Through Hole Lead	1-direction
		PGA	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	4-direction
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
Surface mounted	Standard flat package	QFP	QUAD FLAT PACKAGE		P	1.0mm 0.8mm	Gull-Wing	4-direction
		SOP	SMALL OUTLINE PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull Wing	2-direction
	Standard chip carrier	PLCC	PLASTIC LEADED CHIP CARRIER		P	1.27mm (50MIL)	J-bend	4-direction
		LCC	LEAD LESS CHIP CARRIER		C	1.27mm (50MIL)	Lead less	Package side
	Shrink chip carrier	SPLCC (PLCC)	SHRINK PLASTIC LEADED CHIP CARRIER		P	1.27mm Max. (50MIL Max.)	J-bend	4-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEAD PACKAGE		P	1.27mm (50MIL)	J-bend	2-direction

*P……Plastic, C……Ceramic