PRELIMINARY

INTEL 430TX PCISET: 82439TX SYSTEM CONTROLLER (MTXC)

- Supports Mobile and Desktop
- Supports the Pentium® Processor Family Host Bus at 66 MHz and 60 MHz at 3.3V and 2.5V
- PCI 2.1 Compliant
- Integrated Data Path
- Integrated DRAM Controller
  - 4 Mbytes to 256 MBytes main memory
  - 64-Mbit DRAM/SDRAM Technology Support
  - FPM (Fast Page Mode), EDO and SDRAM DRAM Support
  - 6 RAS Lines Available
  - Integrated Programmable Strength for DRAM Interface
  - CAS-Before-RAS Refresh, Extended Refresh and Self Refresh for EDO
  - CAS-Before-RAS and Self Refresh for SDRAM
- Integrated L2 Cache Controller
  - 64-MB DRAM Cacheability
  - Direct Mapped Organization—Write Back Only
  - Supports 256K and 512K Pipelined Burst SRAM and DRAM Cache SRAM
  - Cache Hit Read/Write Cycle Timings at 3-1-1-1
  - Back-to-Back Read/Write Cycles at 3-1-1-1-1-1-1-1
  - 64K x 32 SRAM also supported
- Fully Synchronous, Minimum Latency 30/33-MHz PCI Bus Interface
  - Five PCI Bus Masters (including PIIX4)
  - 10 DWord PCI-to-DRAM Read Prefetch Buffer
  - 18 DWord PCI-DRAM Post Buffer
  - Multi-Transaction Timer to Support Multiple Short PCI Transactions
- Power Management Features
  - PCI CLKRUN# Support
  - Dynamic Stop Clock Support
  - Suspend to RAM (STR)
  - Suspend to Disk (STD)
  - Power On Suspend (POS)
  - Internal Clock Control
  - SDRAM and EDO Self Refresh During Suspend
  - ACPI Support
  - Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM)
  - SMM Writeback Cacheable in E_SMRAM Mode up to 1 MB
  - 3.3/5V DRAM, 3.3/5V PCI 3.3/5V Tag and 3.3/2.5 SRAM Support
- Test Features
  - NAND Tree Support for all Pins
- Supports the Universal Serial Bus (USB)
- 324-Pin MBGA 430TX PCIset Xcelerated Controller (MTXC) with integrated Data Paths

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The Intel 430TX PCIset (430TX) consists of the 82439TX System Controller (MTXC) and the 82371AB PCI ISA IDE Xcelerator (PIIX4). The 430TX supports both mobile and desktop architectures. The 430TX forms a Host-to-PCI bridge and provides the second level cache control and a full function 64-bit data path to main memory. The MTXC integrates the cache and main memory DRAM control functions and provides bus control to transfers between the CPU, cache, main memory, and the PCI Bus. The second level (L2) cache controller supports a writeback cache policy for cache sizes of 256 Kbytes and 512 Kbytes. Cacheless designs are also supported. The cache memory can be implemented with pipelined burst SRAMs or DRAM cache SRAMs. An external Tag RAM is used for the address tag and an internal Tag RAM for the cache line status bits. For the MTXC DRAM controller, six rows are supported for up to 256 Mbytes of main memory. The MTXC is highly integrated by including the Data Path into the same BGA chip. Using the snoop ahead feature, the MTXC allows PCI masters to achieve full PCI bandwidth. For increased system performance, the MTXC integrates posted write and read prefetch buffers. The 430TX integrates many Power Management features that enable the system to save power when the system resources become idle.

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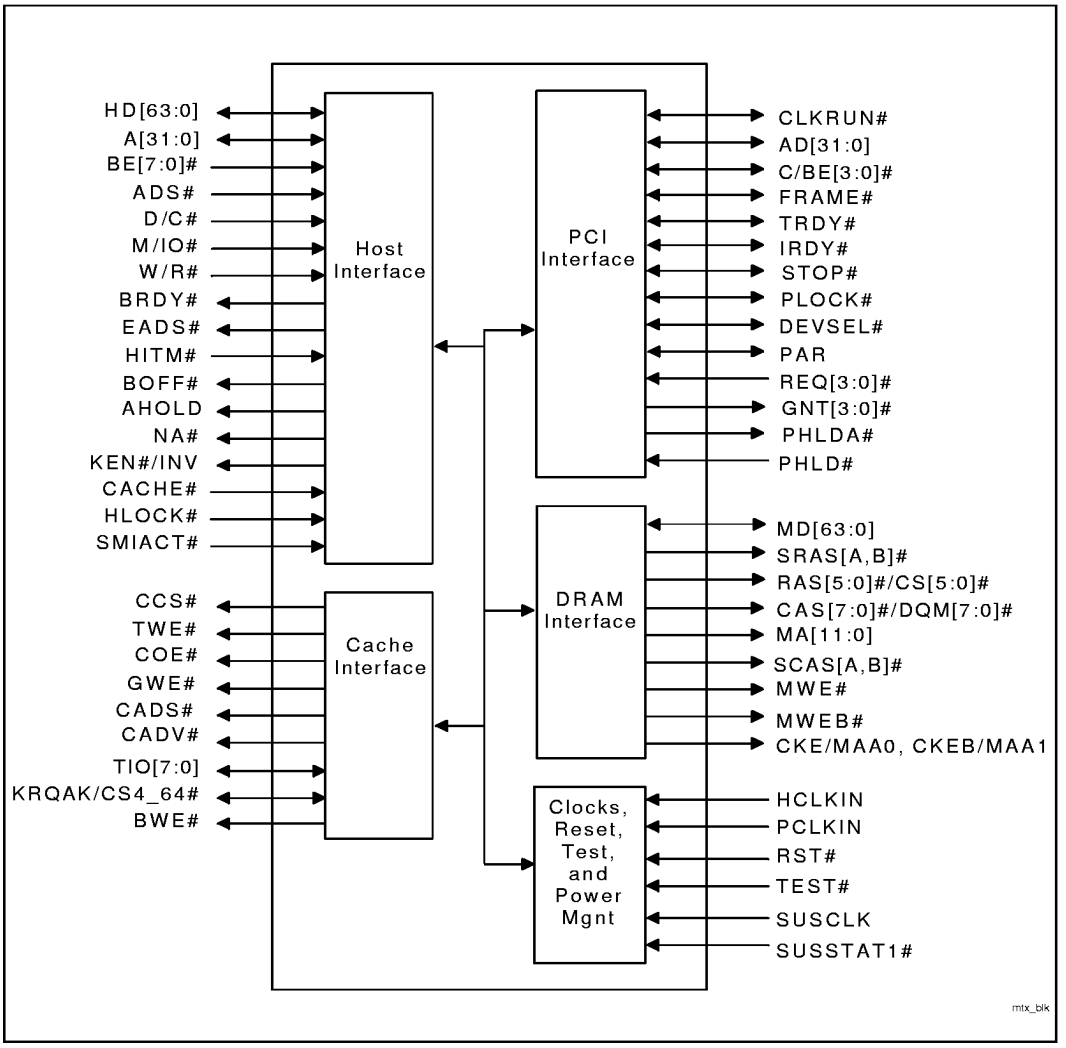


MTXC Simplified Block Diagram

CONTENTS

1.0. ARCHITECTURE OVERVIEW

The MTXC host bridge provides a completely integrated solution for the system controller and datapath components in a Pentium processor system. The MTXC Supports all Pentium family processors since P54C, it has 64-bit Host and DRAM Bus Interface, 32-bit PCI Bus Interface, Second level Cache Interface, and it integrates the PCI arbiter.

The MTXC interfaces with the Pentium processor host bus, a dedicated memory data bus, and the PCI bus (see Figure 1).

The MTXC bus interfaces are designed to interface with 2.5V, 3.3V and 5V busses. The MTXC implements 2.5V and 3.3V drivers and 5V tolerant receivers. The MTXC connects directly to the Pentium processor 3.3V or 2.5V host bus, directly to 5V or 3.3V DRAMs, and directly to the 5V or 3.3V PCI bus. The 430TX also interfaces directly to the 3.3V or 5.0V TAGRAM and 3.3V Cache.

The MTXC works with the PCI IDE/ISA Accelerator 4 (PIIX4). The PIIX4 provides the PCI-to-ISA/EIO bridge functions along with other features such as a fast IDE interface (PIO mode 4 and Ultra DMA/33), Plug-n-Play port, APIC interface, PCI 2.1 Compliance, SMBUS interface, and Universal Serial Bus Host Controller functions.

DRAM Interface

The DRAM interface is a 64-bit data path that supports Standard (or Fast) Page Mode (FPM), Extended Data Out (EDO) and Synchronous DRAM (SDRAM) memory. The DRAM controller inside the MTXC is capable of generating 3-1-1-1 for posted writes for any type of DRAM that is used. While read performance is 6-1-1-1 for SDRAM, 5-2-2-2 for EDO, and 6-3-3-3 for FPM.

The DRAM interface supports 4 Mbytes to 256 Mbytes with six RAS lines. The MTXC supports 4-Mbit, 16-Mbit, and 64-Mbit DRAM and SDRAM technology, both symmetrical and asymmetrical. Parity is not supported, and for loading reasons, x32 and x64 SIMMs/DIMMs/SO-DIMMs should be used.

Second Level Cache

The second level cache is direct mapped and supports both 256-Kbyte and 512-Kbyte SRAM configuration using Pipeline Burst SRAM or DRAM Cache SRAM. The Cache performance is 3-1-1-1 for line read/write and 3-1-1-1-1-1-1-1 for back to back reads that are pipelined. Cacheless configuration is also supported.

PCI Interface

The PCI interface is 2.1 compliant and supports up to four PCI bus masters in addition to the PIIX4 bus master requests.

Datapath and Buffers

The MTXC contains three sets of data buffers for optimizing data flow. A five QWord deep DRAM write buffer is provided for CPU-to-DRAM writes, second level cache write backs, and PCI-to-DRAM transfers. This buffer is used to achieve 3-1-1-1 posted writes to DRAM and also provides DWord merging and burst merging for CPU-to-DRAM write cycles. In addition, an extra line of buffering is provided that is combined with the DRAM Write Buffer to supply an 18 DWord deep buffer for PCI to main memory writes. A five DWord buffer is provided for CPU-to-PCI writes to help maximize the bandwidth for graphic writes to the PCI bus. Also, five QWords of prefetch buffering has been added to the PCI-to-DRAM read path that allows up to two lines of data to be prefetched at an x-2-2-2 rate. The MTXC interfaces directly to the Host and DRAM data bus.

Power Management Features

The MTXC implements extensive power management features. The CLKRUN# feature enables controlling of the PCI clock (on/off). The MTXC supports POS, STR, STD, and Soft-off suspend states. SUSCLK and

SUSSTAT1# signals are used for implementing Suspend Logic. The MTXC supports two SMRAM modes; Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM). The C_SMRAM is the traditional SMRAM feature implemented in Intel PCIsets. The E_SMRAM is a new feature that supports writeback cacheable SMRAM space up to 1 Mbytes. In order to minimize the idle power, the internal clock in MTXC is turned off (gated off) when there is no activity on the Host and PCI Bus.

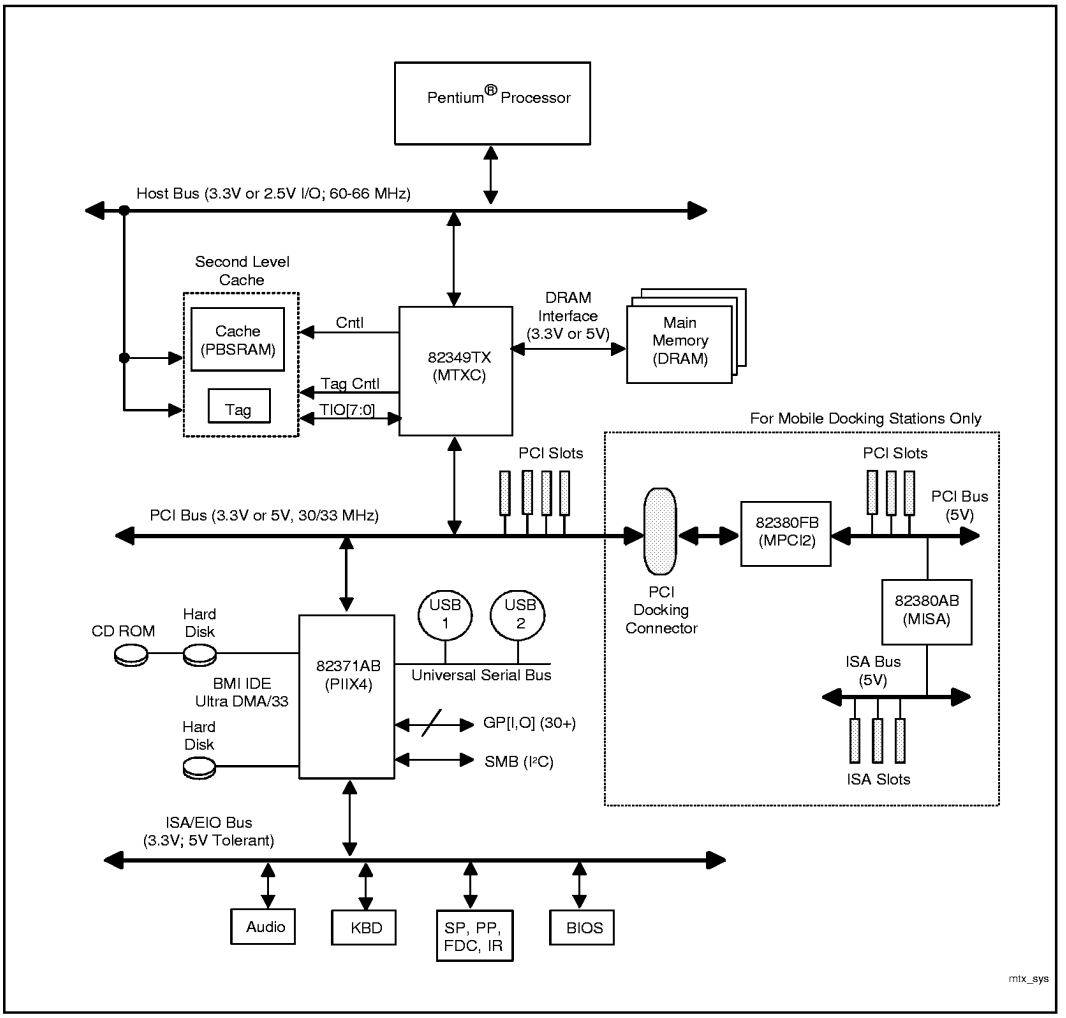


Figure 1. MTXC System Block Diagram

2.0. SIGNAL DESCRIPTION

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signal. The term assert, or assertion indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation indicates that a signal is inactive.

The I/O buffer types are shown below:

Buffer Type	Description
I	input only signal
O	totem pole output
I/O	bi-direction, tri-state input/output pin
s/t/s	sustained tri-state
od	open drain
3.3V/2.5V	Indicates the buffer is 3.3V or 2.5V only, depending on the voltage (3.3V or 2.5V) connected to VccX pins.
3.3V/5V	Indicates that the output is 3.3V and input is 3.3V receiver with 5V tolerance.
5V	Indicates 3.3V receiver with 5V tolerance.

2.1. MTXC Signals

2.1.1. HOST INTERFACE

Name	Type	Description
A[31:3]	I/O 3.3V/2.5V	**Address Bus.** A[31:3] connects to the address bus of the CPU. During CPU cycles A[31:3] are inputs. The MTXC drives A[31:3] during inquire cycles on behalf of PCI initiators. Bits A[31:26] act as inputs when RST# is active
BE[7:0]#	I 3.3V/2.5V	**Byte Enables.** The CPU byte enables indicate which byte lane the current CPU cycle is accessing. All eight byte lanes must be provided to the CPU if the cycle is a cacheable read regardless of the state of BE[7:0]#.
ADS#	I 3.3V/2.5V	**Address Status.** CPU asserts ADS# in T1 of the CPU bus cycle.
BRDY#	O 3.3V/2.5V	**Bus Ready.** The MTXC asserts BRDY# to indicate to the CPU that data is available on reads or has been received on writes.
NA#	O 3.3V/2.5V	**Next Address.** This signal is asserted by the MTXC to indicate to the Processor that it is ready to process a second cycle.

Name	Type	Description
AHOLD	O 3.3V/2.5V	**Address Hold.** The MTXC asserts AHOLD when a PCI initiator is performing a cycle to DRAM. AHOLD is held for the duration of the PCI burst transfer. The MTXC will negate AHOLD when the completion of the PCI to DRAM read or write cycles complete and during PCI peer transfers. AHOLD is kept asserted while PHLDA# is asserted (i.e., duration of PIIX4 granting).
EADS#	O 3.3V/2.5V	**External Address Strobe.** Asserted by the MTXC to inquire the first level cache when servicing PCI master references of DRAM.
BOFF#	O 3.3V/2.5V	**Back Off.** Asserted by the MTXC when required to terminate a CPU cycle that was in progress.
HITM#	I 3.3V/2.5V	**Hit Modified.** Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the first level cache and needs to be written back.
M/IO#, D/C#, W/R#	I 3.3V/2.5V	**Memory/IO; Data/Control; Write/Read.** Asserted by the CPU with ADS# to indicate the type of cycle that the system needs to perform.
HLOCK#	I 3.3V/2.5V	**Host Lock.** All CPU cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no PCI activity to DRAM is allowed.
CACHE#	I 3.3V/2.5V	**Cache.** Asserted by the CPU during a read cycle to indicate the CPU will perform a burst line fill. Asserted by the CPU during a write cycle to indicate the CPU will perform a burst writeback cycle. If CACHE# is asserted to indicate cacheability, the MTXC will assert KEN# either with the first BRDY#, or with NA# if NA# is asserted before the first BRDY#.
KEN#/INV	O 3.3V/2.5V	**Ken/Invalidate.** KEN#/INV functions as both the KEN# signal during CPU read cycles, and the INV signal during L1 snoop cycles. During CPU cycles, KEN#/INV is normally low. KEN#/INV is driven high during the 1st BRDY# or NA# assertion of a non-L1-cacheable CPU read cycle. KEN#/INV is driven high(low) during the EADS# assertion of a PCI master DRAM write(read) snoop cycle. Note that KEN#/INV operation during snoop cycles is independent of the FLCE bit programming.
SMIACT#	I 3.3V/2.5V	**System Management Interrupt Active.** This is asserted by the CPU when it is in system management mode as a result of an SMI. This signal must be sampled active with ADS# for the processor to access the SMM space of DRAM, located at A0000h, after SMM space has been loaded and locked by BIOS at system boot.
HD[63:0]	I/O 3.3V/2.5V	**Host Data.** These signals are connected to the CPU data bus. These signals have internal pull-down resistors.

NOTES:
All of the signals in the host interface are described in the Pentium Processor data sheet. The preceding table highlights MTXC specific uses of these signals.

2.1.2. DRAM INTERFACE

Name	Type	Description
RAS[3:0]# or CS[3:0]#, RAS4#/CS4#/ BA1, RAS5#/CS5#/ MA13	O 3.3 V	**Row Address Strobe—RASx# (EDO/FPM).** These pins select the DRAM row. **Chip Select—CSx# (SDRAM).** These pins activate the SDRAMs. SDRAM accepts any command when its CS# pin is active low. Note: For 64Mbit SDRAM support, BA1/MA12 and MA13 are muxed with the RAS4# and RAS5# signals, respectively. When SDRAMC[bit 1]=1, BA1 and MA13 are driven out on these lines.
CAS[7:0]# or DQM[7:0]	O 3.3 V	**Column Address Strobe (EDO/FPM).** These pins select the DRAM column. **Input/Output Data Mask SDRAM).** These pins act as synchronized output enables during a read cycle and a byte mask during a write cycle. The read cycles require Tdqz clock latency before the functions are actually performed. In case of a write cycle, word mask functions are performed in the same cycle (0 cycle latency).
MA[11:0]	O 3.3 V	**Memory Address (EDO/FPM/SDRAM).** This is the row and column address for DRAM. These buffers now include programmable size selection, as controlled by the DRAMEC[MAD] bit. For 64-Mbit SDRAM support BA1/MA12 and MA13 are muxed with the RAS4# and RAS5# signals, respectively.
MWEB#	O 3.3 V	**Memory Write Enable (second copy) (EDO/FPM/SDRAM).** MWE# should be used as the write enable for the memory data bus. This signal has programmable buffer size selection.
MWE#	O 3.3 V	**Memory Write Enable (EDO/FPM/SDRAM).** MWE# should be used as the write enable for the memory data bus. This signal has programmable buffer size selection.
SRAS[A,B]#	O 3.3 V	**SDRAM Row Address Strobe (SDRAM).** When asserted, this signal latches Row Address on the positive edge of the clock. This signal also allows Row access and precharge. Two copies are provided for loading purpose. These signals have programmable buffer size selection.
SCAS[A,B]#	O 3.3 V	**SDRAM Column Address Strobe (SDRAM).** When asserted, this signal latches Column Address on the positive edge of the clock. This signal also allows Column access. Two copies provided for loading purpose. These signals have programmable buffer size selection.
CKE/MAA0	O 3.3 V	**SDRAM Clock Enable (SDRAM).** SDRAM clock enable pin. When this signal is negated, SDRAM enters power down mode. This signal is also muxed to provide a second copy of memory address MA0 (MAA0). The MA function is selected via DRT[bit2] (offset 67h). MTXC negates CKE (and CKEB) when SUSSTAT1# is asserted. Note that MTXC asserts CKE (and CKEB) for all rows (i.e., CKE and CKEB cannot be selectively asserted for certain rows and negated for other rows).

Name	Type	Description
CKEB/MAA1	O 3.3 V	**SDRAM Clock Enable (SDRAM) (second copy).** SDRAM clock enable pin. When this signal is negated, SDRAM enters into power down mode. Note that this signal is not implemented in the "Suspend Well" and should not be used if suspend to RAM (STR) is implemented. This signal is also muxed to provide a second copy of memory address MA1 (MAA1). The MA function is selected via DRT[bit2] (offset 67h). MTXC negates CKE (and CKEB) when SUSSTAT1# is asserted. Note that MTXC asserts CKE (and CKEB) for all rows (i.e., CKE and CKEB cannot be selectively asserted for certain rows and negated for other rows).
MD[63:0]	I/O 3.3V/5V	**Memory Data.** These signals are connected to the DRAM data bus. These signals have internal pull-down resistors

2.1.3. SECONDARY CACHE INTERFACE

Name	Type	Description
CADV#	O 3.3V	**Cache Advance.** Assertion causes the PBSRAM in the secondary cache to advance to the next QWord in the cache line.
CADS#	O 3.3V	**Cache Address Strobe.** Assertion causes the PBSRAM in the secondary cache to load the PBSRAM address register from the PBSRAM address pins.
CCS#	O 3.3V	**Cache Chip Select (CCS#).** The second level cache will power up, if necessary, and perform an access if this signal is asserted when CADS# is asserted. The second level cache will power down if this signal is negated when CADS# is asserted. When CCS# is negated the second level cache will ignore ADS#. If CCS# is asserted when ADS# is asserted, the second level cache will power up, if necessary, and perform an access.
COE#	O 3.3V	**Cache Output Enable.** The secondary cache data RAMs drive the CPUs data bus when COE# is asserted.
GWE#	O 3.3V	**Global Write Enable.** GWE# assertion causes all the byte lanes to be written into the secondary cache data RAMs, if they are powered up.
BWE#	O 3.3V	**Byte Write Enable.** Asserted low with GWE#=HIGH to enable using host's BE[7:0]# to be used to control byte lanes to pipeline burst SRAM cache.
TIO[7:0]	I/O 3.3V/5V	**Tag Address.** These are inputs during CPU accesses and outputs during second level cache line fills and second level cache line invalidates due to inquire cycles. These signals have internal pull-down resistors.
TWE#	O 3.3V	**Tag Write Enable.** When asserted, new state and tag addresses are written into the external tag.
KRQAK/ CS4_64#	I/O 3.3V	**KRQAK/Chip Select 4 (for 64-Mb Technology).** This pin is a dual-function signal. KRQAK is used in a DRAM Cache L2 implementation and is a bi-directional refresh request/acknowledge. The CS4_64# function is used to generate the fifth chip select line in a SDRAM L2 Cache implementation that supports five rows of 64-Mbit SDRAM. During a hard reset, this signal is sampled to determine if DRAM cache is in the system (see MTXC Strapping options). This signal has a weak internal pull-down. If SDRAMC[bit 1]=1 and DRAM cache is not present in the system (indicated by CEC[bit 5]=0, offset 53h), the CS4_64# function is selected. If DRAM cache is in the system or SDRAMC[bit 1] (offset 54h)=0, then KRQAK is used to drive the KRQAK function.

2.1.4. PCI INTERFACE

Name	Type	Description
AD[31:0]	I/O 3.3/5V	**Address/Data.** The standard PCI address and data lines. Address is driven with FRAME# assertion, data is driven or received in following clocks.
C/BE[3:0]#	I/O 3.3/5V	**Command/Byte Enable.** The command is driven with FRAME# assertion, byte enables corresponding to supplied or requested data is driven on following clocks.
FRAME#	I/O 3.3/5V	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
DEVSEL#	I/O 3.3/5V	**Device Select.** This signal is driven by the MTXC when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
IRDY#	I/O 3.3/5V	**Initiator Ready.** Asserted when the initiator is ready for a data transfer.
TRDY#	I/O 3.3/5V	**Target Ready.** Asserted when the target is ready for a data transfer.
STOP#	I/O 3.3/5V	**Stop.** Asserted by the target to request the master to stop the current transaction.
LOCK#	I/O 3.3/5V	**Lock.** Used to establish, maintain, and release resource locks on PCI.
REQ[3:0]#	I 3.3/5V	**PCI Request.** PCI master requests for PCI bus.
GNT[3:0]#	O 3.3V	**PCI Grant.** Permission is given to the master to use PCI.
PHLD#	I 3.3/5V	**PCI Hold.** This signal comes from the expansion bridge. It is the bridge request for PCI. The MTXC will drain the DRAM write buffers, drain the CPU-to-PCI posting buffers, and acquire the host bus before granting via PHLDA#.
PHLDA#	O 3.3V	**PCI Hold Acknowledge.** This signal is driven by the MTXC to grant PCI to the expansion bridge. PHLDA# protocol has been modified to include support for passive release.
PAR	I/O 3.3/5V	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]. This signal should be pulled high through a weak external pull-up resistor.
CLKRUN#	I/O 3.3/5V	**CLOCK RUN.** An open drain output and also an input. MTXC requests the central resource (PIIX4) to start, or maintain the PCI clock by the assertion of CLKRUN#. MTXC will tri-state CLKRUN# upon negation of reset (since CLK is running upon negation of reset). External pull-up is required. Note: This signal should be connected to the PIIX4 CLKRUN# pin. However, if it is left as a no connect on the MTXC, it must be pulled low through a 100Ω (pull-down resistor.
RST#	I 3.3/5V	**Reset.** When asserted this signal asynchronously resets the MTXC. The PCI signals also tri-state compliant to PCI Rev 2.0 and 2.1 specifications.

2.1.5. TEST AND CLOCK

Name	Type	Description
TEST#	I 3.3/5V	**Test In.** NAND tree mode is activated by driving this pin low. The test mode selected depends on the state of REQ[3:0]#. This pin should be pulled high with an external pull-up during normal operation.
HCLKIN	I 3.3/2.5V	**Host Clock In.** This pin receives a buffered host clock. This clock is used by all of the MTXC logic that is in the Host clock domain.
PCLKIN	I 3.3/5V	**PCI Clock In.** This pin receives a buffered divide-by-2 host clock. This clock is used by all of the MTXC logic that is in the PCI clock domain.

2.1.6. POWER MANAGEMENT

Name	Type	Description
SUSCLK	I 3.3V	**Suspend Clock.** The signal is a 32 KHz input for DRAM refresh circuitry and clocking events in suspend state. The DRAM refresh during suspend and non-suspend states is performed based on this clock. This signal has an internal pull-down resistor.
SUSSTAT1#	I 3.3V	**Suspend Status.** SUSSTAT1# indicates MTXC's power plane status during suspend mode. SUSSTAT1#, along with SUSCLK and RST#, define the suspend protocol between MTXC and PIIX4. This signal has an internal pull-up resistor.

2.1.7. POWER AND GROUND PINS

Name	Type	Description
V_{CC}	3.3V	**Main voltage supply.** These pins are the primary voltage supply for the MTXC core and I/O periphery and must be connected to 3.3V.
V_{CC} (CPU)	3.3V or 2.5V	**CPU Interface Voltage Supply.** These pins are the primary voltage supply for the MTXC Host periphery and must be connected to either 2.5V or 3.3V, depending on the voltage level of the CPU interface. Refer to the Power sequencing requirements section for additional details.
V_{CC} (SUS)	3.3V	**Suspend Well Voltage Supply.** These pins are the primary voltage supply for the MTXC suspend logic and I/O. If suspend to RAM is supported, these pins should be on an isolated power plane; otherwise, they can be connected to the same 3.3V source used for the V_{CC} pins.
V_{CC}5REF	3.3V or 5V	**Voltage Reference.** This pin is tied to 5V through a small external power sequencing circuit, if MTXC signals are required to be 5V Tolerant. In a non 5V tolerant system (i.e. 3.3V only system), this signal can be tied directly to V_{CC}. Refer to the Power sequencing requirements section for additional details.
V_{SS}	0V	**Ground.** These pins are the ground for the MTXC.

2.2. MTXC Strapping Options

Name	Type	Description
SCS	A[31:30]	**Secondary Cache Size.** Described in the Cache Control Register bits 7:6.
L2RAMT	A[29:28]	**Initial L2 RAM Type.** Described in the Cache Control Register bits 5:4.
DRAM Cache	KRQAK	**DRAM Cache L2 Present Upon Reset Negation.** This bit is sampled to detect DRAM L2 cache. If sampled high, a DRAM Cache is present. A weak pulldown is provided internally. A DRAM cache module should implement a pull-up on this pin that overrides the weak pulldown. BIOS does not have to be aware of this, this information is used by the MTXC to maintain optimal Pburst timings.
25VD	A26	**2.5V Voltage Detection.** This bit is used to determine the voltage level (3.3V or 2.5V) of the host clock connected to the host clock pin and the voltage on the V_{CC}(CPU) pins. An external pull-down or pull-up resistor is required on this pin (pulled down for 2.5V and pulled up for 3.3V).
HFD	A27	**Frequency Detection.** BIOS can use this bit to determine if the system is 60 MHz (external pull-up) or 66 MHz (no strapping is present) as described in the DRTH Register, bit 7. DRTH[bit 7] register is initialized with the inverted value of pin A27 upon reset negation. The A27 input buffer includes a weak pulldown resistor which will force DRTH[bit 7] to default to 1 if no strapping is present.

2.3. Power Planes

The MTXC has three primary internal power planes. These power planes permit parts of the MTXC to power down to conserve battery life. Table 1 shows the internal planes and their uses.

Table 1. MTXC Internal Power Planes

Power Plane	Description	Signals Powered	V_{CC} Pins	GND Pins
SUSPEND	Contains the logic needed to resume from the Suspend-to-RAM state. This power supply should be capable of providing a "trickle" current. The input signals attached to the SUSPEND power plane Do Not Support 5V Input Levels. These signals must not exceed V_{CC} (SUS).	MWE#, MWEB#, CKE, RAS[5:0]# [1], CAS[7:0]#, SUSCLK, SUSSTAT1#	V_{CC} (SUS)	V_{SS}
CPU	CPU Interface signals have a separate supply so that the CPU interface can be 3.3V for existing CPUs and can be 2.5V on future CPUs.	A[31:3], BE[7:0]#, ADS#, BRDY#, NA#, AHOLD, EADS#, BOFF#, HITM#, M/IO#, D/C#, W/R#, HLOCK#, CACHE#, KEN#/INV, SMIACT#, HD[63:0], HCLKIN	V_{CC} (CPU)	V_{SS}
V_{CC}5REF	The V_{CC}5REF signal provides protection for the 5V tolerant 3.3V signals.	PCI Bus Input and I/O, MD[63:0], TIO[7:0], PCLKIN, TEST#	V_{CC}5REF	V_{SS}
MAIN	Contains all the rest of the MTXC logic. This plane is powered by the main system power supply.	All Other Signal Pins	V_{CC}	V_{SS}

NOTES:

1. KRQAK is not part of the suspend well. When this pin is used as the 5th RAS line (CS4_64), special considerations must be taken.

2.4. Power Sequencing Requirements

The Vcc5REF signal must be tied to 5V in a system requiring 5V tolerance. In a 5V tolerant system, Vcc5REF must power up before or simultaneous to Vcc. It must power down after or simultaneous to Vcc. At any time, Vcc5REF should not be more than 0.6 volts below Vcc. In a non-5V tolerant system (3.3V only), this signal can be tied directly to Vcc. In this case, there are no sequencing requirements. Refer to Figure 2 for an example circuit schematic which may be used to ensure the proper Vcc5REF sequencing.

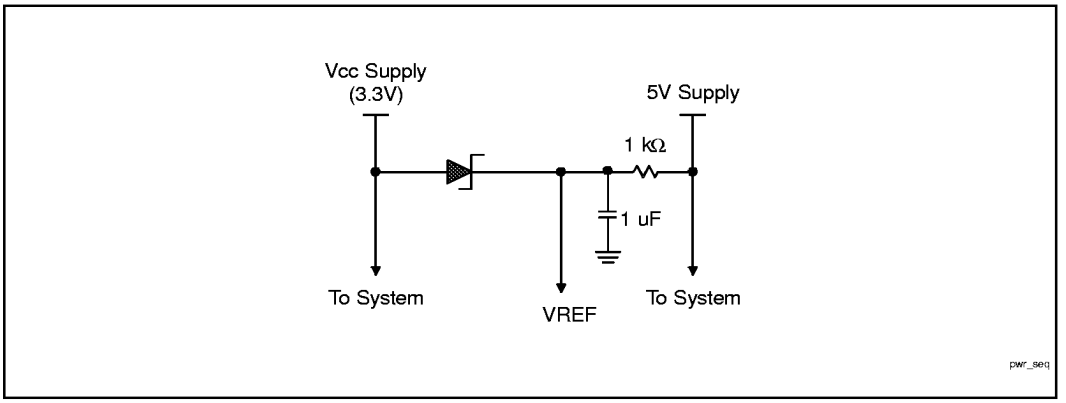


Figure 2. Example Vcc5REF Sequencing Circuit

The Vcc(CPU) power plane is tied to either 2.5 volts or 3.3 volts, depending on the voltage level of the CPU interface. In a system that ties this power plane to 2.5 volts, the Vcc(CPU) pins must power up after or simultaneous to Vcc. It must power down before or simultaneous to Vcc. At any time, Vcc should not be more than 1.2 volts below the Vcc(CPU) plane.

2.5. Signal States During And After A Hard Reset

Table 2 shows the state of all the MTXC output and bi-directional signals when RST# is asserted. An undefined state means that the signal is driven either high or low, but not tri-stated.

Table 2. Signal States During/After Reset

Name	State during RST#	State After RST#
A[31:3]	Low	Tri-State
BRDY#	High	High
NA#	High	High
AHOLD	High	Low
EADS#	High	High
BOFF#	High	High
KEN#/INV	Low	Low
HD[63:0]	Tri-State	Tri-State
RAS[5:0]# or CS[5:0]#	Undefined	High
CAS[7:0]# or DQM[7:0]	Undefined	Undefined
MA[11:0], BA1,MA13	Undefined	Undefined
MWE#, MWEB#	High	High
SRAS[A,B]#	High	High
SCAS[A,B]#	High	High
CKE,CKEB	Undefined	High
MD[63:0]	Tri-State	Tri-State
CADV#	High	High
CADS#	High	High

Table 2. Signal States During/After Reset

Name	State during RST#	State After RST#
CCS#	Low	Low
COE#	High	High
GWE#	High	High
BWE#	High	High
TIO[7:0]	Low	Tri-State
TWE#	Low	High
KRQAK	Input	Input
AD[31:0]	Low	Tri-State
C/BE[3:0]#	Low	Tri-State
FRAME#	Tri-State	Tri-State
DEVSEL#	Tri-State	Tri-State
IRDY#	Tri-State	Tri-State
TRDY#	Tri-State	Tri-State
STOP#	Tri-State	Tri-State
LOCK#	Tri-State	Tri-State
GNT[3:0]#	Tri-State	High
PHLDA#	High	High
PAR	Low	Undefined
CLKRUN#	Tri-State	Tri-State

3.0. REGISTER DESCRIPTION

The MTXC contains two sets of software accessible registers (I/O Mapped and PCI configuration registers), accessed via the Host CPU I/O address space. The I/O mapped registers control access to PCI configuration space. Configuration registers residing in PCI configuration space used to specify PCI configuration, DRAM configuration, cache configuration, operating parameters and optional system features.

The MTXC internal registers (both I/O Mapped and PCI Configuration registers) are only accessible by the Host CPU and cannot be accessed by PCI masters. The registers can be accessed as Byte, Word (16-bit), or DWord (32-bit) quantities, with the exception of CONFADD, which can only be accessed as a DWord. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field). The following nomenclature is used for access attributes:

RO **READ ONLY**. If a register is read only, writes to this register have no effect.

R/W **READ/WRITE**. A register with this attribute can be read and written.

R/WC **READ/WRITE CLEAR**. A register bit with this attribute can be read and written. However, a write of 1 clears (sets to 0) the corresponding bit and a write of 0 has no effect.

Some of the MTXC registers described in this section contain reserved bits. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back.

In addition to reserved bits within a register, the MTXC contains address locations in the PCI configuration space that are marked "Reserved" (Table 3). The MTXC responds to accesses to these address locations by completing the Host cycle and returning a value of zero. The registers marked as "Undefined" will return a non-zero value and are defined as read only. Software should not write to reserved or undefined MTXC configuration locations in the device-specific region (above address 3Fh).

Upon RESET, the MTXC sets its internal configuration registers to predetermined **default** states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, cache configuration, operating parameters and optional system features that are applicable, and to program the MTXC registers accordingly.

3.1. I/O Mapped Registers

The MTXC contains three registers that reside in the CPU I/O address space—the Configuration Address (CONFADD) Register, the Configuration Data (CONFDATA) Register, and the PM2 Register Block. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3.1.1. PM2_CNTRL—PM2 REGISTER BLOCK

I/O Address: 0022h
Default Value: 00h
Access: Read/Write

Bit	Descriptions
7:1	**Reserved.**
0	**Arbiter Disable (ARB_DIS).** When ARB_DIS=1, the MTXC does not respond to any REQ# signals (including PHOLD#) going active until this bit is set back to 0. This bit is used to disable bus master accesses prior to placing the CPU in a stop clock state. This bit maintains cache coherency by preventing PCI masters from gaining access to the PCI bus and causing snoop cycle activity. MCTL[Bit 6] (offset 79h) must be set to 1 before this register is accessible.

3.1.2. CONFADD—CONFIGURATION ADDRESS REGISTER

I/O Address: 0CF8h (Accessed as a DWord)
Default Value: 00000000h
Access: Read/Write

CONFADD is a 32-bit register accessed only when referenced as a DWord. A Byte or Word reference will "pass through" the Configuration Address Register onto the PCI bus. The CONFADD register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Descriptions
31	**Configuration Enable (CONE).** 1=Enable. 0=Disable.
30:24	**Reserved.**
23:16	**Bus Number.** When the Bus Number is programmed to 00h the target of the Configuration Cycle is either the MTXC or the PCI Local Bus that is directly connected to the MTXC, depending on the Device Number field. A type 0 Configuration Cycle is generated on PCI if the Bus Number is programmed to 00h and the MTXC is not the target. If the Bus Number is non-zero a type 1 configuration cycle is generated on PCI with the Bus Number mapped to AD[23:16] during the address phase.
15:11	**Device Number.** This field selects one agent on the PCI bus selected by the Bus Number. During a Type 1 Configuration cycle this field is mapped to AD[15:11]. During a Type 0 Configuration Cycle this field is decoded and one of AD[31:11] is driven to a 1. The MTXC is always Device Number 0.
10:8	**Function Number.** This field is mapped to AD[10:8] during PCI configuration cycles. This allows the configuration registers of a particular function in a multi-function device to be accessed. The MTXC responds to configuration cycles with a function number of 000b; all other function number values attempting access to the MTXC (Device Number=0, Bus Number=0) will generate a type 0 configuration cycle onto the PCI bus with no IDSEL asserted, which will result in a master abort.
7:2	**Register Number.** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to AD[7:2] during PCI configuration cycles.
1:0	**Reserved.**

3.1.3. CONFDATA—CONFIGURATION DATA REGISTER

I/O Address: 0CFCh
Default Value: 00000000h
Access: Read/Write

CONFDATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFDATA is determined by the contents of CONFADD.

Bit	Descriptions
31:0	**Configuration Data Window (CDW).** If bit 31 of CONFADD is 1, any I/O reference that falls in the CONFDATA I/O space is mapped to configuration space using the contents of CONFADD.

PCI CONFIGURATION SPACE MAPPED REGISTERS

The PCI Bus defines a slot based "configuration space" that allows each device to contain up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space—**Configuration Read** and **Configuration Write**. While memory and I/O spaces are supported by the Pentium microprocessor, configuration space is not supported. The PCI specification defines two mechanisms to access configuration space, Mechanism #1 and Mechanism #2. The MTXC supports only Mechanism #1. The bus cycles used to access MTXC internal configuration registers are described later in the PCI cycle timings section.

The configuration access mechanism makes use of the CONFADD Register and CONFDATA Register. To reference a configuration register, a DWord I/O write cycle is used to place a value into CONFADD that specifies the PCI bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFADD[31] must be 1 to enable a configuration cycle. CONFDATA then becomes a window onto four bytes of configuration space specified by the contents of CONFADD. Any read or write to CONFDATA will result in the MTXC translating CONFADD into a PCI configuration cycle.

Type 0 Access

If the Bus Number field of CONFADD is 0 a Type 0 Configuration cycle is performed on PCI. CONFADD[10:2] is mapped directly to AD[10:2]. The Device Number field of CONFADD is decoded onto AD[31:11]. The MTXC is Device #0 and does not pass its configuration cycles to PCI so AD11 will never be asserted. Device #1 will assert AD12, Device #2 will assert AD13, and so forth up to Device #20 which will assert AD31. Only one AD line is asserted at a time. All device numbers higher than 20 cause a type 0 configuration access with no IDSEL asserted, which will result in a Master Abort.

Type 1 Access

If the Bus Number field of CONFADD is non-zero a Type 1 Configuration cycle is performed on PCI. CONFADD[23:2] is mapped directly to AD[23:2]. AD[1:0] are driven to 01 to indicate a Type 1 Configuration cycle. All other lines are driven to 0.

Table 3. MTXC Configuration Space

Address Offset	Register Symbol	Register Name	Access
PCI Specific Registers			
00–01h	VID	Vendor Identification	RO
02–03h	DID	Device Identification	RO
04–05h	PCICMD	PCI Command Register	R/W
06–07h	PCISTS	PCI Status Register	RO, R/WC
08	RID	Revision Identification	RO
09–0Bh	CLASSC	Class Code	RO
0Ch	—	Reserved	—
0Dh	MLT	Master Latency Timer	R/W
0Eh	HEDT	Header Type	—
0Fh	BIST	BIST Register	R/W
10–3Fh	—	Reserved	—
MTXC Specific Registers			
40–4Eh	—	Reserved	—
4Fh	ACON	Arbitration Control	R/W
50h	PCON	PCI Control	R/W
51h	—	Reserved	—
52h	CC	Cache Control	R/W
53	CEC	Extended Cache Control	R/W
54–55h	SDRAMC	SDRAM Control	RW
56h	DRAMEC	DRAM Extended Control	R/W
57h	DRAMC	DRAM Control	R/W
58h	DRAMT	DRAM Timing	R/W
59–5Fh	PAM[6:0]	Programmable Attribute Map (7 registers)	R/W
60–65h	DRB[5:0]	DRAM Row Boundary (6 registers)	R/W
66h	—	Reserved	—
67h	DRTH	DRAM Row Type High	R/W
68h	DRTL	DRAM Row Type Low	R/W

Table 3. MTXC Configuration Space

Address Offset	Register Symbol	Register Name	Access
69–6Ah	—	Undefined	RO
6B–6Fh	—	Reserved	—
70h	MTT	Multi-Transaction Timer	R/W
71h	ESMRAMC	Extended System Management RAM Control	R/W
72h	SMRAMC	System Management RAM Control	R/W
73h	—	Reserved	—
74h	—	Undefined	RO
76–78h	—	Reserved	—
78h	—	Undefined	RO
79	MCTL	Miscellaneous Control Register	R/W
7A–FCh	—	Reserved	—
FDh	—	Undefined	RO
FE–FFh	—	Reserved	—

3.1.4. VID—VENDOR IDENTIFICATION REGISTER

Address Offset: 00–01h
Default Value: 8086h
Attribute: Read Only

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identify any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number.** This is a 16-bit value assigned to Intel.

3.1.5. DID—DEVICE IDENTIFICATION REGISTER

Address Offset: 02–03h
Default Value: 7100h
Attribute: Read Only

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number.** This is a 16 bit value assigned to the MTXC.

3.1.6. PCICMD—PCI COMMAND REGISTER

Address Offset: 04–05h
Default: 06h
Access: Read/Write

This 16-bit register provides basic control over the MTXC's ability to respond to PCI cycles. The PCICMD Register in the MTXC enables and disables the assertion of SERR# and PCI master accesses to main memory.

Bit	Description
15:10	**Reserved**.
9	**Fast Back-to-Back (FB2B). (Not implemented)** This bit is hardwired to 0.
8	**SERR# Enable (SERRE). (Not implemented)** This bit is hardwired to 0.
7	**Address/Data Stepping. (Not implemented)** This bit is hardwired to 0.
6	**Parity Error Enable (PERRE). (Not implemented)** This bit is hardwired to 0.
5	**Video Pallet Snooping (VPS). (Not implemented)** This bit is hardwired to 0.
4	**Memory Write and Invalidate Enable (MWIE). (Not implemented)** This bit is hardwired to 0. The MTXC will never use the Memory Write and Invalidate PCI command.
3	**Special Cycle Enable (SCE). (Not implemented)** This bit is hardwired to 0, as the MTXC does not respond to PCI special cycles.

Bit	Description
2	**Bus Master Enable (BME). (Not implemented)** This bit is hardwired to 1. The MTXC does not support disabling of its bus master capability on the PCI Bus.
1	**Memory Access Enable (MAE).** When MAE=1, the MTXC permits PCI masters to access main memory if the PCI address selects enabled DRAM space. When MAE=0, the MTXC does not respond to main memory accesses.
0	**I/O Access Enable (IOAE). (Not implemented)** The MTXC does not respond to PCI I/O cycles. This bit is hardwired to 0.

3.1.7. PCISTS—PCI STATUS REGISTER

Address Offset: 06–07h
Default Value: 0200h
Access: Read Only, Read/Write Clear

PCISTS is a 16-bit status register that reports the occurrence of a PCI master abort and PCI target abort. PCISTS also indicates the DEVSEL# timing that has been set by the MTXC hardware.

Bit	Description
15	**Detected Parity Error (DPE).** This bit is hardwired to 0, as PCI received parity checking is not implemented by the MTXC.
14	**Signaled System Error (SSE).** This bit is hardwired to 0 as MTXC does not support SERR#.
13	**Received Master Abort Status (RMAS).** When the MTXC terminates a Host-to-PCI transaction (MTXC is a PCI master) with an unexpected master abort, this bit is set to 1. Note that master abort is the normal and expected termination of PCI special cycles. Software resets this bit to 0 by writing a 1 to it.
12	**Received Target Abort Status (RTAS).** When a MTXC-initiated PCI transaction is terminated with a target abort, RTAS is set to 1. Software resets RTAS to 0 by writing a 1 to it.
11	**Signaled Target Abort Status (STAS).** This bit is hardwired to 0, as the MTXC never terminates a PCI cycle with a target abort.
10:9	**DEVSEL# Timing (DEVT).** This 2-bit field indicates the timing of the DEVSEL# signal when the MTXC responds as a target, and is hardwired to the value 01b (medium) to indicate the slowest time that DEVSEL# is generated.
8	**Data Parity Detected (DPD).** This bit is hardwired to 0, as PERR# is not implemented.
7	**Fast Back-to-Back (FB2B).** This bit is hardwired to 0, as fast back to back cycle generation is not implemented.
6	**User Defined Format (UDF).** This bit is hardwired to 0. This is because the MTXC does not contain any configurations that depend on the environment, such as network frequencies.
5	**66-MHz PCI Capable (66C).** This bit is hardwired to 0. The MTXC does not interface to 66-MHz PCI.
4:0	**Reserved**.

3.1.8. RID—REVISION IDENTIFICATION REGISTER

Address Offset: 08h
Default Value: 01h
Access: Read Only

This register contains the revision number of the MTXC. These bits are read only and writes to this register have no effect.

Bit	Description
7:0	**Revision Identification Number.** This is an 8-bit value that indicates the revision identification number for the MTXC.

3.1.9. CLASSC—CLASS CODE REGISTER

Address Offset: 09–0Bh
Default Value: 00h
Access: Read Only

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the MTXC. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Description
23:16	**Base Class Code (BASEC).** 06=Bridge device.
15:8	**Sub-Class Code (SCC).** 00h=Host Bridge.
7:0	**Programming Interface (PI).** 00h=Hardwired as a Host-to-PCI Bridge.

3.1.10. MLT—MASTER LATENCY TIMER REGISTER

Address Offset: 0Dh
Default Value: 00h
Access: Read/Write

MLT is an 8-bit register that controls the amount of time the MTXC, as a bus master, can burst data on the PCI Bus. The Count Value is an 8-bit quantity. However MLT[2:0] are reserved and assumed to 0 when determining the Count Value. MLT is used to guarantee the host CPU a minimum amount of the system resources.

The number of clocks programmed in the MLT represents the guaranteed time slice (measured in PCI clocks) allotted to the MTXC, after which it must surrender the bus as soon as other PCI masters request the bus. The default value of MLT is 00h or 0 PCI clocks.

Bit	Description
7:3	**Master Latency Timer Count Value**
2:0	**Reserved.** Read as 0s

3.1.11. HEDT—HEADER TYPE REGISTER

Address Offset: 0Eh
Default Value: 00h
Access: Read Only

This register contains the Header Type of the MTXC. This code is 00h indicating that the MTXC's configuration space map follows the basic format.

Bit	Description
7:0	**Device Type (DEVICET).** 00h=Indicates a basic configuration space format.

3.1.12. BIST—BIST REGISTER

Address Offset: 0Fh
Default Value: 00h
Access: Read/Write

The Built In Self Test (BIST) function is not supported by the MTXC. Writes to this register have no effect.

Bit	Description
7	**BIST Supported.** This read only bit is always set to 0, disabling the BIST function. Writes to this bit position have no effect.
6	**Start BIST.** This function is not supported and writes have no effect.
5:4	**Reserved**.
3:0	**Completion Code.** This read only field always returns 0 when read and writes have no effect.

3.1.13. ACON—ARBITRATION CONTROL REGISTER

Address Offset: 4Fh
Default Value: 00h
Access: Read/Write

The ACON Register enables and disables features related to PCI arbitration and PCI 2.1 compliance.

Bit	Description
7	**Extended CPU-to-PIIX4 PHLDA# Signaling Enable (XPLDE).** When XPLDE=1, the MTXC adds the following additional signaling to signal PHLDA# (i.e., in addition to the normal CPU/PIIX4 PHOLD/PHLDA# protocol): 1. Whenever the North bridge begins a PCI read/write transaction, it will assert PHLDA# for 1 PCLK within the address phase of the transaction. 2. If the CPU is attempting a LOCKed cycle AND LOCK has been established (i.e. PLOCK# was seen negated in address phase), the PHLDA# remains asserted for one additional clock following the address phase. This bit should be set to 1 anytime both Passive Release and Delayed Transaction are enabled in the PIIX4. Passive release and delayed transaction are enabled via bits 1 and 0 in PIIX4 register 82h (function 0). When bit 7 in this register is set to 1 (enabled), Bit 7 in PIIX4 Register, 6A (Function 0) must also be set to 1. When enabling these two bits, enable Bit 7 in the PIIX4 first, followed by bit 7 in this register. When disabling these two bits, disable Bit 7 in this register first, followed by bit 7 in the PIIX4.
6:0	**Reserved.**

3.1.14. PCON—PCI CONTROL REGISTER

Address Offset: 50h
Default Value: 00h
Access: Read/Write

The PCON Register enables and disables features related to the PCI bus that are not already covered in the required PCI space.

Bit	Description
7:4	**Reserved.**
3	**PCI Concurrency Enable (PCE).** 1=CPU can access DRAM and L2 while a non-PIIX4 PCI master is targeting Peer PCI devices. 0 (default)=CPU is held off of the bus during all PCI master cycles. This bit should be set to 1 by BIOS during normal operation.
2:0	**Reserved.**

3.1.15. CC—CACHE CONTROL REGISTER

Address Offset: 52h
Default Value: SSSS0010 (S=Strapping option)
Access: Read/Write

This 8-bit register defines the secondary cache operations. The CC register enables and disables the second level cache, adjusts cache size, selects the cache write policy, selects the caching policy when CACHE# is negated on reads, informs the MTXC how the SRAMs are connected, and defines the cache SRAM type. After a hard reset, CC[7:4] reflect the signal levels on the Host address lines A[31:28].

Bit	Description
7:6	**Secondary Cache Size (SCS).** This field reflects the inverted signal level on the A[31:30] pins at the rising edge of the RESET signal. The options are: **Bits[7:6] Secondary Cache Size** 00 Cache not populated 01 256 Kbytes 10 512 Kbytes 11 Reserved The RESET values can be overwritten with subsequent writes to the CC Register. **NOTE** 1. When bits[7:6]=00, the secondary cache is disabled. 2. When bits[7:6]≠00, the FLCE bit must also be set to 1 (L2 cache cannot be enabled unless the L1 cache is also enabled).

Bit	Description
5:4	**L2 SRAM Type (L2SRAMT).** This field reflects the inverted signal level on the A[29:28] pins at the rising edge of the RESET signal. The RESET values can be overwritten with subsequent writes to the CC Register. The options are: **Bits[5:4] SRAM Type** 00 Pipelined Burst SRAM 01 Reserved 10 Reserved 11 Two banks of Pipelined Burst **NOTE** When 512-KB Pipelined Burst SRAM L2 mode is selected (via SCS and SRAMT), CCS# is negated after NA# is asserted, and reasserted after a pipelined ADS# is detected. CADS# is asserted along with the final BRDY# for a cycle if a pipelined cycle is outstanding (i.e., an ADS# was detected).
3	**NA Disable (NAD).** 1=Disable. 0=Enable. When disabled, MTXC never asserts the NA# pin. When enabled, NA# assertion is dependent on the cache type and size selected (via SRAMT, SCS). Note that NAD must be set to 1 if the NA# pin of the MTXC is not connected to the processor. This bit should be set to 0 for normal operation in systems that connect NA# to the processor.
2	**Reserved.**
1	**Secondary Cache Force Miss or Invalidate (SCFMI).** When set to a 1, the L2 hit/miss detection is disabled, and all tag lookups result in a miss. If the L2 is enabled, then the cycle is processed as a miss (as described in Chapter 4.2). If the L2 is populated but disabled (FLCE=0), then when SCFMI is set to a 1, any CPU read cycle will invalidate the selected tag entry. When SCFMI is set to a 0, normal L2 cache hit/miss detection and cycle processing occurs. Software can flush the cache (cause all modified lines to be written back to DRAM) by setting SCFMI to a 1 with the L2 enabled (non-zero SCS, FLCE=1), and reading all L2 cache tag address locations. See FLCE bit description for FLCE/SCFMI interaction.
0	**First Level Cache Enable (FLCE).** 1=Enable. 0=Disable. When FLCE=1, the MTXC responds to CPU cycles with KEN# asserted for cacheable memory cycles. When FLCE=0, KEN# is always negated. This prevents new cache line fills to either the first level or second level cache. The FLCE/SCFMI interaction is summarized below. Note that “Normal L2 operation” is further dependent on the SCS field programming. **FLCE SCFMI L2 Result** 0 0 L2 disabled 0 1 L2 disabled, MTXC tag invalidate on reads 1 0 Normal L2 operation (dependent on SCS) 1 1 L2 enabled, MTXC miss forced on reads/writes (Note that writes to the cache are also forced as misses, making it possible to create incoherent DRAM/L2 data.)

3.1.16. CEC—EXTENDED CACHE CONTROL REGISTER

Address Offset: 53h
Default Value: 14h
Access: Read/Write, Read Only

This 8-bit register defines the refresh rate (in HCLKs) for a DRAM CACHE L2 cache implementation, if enabled.

Bit	Description
7:6	**Reserved**
5	**DRAM CACHE L2 Present (ML2)—RO.** When ML2=1, an L2 DRAM CACHE is present.
4:0	**DRAM Cache L2 Refresh Timer (MCRT)—R/W.** These bits determine the time the MTXC remains idle during a DRAM cache refresh sequence. The smallest value for the MRCT must be 04h; otherwise, the MTXC will not function properly. The default value sets the timer refresh to 20 HCLKs.

3.1.17. SDRAMC—SDRAM CONTROL REGISTER

Address Offset: 54–55h
Default Value: 0000h
Access: Read/Write

Bit	Description
15:9	**Reserved.**
8:6	**Special SDRAM Mode Select (SSMS).** These bits select 1 of 4 special SDRAM modes for testing and initialization. Note that the NOP command must be programmed first before any other command can be issued. After the DRAM detection process has completed, bits[7:5] must remain at "000" during normal DRAM operation. **Bits[8:6] Mode** 000 **Normal SDRAM mode (default).** 001 **NOP Command Enable (NOPCE).** This mode forces all CPU cycles to DRAM to generate a SDRAM NOP command on the memory interface. 010 **All Banks Precharge Command Enable (ABPCE).** This setting enables a mode where all CPU cycles to DRAM are converted to an all banks precharge command on the memory interface. Used for BIOS Detection algorithm. 011 **Mode Register Command Enable (MRCE).** This setting enables a mode where all CPU cycles to DRAM are converted into MRS commands to the memory interface. The command is driven on the MA[11:0] lines. MA[2:0] needs to be always driven to 010 for burst of 4 mode. MA3 needs to be always driven to 1 for interleave wrap type mode. MA4 needs to be driven to the value in the CAS# Latency bit. MA[6:5] needs to be always driven to 01. MA[11:7] needs to be always driven to 00000. The BIOS will select an appropriate host address for each Row of memory such that the right commands are generated on the Memory Address MA[11:0] lines. The BIOS needs to be cognizant of the mapping of the Host addresses to Memory addresses. e.g. A Host address of 1D0h will set up the Mode registers in Row 0 of SDRAM with Burst length of 4, Wrap type of interleaved, and CAS latency of 3. 100 **CBR Cycle Enable (CBRC).** This setting enables a mode where all CPU cycles to DRAM are converted to SDRAM CBR refresh cycles on the memory interface. 101 **Reserved** 11X **Reserved**

Bit	Description
5	**RAS# to CAS# Override (RCO).** When set to 1, and the CL bit (CAS Latency) is 0 (CAS Latency=3), then a RAS# to CAS# delay of 2 HCLKs is provided for SDRAM. When set to 0, a RAS# to CAS# delay for SDRAM is determined by the CL bit.
4	**CAS# Latency (CL).** When set to 1, a CAS# latency of 2 is used for all SDRAM cycles. When reset to 0, CAS# latency of 3 is used for all SDRAM cycles.
3	**RAS# Timing (RT).** This bit controls RAS# precharge, RAS# active to precharge time and Refresh to RAS# active delay (in HCLKs): **Bit 3 / RAS# Precharge / RAS# act. to Precharge / Refresh to RAS# act.** 0 / 3 / 5 / 8 1 / 3 / 4 / 7
2	**Reserved.**
1	**64-Mbit Technology Enable (64MTEN).** 1=Enable. 0=Disable. When set to 0, the MTXC does not support 64-Mbit SDRAM devices. In this mode, the MTXC supports 4-Mbit, 16-Mbit, and 64-Mbit technology for EDO/FPM systems and 4 Mbit and 16 Mbit for SDRAM systems (i.e., 64 Mbit not supported in SDRAM systems). When set to 1, the MTXC supports 4 Mbit, 16 Mbit, and 64 Mbit for both SDRAM and EDO/FPM devices. In this mode, the RAS#/CS5# signal becomes RAS#/CS5#/MA13, RAS4#/CS4# becomes RAS4#/CS4#/BA1, and KRQAK/CS4_64# becomes CS4_64#. CS4_64# (fifth row) function is provided if this signal is set to 1 and DRAM Cache is not present in the system (indicated by a 0 in bit 5, register 53h).
0	**Reserved.**

Table 4 lists the CAS# Latency, RAS# to CAS#, RAS# Precharge, RAS# Active to Precharge and Refresh to RAS# active programmable timings.

Table 4. Programming Timings

Operating Frequency	CAS Latency (CL)	RAS# to CAS# (Trcd)	RAS# Precharge (Trp)	RAS# active to Precharge (Tras)	Refresh to RAS# (Trc)	Register 54h Bits[5:3]
60/66 MHz	3 HCLKs	3 HCLKs	3 HCLKs	5 HCLKs	8 HCLKs	000
60/66 MHz	3 HCLKs	2 HCLKs	3 HCLKs	5 HCLKs	8 HCLKs	100
60/66 MHz	2 HCLKs	2 HCLKs	3 HCLKs	4 HCLKs	7 HCLKs	011

3.1.18. DRAMEC—DRAM EXTENDED CONTROL REGISTER

Address Offset: 56h
Default Value: 52h
Access: Read/Write

This 8-bit register contains additional controls for main memory DRAM operating modes and features.

Bit	Description
7	**Reserved.**
6	**Refresh RAS# Assertion(RRA).** 1=5 clocks (RAS# asserted for Refresh cycles). 0=4 clocks.
5	**Fast EDO Lead Off (FELO).** 1=Enables fast timing EDO read cycles. 0=Disable. This is valid for EDO DRAMs only (in both a synchronous cache and a Cacheless system). This result is a 1 HCLK pull-in for all read leadoff latencies for EDO DRAMs. (i.e., Page hits, Page misses, and Row Misses). This bit must be 0 if any of the DRAM rows is populated with FPM DRAMs.
4	**Speculative Lead Off (SLD).** If set to 0, the DRAM Controller read request is presented before the final memory target (Cache/DRAM/PCI) has been decoded by the MTXC. This results in a 1 HCLK pull-in for all read leadoff latencies. Note that if the cycle does not actually target DRAM, the DRAM cycle is later terminated. The SLD bit applies to EDO/FPM and SDRAM. This bit should be set to 1 in systems with a L2 cache and to 0 for systems without a L2 cache
3	**Reserved.**
2:1	**Memory Address Drive Strength (MAD).** This field controls the strength of the output buffers driving the MA, SRASx#, SCASx#, MWEx# and CKEx pins. It is recommended that series termination or undershoot and overshoot diodes be used on these lines. **Bit[2:1] MA[13,11:0], BA1 SRAS[A,B],SCAS[A,B], MWEx#, CKEx** 00 10 mA 10 mA 01 10 mA 16 mA 10 16 mA 10 mA 11 16 mA 16 mA Setting Memory Address Drive Strength: **1 Row 2 Row 3 Row 4 Row 5 Row 6 Row** 00 00 11 11 11 01* * Assuming All Rows are buffered
0	**Reserved.**

3.1.19. DRAMC—DRAM CONTROL REGISTER

Address Offset: 57h
Default Value: 01h
Access: Read/Write

This 8-bit register controls main memory DRAM operating modes and features.

Bit	Description
7:6	**Hole Enable (HEN).** This field enables a memory hole in DRAM space. CPU cycles matching an enabled hole are passed on to PCI. PCI cycles matching an enabled hole will be ignored by the MTXC (no DEVSEL#). Note that a selected hole is not remapped. **Bits[7:6] Hole Enabled** 00 None 01 512 KB–640 KB (128 Kbytes) 10 15 MB–16 MB (1 Mbyte) 11 14 MB–16 MB (2 Mbytes)
5	**Reserved.**
4	**Enhanced Paging Disable (EPD).** 1=MTXC keeps page open until a page/row miss. When EPD=0, the MTXC uses additional information to keep the DRAM page open when the host may be "right back". See DRAM section for additional information. This bit should be set to 0 for normal operation.
3	**EDO Detect Mode Enable (EDME).** 1=Enables a special timing mode for BIOS to detect EDO DRAM type on a bank-by-bank basis. Once all DRAM row banks have been tested for EDO, the EDME bit should be set to 0. Otherwise, performance will be seriously impacted.
2:0	**DRAM Refresh Rate (DRR).** The DRAM refresh rate for "FPM/EDO only" DRAM subsystem is adjusted according to the value selected by this field. DRAM refresh is implemented using SUSCLK. **Bits[2:0] DRAM Refresh Rate** 000 Refresh Disabled (results in the eventual loss of DRAM data) 001 15.6 µs 010 31.2 µs (for EDO/FPM only memory subsystem) 011 64.4 µs (for EDO/FPM only memory subsystem) 100 125 µs (for EDO/FPM only memory subsystem) 101 256 µs (for EDO/FPM only memory subsystem) 110 Reserved 111 Reserved **NOTES** 1. If any of the row is populated with SDRAMs, this field must be set to 15.6 µs refresh rate. 2. Selecting refresh rate of 125 µs or 256 µs may violate the max RAS# active time DRAM specification. It is up to the system designer to make sure this does not happen.

3.1.20. DRAMT—DRAM TIMING REGISTER

Address Offset: 58h
Default Value: 00h
Access: Read/Write

This 8-bit register controls main memory DRAM timings. For SDRAM specific timing control, see the SDRAMC timing register definition.

Bit	Description
7	**Reserved.**
6:5	**DRAM Read Burst Timing (DRBT).** The DRAM read burst timings are controlled by the DRBT field. Slower rates may be required in certain system designs to support loose layouts or slower memories. Most system designs will be able to use one of the faster burst mode timings. The timing used depends on the type of DRAM on a per-bank basis, as indicated by the DRT register. The x322 timings for EDO Burst rate should be used only when the Fast EDO Path Select (FEPS) bit is set to 1 and the timings for the EDO Burst rate for X222 have a negative margin. This forces the MXS to be negated after the leadoff; thus, selecting the fast path for the leadoff and the slow path for the burst cycles. When FEPS=1 and the EDO Burst rate is set to x222, the EDO read cycle is selected through the fast path for both leadoff and the burst cycles. When FEPS=0 and the EDO Burst rate is set to x222, the EDO read cycle is selected through the slow path for both leadoff and the burst cycles. **DRBT** / **EDO Burst Rate** / **FPM Burst Rate** 00 / x444 / x444 01 / x333 / x444 10 / x222 / x333 11 / Reserved / Reserved
4:3	**DRAM Write Burst Timing (DWBT).** The DRAM write burst timings are controlled by the DWBT field. Slower rates may be required in certain system designs to support loose layouts or slower memories. Most system designs will be able to use one of the faster burst mode timings. **DWBT** / **EDO/FPM Burst Rate** / **DWBT** / **EDO/FPM Burst Rate** 00 / x444 / 10 / x222 01 / x333 / 11 / Reserved
2	**Reserved.**

Bit	Description
1:0	**DRAM Leadoff Timing (DLT).** The DRAM leadoff timings are controlled by the DLT bits. Slower leadoffs may be required in certain system designs to support loose layouts or slower memories. The Row Miss leadoff timings are summarized below for EDO/FPM reads and writes. Changing DLT affects the Row Miss and Page Miss timings only (e.g., DLT=01 is one clock faster than DLT=00 on Row Miss and Page Miss timings). These bit control MA setup to CAS# assertion. DLT does not affect page hit timings. Thus, DLT=00 or DLT=01 has same page hit timings for reads and writes (e.g., for reads, it would be 10-3=7 clocks for DLT=00 or DLT=01)

DLT	Read Leadoff	Write Leadoff	RAS# Precharge	RAS-to-CAS Delay
00	11	7	3	4
01	10	6	3	3
10	11	7	4	4
11	10	6	4	3

SLD and FELO bits have cumulative effect on the leadoff timings. The above leadoff represent timings with SLD=1 and FELO=0.

3.1.21. PAM—PROGRAMMABLE ATTRIBUTE MAP REGISTERS (PAM[6:0])

Address Offset: 59h (PAM0) (5Fh (PAM6)
Default Value: 00h
Attribute: Read/Write
Size: 8 bits (each register)

The MTXC allows programmable memory and cacheability attributes on 14 memory segments of various sizes in the 640-Kbytes to 1-Mbyte address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Three bits are used to specify L1 cacheability and memory attributes for each memory segment. These attributes are:

RE **Read Enable**. When RE=1, the CPU read accesses to the corresponding memory segment are directed to main memory. Conversely, when RE=0, the CPU read accesses are directed to PCI.

WE **Write Enable**. When WE=1, the CPU write accesses to the corresponding memory segment are directed to main memory. Conversely, when WE=0, the CPU write accesses are directed to PCI.

CE **Cache Enable**. When CE=1, the corresponding memory segment is L1 cacheable. CE must not be set to 1 when RE is reset to 0 for any particular memory segment. When CE=1 and WE=0, the corresponding memory segment is cached in the first level cache only on CPU code read cycles.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only. The characteristics for memory segments with these read/write attributes are described in Table 5.

Table 5. Attribute Definition

Read/Write Attribute	Definition
Read Only	Read cycles: CPU cycles are serviced by the DRAM in a normal manner. Write cycles: CPU initiated write cycles are ignored by the DRAM interface as well as the cache. Instead, the cycles are passed to PCI for termination. Areas marked as Read Only are L1 cacheable for Code accesses only. These regions are not cached in the second level cache.
Write Only	Read cycles: All read cycles are ignored by the DRAM interface as well as the second level cache. CPU-initiated read cycles are passed onto PCI for termination. The write only state can be used while copying the contents of a ROM, accessible on PCI, to main memory for shadowing, as in the case of BIOS shadowing. Write cycles: CPU write cycles are serviced by the DRAM and L2 cache in a normal manner.
Read/Write	This is the normal operating mode of main memory. Both read and write cycles from the CPU and PCI are serviced by the DRAM and L2 cache interface.
Disabled	All read and write cycles to this area are ignored by the DRAM and cache interface. These cycles are forwarded to PCI for termination.

Each PAM Register controls two regions, typically 16 Kbytes in size. Each of these regions has a 4-bit field. The four bits that control each region have the same encoding and are defined in Table 6.

PCI master access to DRAM space is also controlled by the PAM Registers. If the PAM programming indicates a region is writeable, then PCI master writes will be accepted (DEVSEL# generated). If the PAM programming indicates a region is readable, PCI master reads will be accepted. If a PCI write to a non-writeable DRAM region, or a PCI read to a non-readable DRAM region is seen, the MTXC will not accept the cycle (DEVSEL# will not be asserted). PCI master accesses to enable memory hole regions will not be accepted.

Table 6. Attribute Bit Assignment

Bits [7, 3] Reserved	Bits [6, 2] Cache Enable	Bits [5, 1] Write Enable	Bits [4, 0] Read Enable	Description
x	x	0	0	DRAM disabled, accesses directed to PCI
x	0	0	1	read only, DRAM write protected, non-cacheable
x	1	0	1	read only, DRAM write protected, L1 cacheable for code accesses only
x	0	1	0	write only
x	0	1	1	read/write, non-cacheable
x	1	1	1	read/write, cacheable

As an example, consider a BIOS that is implemented on the expansion bus. During the initialization process the BIOS can be shadowed in main memory to increase the system performance. When a BIOS is shadowed in main memory, it should be copied to the same address location. To shadow the BIOS, the attributes for that address range should be set to write only. The BIOS is shadowed by first doing a read of that address. This read is forwarded to the expansion bus. The CPU then does a write of the same address, which is directed to main

memory. After the BIOS is shadowed, the attributes for that memory area are set to read only so that all writes are forwarded to the expansion bus.

Table 7. PAM Register and Associated Memory Segments

PAM Reg.	Attribute Bits				Memory Segment	Comments	Offset
PAM0[3:0]	Reserved						59h
PAM0[7:4]	R	CE	WE	RE	0F0000h – 0FFFFFh	BIOS Area	59h
PAM1[3:0]	R	CE	WE	RE	0C0000h – 0C3FFFh	ISA Add-on BIOS	5Ah
PAM1[7:4]	R	CE	WE	RE	0C4000h – 0C7FFFh	ISA Add-on BIOS	5Ah
PAM2[3:0]	R	CE	WE	RE	0C8000h – 0CBFFFh	ISA Add-on BIOS	5Bh
PAM2[7:4]	R	CE	WE	RE	0CC000h – 0CFFFFh	ISA Add-on BIOS	5Bh
PAM3[3:0]	R	CE	WE	RE	0D0000h – 0D3FFFh	ISA Add-on BIOS	5Ch
PAM3[7:4]	R	CE	WE	RE	0D4000h – 0D7FFFh	ISA Add-on BIOS	5Ch
PAM4[3:0]	R	CE	WE	RE	0D8000h – 0DBFFFh	ISA Add-on BIOS	5Dh
PAM4[7:4]	R	CE	WE	RE	0DC000h – 0DFFFFh	ISA Add-on BIOS	5Dh
PAM5[3:0]	R	CE	WE	RE	0E0000h – 0E3FFFh	BIOS Extension	5Eh
PAM5[7:4]	R	CE	WE	RE	0E4000h – 0E7FFFh	BIOS Extension	5Eh
PAM6[3:0]	R	CE	WE	RE	0E8000h – 0EBFFFh	BIOS Extension	5Fh
PAM6[7:4]	R	CE	WE	RE	0EC000h – 0EFFFFh	BIOS Extension	5Fh

NOTES:
The CE bit should not be changed while the L2 cache is enabled.

DOS Application Area (00000h–9FFFh)

Read, write, and cacheability attributes are always enabled and are not programmable for the 0–640-Kbytes DOS application region.

Video Buffer Area (A0000h–BFFFFh)

This 128-Kbytes area is not controlled by attribute bits. CPU-initiated cycles in this region are always forwarded to PCI for termination. This area is not cacheable.

Expansion Area (C0000h–DFFFFh)

This 128-Kbytes area is divided into eight 16-Kbytes segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled Memory that is disabled is not remapped. Cacheability status can also be specified for each segment.

Extended System BIOS Area (E0000h–EFFFFh)

This 64-Kbytes area is divided into four 16-Kbytes segments. Each segment can be assigned independent cacheability, read, and write attributes. Memory segments that are disabled are not remapped elsewhere.

System BIOS Area (F0000h–FFFFFh)

This area is a single 64-Kbytes segment. This segment can be assigned cacheability, read, and write attributes. When disabled, this segment is not remapped.

Extended Memory Area (100000h–FFFFFFFFh)

The extended memory area can be split into several parts:

- Flash BIOS area from 4 Gbytes to 4 Gbytes–512 Kbytes (aliased on ISA at 16 Mbytes–15.5 Mbytes)
- DRAM Memory from 1 Mbytes to a maximum of 512 Mbytes
- PCI Memory space from the top of DRAM to 4 Gbytes–512 Kbytes

On power-up or reset the CPU vectors to the Flash BIOS area, mapped in the range of 4 Gbytes to 4 Gbytes–512 Kbytes. This area is physically mapped on the expansion bus. Since these addresses are in the upper 4-Gbytes range, the request is directed to PCI.

The DRAM memory space can occupy extended memory from a minimum of 1 Mbytes up to 256 Mbytes. This memory is cacheable.

PCI memory space from the top of main memory to 4 Gbytes is always non-cacheable.

3.1.22. DRB—DRAM ROW BOUNDARY REGISTERS

Address Offset: 60–65h
Default Value: 02h
Access: Read/Write

The MTXC supports 6 rows of DRAM. Each row is 64-bits wide. The DRAM Row Boundary Registers define upper and lower addresses for each DRAM row. Contents of these 8-bit registers represent the boundary addresses in 4-Mbytes granularity.

DRB0=Total amount of memory in row 0 (in 4 Mbytes)
DRB1=Total amount of memory in row 0 + row 1 (in 4 Mbytes)
DRB2=Total amount of memory in row 0 + row 1 + row 2 (in 4 Mbytes)
DRB3=Total amount of memory in row 0 + row 1 + row 2 + row 3 (in 4 Mbytes)
DRB4=Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 (in 4 Mbytes)
DRB5=Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 + row 5 (in 4 Mbytes)

The DRAM array can be configured with 512-KB, 1-MB, 4-MB, or 16-MB deep by 32- or 36-bit wide SIMMs. Each register defines an address range that will cause a particular RAS# line to be asserted (e.g., if the first DRAM row is 8 Mbytes, accesses within the 0 to 8-Mbytes range will cause RAS0# to be asserted).

NOTE

When programming the DRB registers, the following programming consideration must be followed: When DRB3 is written, DRB4 and DRB5 are also modified with the value written into DRB3. When DRB4 is written, DRB5 is also modified with the value written into DRB4. To avoid data corruption in the DRB4 and DRB5 registers, program DRB3 first, followed by DRB4 and then DRB5. If either DRB3 or DRB4 are written, this sequence should be followed.

Bit	Description
7	**Reserved.**
6:0	**Row Boundary Address.** This 7-bit value is compared against the address lines A[28:22] to determine the upper address limit of a particular row (i.e., DRB minus previous DRB=row size).

Row Boundary Address

These 8 bit values represent the upper address limits of the 6 rows (i.e., this row minus previous row=row size). Unpopulated rows have a value equal to the previous row (row size=0). DRB5 reflects the maximum amount of DRAM in the system. The top of memory is determined by the value written into DRB5. If DRB5 is greater than 256 Mbytes, then 256 Mbytes of DRAM are available. BIOS must make sure that the DRB registers do not reflect more than 256M of Main memory.

As an example of a general purpose configuration where 3 physical rows are configured for either single-sided or double-sided SIMMs, the memory array would be configured like the one shown in Figure 3. In this configuration, the MTXC drives two RAS# signals directly to the SIMM rows. If single-sided SIMMs are populated, the even RAS# signal is used and the odd RAS# is not connected. If double-sided SIMMs are used, both RAS# signals are used.

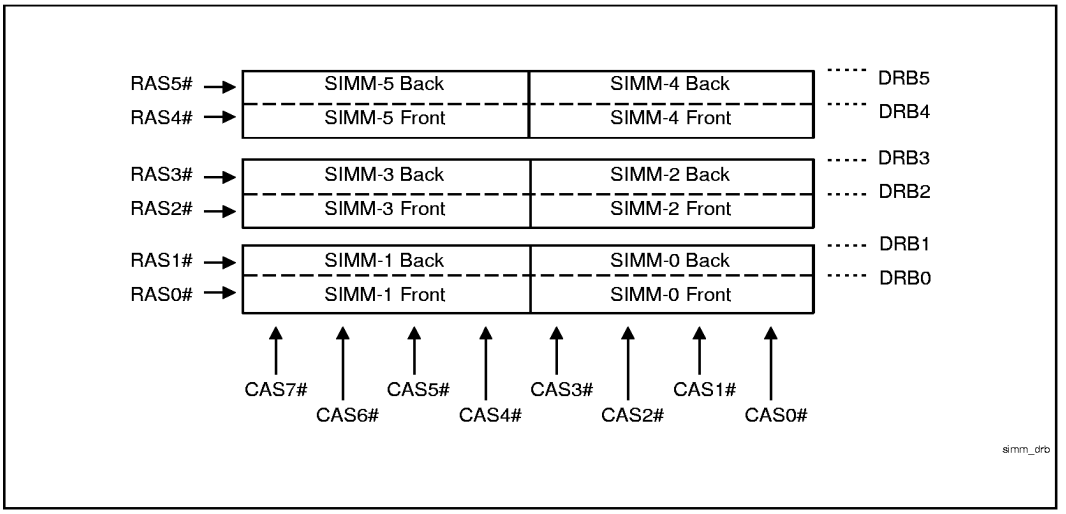


Figure 3. SIMMs and Corresponding DRB Registers

The following 2 examples describe how the DRB Registers are programmed for cases of single-sided and double-sided SIMMs on a motherboard having a total of four 8-byte or eight 4-byte SIMM sockets.

Example #1

The memory array is populated with four single-sided 1 MB x 32 SIMMs, a total of 16 MBytes of DRAM. Two SIMMs are required for each populated row making each populated row 8 Mbytes in size.

DRB0=02h	populated (2 SIMMs, 8 Mbytes this row)
DRB1=04h	populated (2 SIMMs, 8 Mbytes this row)
DRB2=04h	empty row
DRB3=04h	empty row
DRB4=04h	empty row
DRB5=04h	empty row

Example #2

As an another example, the memory array is populated with two 2 Mbytes x 32 double-sided SIMMs (one row), and four 4 Mbytes x 32 single-sided SIMMs (two rows), yielding a total of 96 Mbytes of DRAM. The DRB Registers are programmed as follows:

DRB0=04h	populated with 16 Mbytes, 1/2 of double-sided SIMMs
DRB1=08h	the other 16 Mbytes of the double-sided SIMMs
DRB2=10h	populated with 32 Mbytes, one of the sided SIMMs
DRB3=18h	the other 32 Mbytes of single-sided SIMMs
DRB4=18h	empty row
DRB5=18h	empty row

3.1.23. DRTH—DRAM ROW TYPE REGISTER HIGH

Address Offset: 67h
Default Value: S0000000
Access: Read/Write

This 8-bit register identifies the type of DRAM (EDO, SPM (standard page mode)), or SDRAM (synchronous DRAM) used in rows 4 and 5 and should be programmed by BIOS for optimum performance if EDO DRAMs or SDRAMs are used. The MTXC uses these bits to determine the correct cycle timing to use before a DRAM cycle is run. Bit 7 of this register is used for Host Frequency Detection (HFD). Bit 2 of this register is used to determine the muxing results of CKE/MAA0 and CKEB/MAA1.

NOTE

This register should not be written while DRAM refresh is enabled.

Bit	Description
7	**Host Frequency Detection (HFD).** 1=66 MHz. 0=60 MHz. This bit is initialized to the inverted level on the A27 signal at the rising edge of the RST#. Since A27 pin contains an internal weak pulldown, unless an external resistor exits, the field is initialized to 1, indicating 66 MHz. Subsequent writes to this field will override the reset strap value. BIOS can use the value to determine if the system is 60 MHz (external pull-up) or 66 MHz (no strapping).
5:4, 1:0	**DRAM Row Type (DRT).** The DRT bits select the DRAM type installed in each physical DRAM Row. Each one-of-four bit pairs in this register corresponds to the DRAM row identified by the corresponding DRB register. **DRT Bits — DRAM Row** 5,1 — 5 4,0 — 4 **DRT — DRAM Type value definitions** 0,0 — SPM DRAM 0,1 — EDO DRAM 1,0 — SDRAM 1,1 — Reserved
6,3	**Reserved.**
2	**Memory Address Select Enable (MASELEN).** When this bit is set to 1, CKE and CKEB are used to propagate the second copy of the MA0 and MA1 lines. CKE is muxed with MAA0 and CKEB is muxed with MAA1. When this bit is set to 0, the CKE and CKEB functionality is propagated across these lines. This bit defaults to 0 and BIOS must set it to 1 to take advantage of the second copy of the MA0 and MA1 lines.

3.1.24. DRTL—DRAM ROW TYPE REGISTER LOW

Address Offset: 68h
Default Value: 00h
Access: Read/Write

This 8-bit register identifies the type of DRAM (EDO, SPM (standard page mode)), or SDRAM (synchronous DRAM) used in rows 0 to 3 and should be programmed by BIOS for optimum performance if EDO DRAM's or SDRAMs are used. The hardware uses these bits to determine the correct cycle timing to use before a DRAM cycle is run.

Bit	Description
7:0	**DRAM Row Type (DRT).** The DRT bits select the DRAM type installed in each physical DRAM Row. Each one-of-four bit pairs in this register corresponds to the DRAM row identified by the corresponding DRB register. **DRT Bits — DRAM Row** 7,3 — 3 6,2 — 2 5,1 — 1 4,0 — 0 **DRT — DRAM Type value definitions** 0,0 — SPM DRAM 0,1 — EDO DRAM 1,0 — SDRAM 1,1 — reserved

3.1.25. MTT—MULTI-TRANSACTION TIMER REGISTER (RESERVED TEST MODE REGISTER)

Address Offset: 70h
Default Value: 20h
Access: Read/Write

MTT is an 8-bit register that controls the amount of time that the MTXC's arbiter allows a PCI initiator to perform multiple transactions on the PCI bus. The MTT guarantees the minimum time, measured in PCLKs, that the PCI agent retains the ownership of the PCI bus from the initial assertion of grant.

Bit	Description
7:2	**MTT Count value.** The number of clocks programmed in the MTT represents the guaranteed time slice (in PCLKs) allotted to the current agent, after which the MTXC will grant the bus as soon as another PCI agent requests the bus. The value of 00h disables this function. The count value should be set to multiples of 4 (i.e., 2 lsbs are ignored).
1:0	**Reserved.** Hardwired to 0. (i.e., counter has a resolution of 4 PCLKs)

3.1.26. ESMRAMC—EXTENDED SYSTEM MANAGEMENT RAM CONTROL REGISTER

Address Offset: 71h
Default Value: 00h
Access: Read/Write

The Extended SMRAM register controls the configuration of Extended SMRAM space. MTXC supports two types of SMRAM memory: Compatible and Extended. The Compatible SMRAM (C_SMRAM) memory provides an uncacheable SMRAM memory space below 1 Mbytes in the A and B segments. The Extended SMRAM (E_SMRAM) memory provides a writeback cacheable SMRAM memory space that is above 1 Mbytes. This register provides the following types of control over SMRAM space:

- Where the memory space is located (above 1 Mbytes, below 1 Mbytes)
- Enabling of SMRAM memory (TSEG, 128 Kbytes, 256 Kbytes, 512 Kbytes or 1 Mbytes of additional SMRAM memory) for Extended SMRAM space only.
- Cacheability control (for the Extended SMRAM space only)
- Protection of SMRAM space for non-SMM accesses

Bit	Description
7	**High SMRAM Enable (H_SMRAME).** 1=Enable. 0=Disable. This bit enables the high SMRAM memory space to appear in the appropriate physical address locations between 100A0000h and 100F0000h.
6	**Extended SMRAM Error (E_SMERR).** This bit is set when CPU accesses the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit=0. It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it.
5	**SMRAM Cache Strategy (SM_CACHE).** Hardwired to 0. This bit determines how Extended SMRAM space is cached (writethru or writeback). Since the MTXC supports only writeback for extended SMRAM space, this bit is hardwired to 0.
4	**SMRAM_L1_EN (SM_L1).** This bit should be set to 1 if Extended SMRAM is being used and the system wishes to L1 writeback cache this memory space. Default value for this bit is 0.
3	**SMRAM_L2_EN (SM_L2).** This bit should be set to 1 if Extended SMRAM is being used, and there is less than 32 Mbytes of DRAM in the system. Setting of this bit when SM_L1 bit=1 allows the Extended SMRAM to be writeback cached in the L2. Default value for this bit is 0.
2:1	**TSEG_SZ[1-0] (T_SZ).** Selects the size of the TSEG memory block, if enabled. This memory is taken from the top of DRAM space, which is no longer claimed by the memory controller (all accesses to this space are sent to the PCI bus if TSEG_EN is set). This memory appears at the physical memory space of 256 Mbytes plus the top of memory (TOM) minus the size of TSEG. This field decodes as follows: **Bits[1,0] Description** 00 (TOM-128 KB) to TOM 01 (TOM-256 KB) to TOM 10 (TOM-512 KB) to TOM 11 (TOM-1 MB) to TOM
0	**TSEG_EN (T_EN).** When G_SMRAME=1 and T_EN=1, the TSEG is enabled to appear in the appropriate physical address space.

3.1.27. SMRAMC—SYSTEM MANAGEMENT RAM CONTROL REGISTER

Address Offset: 72h
Default Value: 02h
Access: Read/Write

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. MTXC supports two types of SMRAM memory: Compatible and Extended. The Open, Close, and Lock bits function only when G_SMRAME bit is set to a 1. Also, the OPEN bit be reset before the LOCK bit is set.

Bit	Description
7	**Reserved.**
6	**SMM Space Open (D_OPEN).** When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMIACT# is negated. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 is mutually exclusive with D_CLS=1. When D_LCK is set to a 1, D_OPEN is reset to 0 and becomes read only.
5	**SMM Space Closed (D_CLS).** When D_CLS=1, SMM space DRAM is not accessible to data references, even if SMIACT# is asserted. Code references may still access SMM space DRAM. This will allow SMM software to reference "through" SMM space to update the display, even when SMM space is mapped over the VGA range. Software should ensure that D_OPEN=1 is mutually exclusive with D_CLS=1.
4	**SMM Space Locked (D_LCK).** When D_LCK is set to 1, D_OPEN is reset to 0 and both D_LCK and D_OPEN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a power-on reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to "lock down" SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	**Global SMRAM Enable (G_SMRAME)**. If set to a 1, then Compatible SMRAM functions is enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADS# with SMIACT#). To enable Extended SMRAM function this bit has be set to 1. Refer to the section on SMM for more details.
2:0	**Compatible SMM Space Base Segment (C_BASE_SEG).** This field programs the location of SMM space. SMM DRAM is not remapped. It is simply "made visible" if the conditions are right to access SMM space; otherwise, the access is forwarded to PCI. C_BASE_SEG=010 selects the SMM space as A0000–BFFFFh. All other values are reserved. PCI initiators are not allowed to access to SMM space. These bits are hardwired to 010.

Table 8 summarizes the operation of SMRAM space cycles targeting the SMI space addresses.

Table 8. SMRAM Space Cycles

G_SMRAME	D_LCK	D_CLS	D_OPEN	SMIACT#	H_SMRAME	TSEG_EN	Code Fetch			Data Access		
0	x	x	x	x	x	x	A→PCI	S→PCI	T→PCI	A→PCI	S→PCI	T→PCI
1	0	0	0	0	0	0	A→DRAM	S→PCI	T→PCI	A→DRAM	S→PCI	T→PCI
1	0	0	0	0	0	1	A→DRAM	S→PCI	T→DRAM	A→DRAM	S→PCI	T→DRAM
1	0	0	0	0	1	0	A→PCI	S→DRAM	T→PCI	A→PCI	S→DRAM	T→PCI
1	0	0	0	0	1	1	A→PCI	S→DRAM	T→DRAM	A→PCI	S→DRAM	T→DRAM
1	0	x	0	1	x	x	A→PCI	S→PCI	T→PCI	A→PCI	S→PCI	T→PCI
1	0	0	1	x	0	0	A→DRAM	S→PCI	T→PCI	A→DRAM	S→PCI	T→PCI
1	0	0	1	x	0	1	A→DRAM	S→PCI	T→DRAM	A→DRAM	S→PCI	T→DRAM
1	0	0	1	x	1	0	A→PCI	S→DRAM	T→PCI	A→PCI	S→DRAM	T→PCI
1	0	0	1	x	1	1	A→PCI	S→DRAM	T→DRAM	A→PCI	S→DRAM	T→DRAM
1	0	1	0	0	0	0	A→DRAM	S→PCI	T→PCI	A→PCI	S→PCI	T→PCI
1	0	1	0	0	0	1	A→DRAM	S→PCI	T→DRAM	A→PCI	S→PCI	T→PCI
1	0	1	0	0	1	0	A→DRAM	S→DRAM	T→PCI	A→PCI	S→PCI	T→PCI
1	0	1	0	0	1	1	A→PCI	S→DRAM	T→DRAM	A→PCI	S→PCI	T→PCI
1	0	1	1	x	x	x	Invalid			Invalid		
1	1	0	0	0	0	0	A→DRAM	S→PCI	T→PCI	A→DRAM	S→PCI	T→PCI
1	1	0	0	0	0	1	A→DRAM	S→PCI	T→DRAM	A→DRAM	S→PCI	T→DRAM
1	1	0	0	0	1	0	A→PCI	S→DRAM	T→PCI	A→PCI	S→DRAM	T→PCI
1	1	0	0	0	1	1	A→PCI	S→DRAM	T→DRAM	A→PCI	S→DRAM	T→DRAM
1	1	x	0	1	x	x	A→PCI	S→PCI	T→PCI	A→PCI	S→PCI	T→PCI
1	1	1	0	0	0	0	A→DRAM	S→PCI	T→PCI	A→PCI	S→PCI	T→PCI
1	1	1	0	0	0	1	A→DRAM	S→PCI	T→DRAM	A→PCI	S→PCI	T→PCI
1	1	1	0	0	1	0	A→PCI	S→DRAM	T→PCI	A→PCI	S→PCI	T→PCI
1	1	1	0	0	1	1	A→PCI	S→DRAM	T→DRAM	A→PCI	S→PCI	T→PCI

NOTES:

1. A=A Segment, S=100A0000h to 100FFFFFh, and T=T Segment. The Code Fetch and Data Access columns indicate whether the access is to the PCI bus or to main memory DRAM.

3.1.28. MCTL—MISCELLANEOUS CONTROL REGISTER

Address Offset: 79h
Default Value: 00h
Access: Read/Write

Bit	Description
7	**Reserved.**
6	**ACPI Control Register Enable (ACRE).** 0=Any CPU access to I/O address 0022h is passed on to the PCI bus. 1=Any CPU access to I/O address 0022h is processed internally in the MTXC. This bit must be set to 1 before accessing the "Arbiter Disable" bit in the PM2_CNTRL Register (0022h).
5	**Suspend Refresh Type (SRT).** 0=CBR refresh. 1=Self refresh. This bit determines what type of DRAM refresh is used during Power On Suspend (POS) or Suspend to DRAM modes. This bit applies to EDO/FPM DRAM only. SDRAM always uses self refresh, regardless of the state of this bit.
4	**Normal Refresh Enable (NREF_EN).** Setting this bit to 1 switches MTXC from suspend refresh to normal refresh. After the reset, this bit must be set by software executing out of EPROM. MTXC waits for this bit to be set before exiting out of suspend refresh mode.
3	**Reserved.**
2	**Internal Clock Control (Gated Clock) Disable (ICC).** 1=Disable. 0=Enable. This bit, when set to 0, allows the MTXC to reduce its power consumption (via turning off its internal clocks, to specific interfaces) when in chip standby mode. This bit defaults to 0.
1:0	**Reserved.**

4.0. FUNCTIONAL DESCRIPTION

4.1. Host Interface

The Host Interface of the MTXC is designed to support the Pentium microprocessor. The host interface of the MTXC supports 60-, and 66-MHz bus speeds. The Intel 430TX PCIset supports the Pentium microprocessor with a full 64-bit data bus, 32-bit address bus, and associated internal writeback cache logic. Host bus addresses are decoded by the MTXC for accesses to main memory, PCI memory, and PCI I/O. The MTXC also supports the pipelined addressing capability of the Pentium microprocessor.

4.2. Secondary Cache Interface

The MTXC integrates a high performance writeback second level cache controller using internal/external tags and provides a full first level and second level cache coherency mechanism. The second level cache is direct mapped, nonsectored, and supports a writeback, no write allocate (lines are not allocated on write misses) write policy.

The second level cache can be configured to support either a 256-KB or 512-KB cache using synchronous pipelined burst SRAM or DRAM Cache. One additional PCIset signal (KRQAK) is required to support DRAM Cache. 64-Mbytes cacheability coverage is obtained with 8Kx8 standard SRAM to store the tags for 256-KB configuration. For the 512-KB configurations, a 16Kx8 standard SRAM is used to store the tags and the valid bits for 64-MB cacheability.

A second level cache line is 32-bytes wide. In the 256-KB configurations, the second level cache contains 8K lines, while the 512-KB configurations contain 16K lines. Valid and modified status bits are kept on a per line basis. Cacheability of the entire memory space in first level cache is supported, while only the lower 64 MB of main memory is cacheable in the second level cache. Table 9 shows the tag sizes needed to support different sizes of cacheability. Only main memory controlled by the MTXC DRAM interface is cached. PCI memory is not cached.

Table 9. Cacheability

Cache Size	Tag Size	Cacheability
256 Kbytes	8K by 8 bits	64 Mbytes
512 Kbytes	16K by 8 bits (including valid bit)	64 Mbytes

The following table shows the different standard SRAM access time requirements for different host clock frequencies.

Table 10. SRAM Access Time Requirements

Host Clock Frequency (MHz)	Pipelined Burst Clock-to-Output Access Time (ns)	Tag RAM Cycle Time (ns)
60	10	15
66	8.5	15

Figure 4 and Figure 5 show the connections between the MTXC and the external tag RAM and data SRAM.

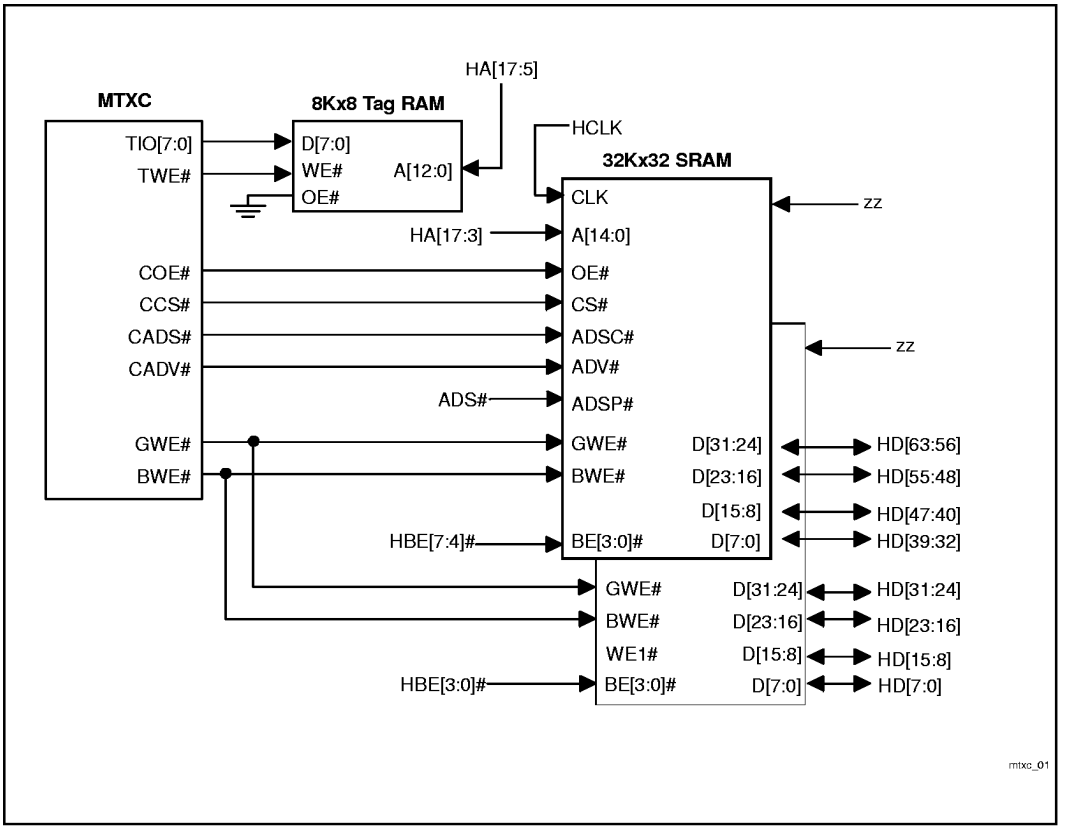


Figure 4. MTXC Connections for 256K Second Level Cache with PBSRAM

Figure 5 shows a 512-KB implementation using four 32Kx32 SRAM. Two 64Kx32 devices could also be used. In this case, HA18 would not be connected to CS2# (i.e., CS2 and CS2# should be connected to an active state). HA18 should be connected to one of the address lines on the 64Kx32 SRAM and is still required for the TAG RAM.

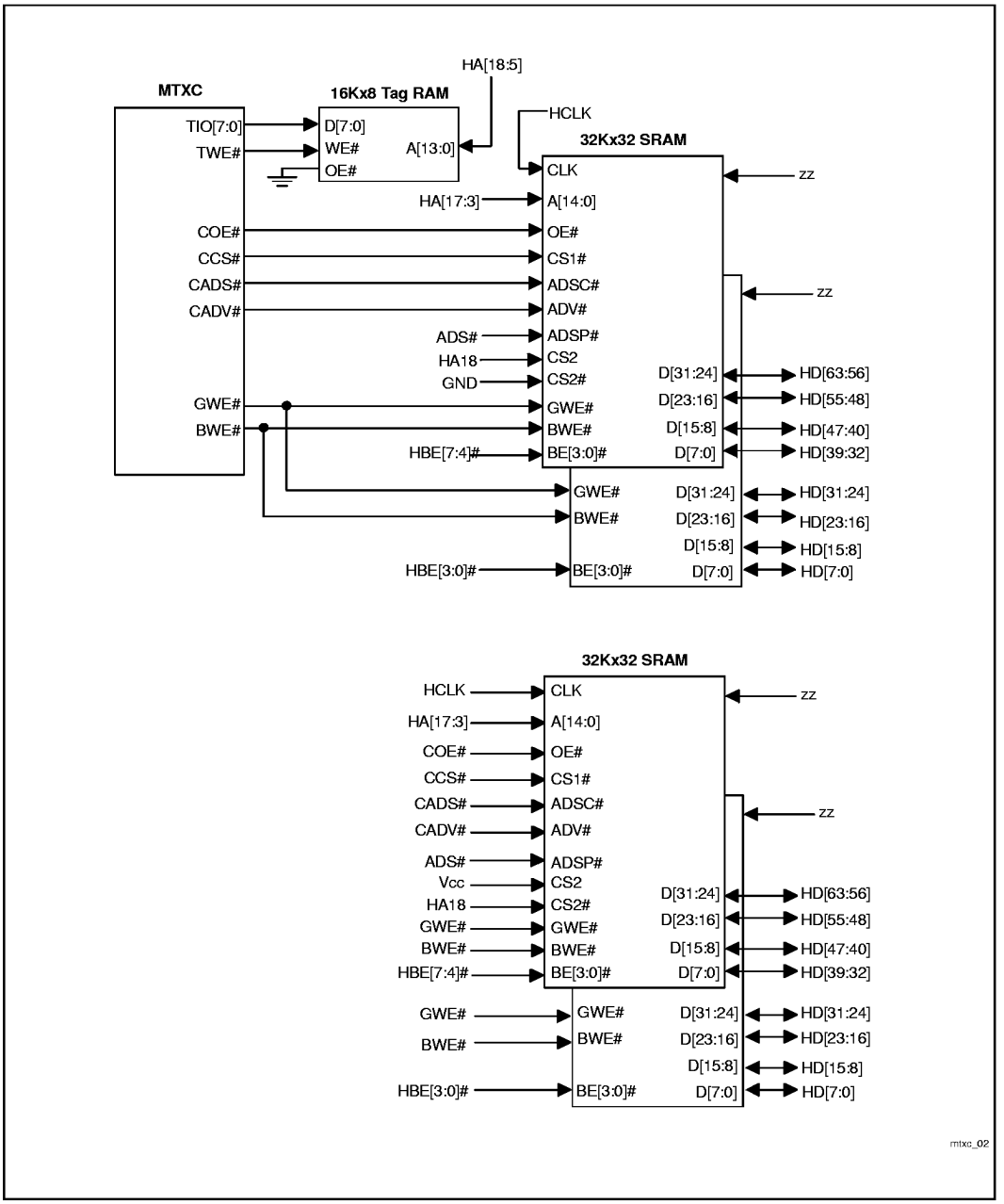


Figure 5. MTXC Connections for 512K Second Level Cache with PBSRAM

4.2.1. CLOCK LATENCIES

Table 11 lists the latencies for various processor transfers to and from the second level cache.

Table 11. Second Level Cache Latencies with Pipelined Burst SRAM

Cycle Type	HCLK Count
Burst Read	3-1-1-1
Burst Write (write back)	3-1-1-1
Single Read	3
Single Write	3
Pipelined Back-to-Back Burst Reads	3-1-1-1,1-1-1-1 (note 1)

NOTES:
1. The back to back cycles do not account for CPU idle clocks between cycles.

4.2.2. SNOOP CYCLES

The snoop (or inquire) cycle is used to probe the first level and second level caches when a PCI master attempts to access main memory. This is done in order to maintain coherency between the first and second level caches and main memory.

To maintain optimum PCI bandwidth to DRAM, the MTXC utilizes a snoop ahead algorithm. Once the snoop for the first cache line of a transfer has completed, the MTXC automatically snoops the next sequential cache line. This algorithm enables the MTXC to continue burst transfers across cache line boundaries.

Reads

Snoop cycles are performed by driving the PCI master address onto the host address bus and asserting EADS#. The processor then performs a tag lookup to determine whether the addressed memory is in the first level cache. If the snoop hit is to a Modified Line in the first level cache (HITM# asserted), then the line in the first level cache is posted to the DRAM Posted Write buffers. The line in the second level cache (if it exists) is invalidated. The line in the first level cache is not invalidated if the INV pin on the CPU is tied to the KEN# signal from the MTXC. KEN#/INV will be driven low by the MTXC with EADS# assertion during PCI master read cycles.

At the same time as the first level snoop cycle, the MTXC performs a tag lookup to determine whether the addressed memory is in the second level cache. A hit to a modified line in the second level cache also results in a writeback to DRAM posted write buffers if HITM# is not asserted. The PCI data is serviced from the DRAM after the line has been retired to DRAM.

Writes

PCI Master write cycles never result in a write directly into the second level cache. A snoop hit to a modified line in either the first or second caches results in a writeback of that line to main memory. If both the first and second level caches have modified lines, then the line is written back from the first level cache. In all cases lines in the first and second level caches are invalidated and the PCI write to main memory occurs after the writeback completes. A PCI master write snoop hit to an unmodified line in either the first or second level caches results in the line being invalidated. KEN#/INV will be driven high by the MTXC with EADS# assertion during PCI master write cycles.

4.2.3. DRAM CACHE SECOND LEVEL CACHE MODE

DRAM Cache L2 cache implementation is similar to Pipelined Burst SRAM, except for the addition of the KRQAK bi-direct refresh handshake signal between the MTXC and L2 SRAM. A DRAM Cache type L2 is assumed present when the KRQAK pin is sampled high during the negation of the reset signal. An internal weak pull-down is used on the MTXC KRQAK pin to default to a non DRAM Cache L2 mode, if this pin is left unconnected. An external pull-up (10 kΩ) must be used on KRQAK when DRAM Cache SRAM is used. Note that there is no configuration bit associated with the L2 Pseudo SRAM mode.

The SRAM can operate in either master or slave mode via the M/S# strapping bit. In master mode, the SRAM drives the KRQAK pin to request a refresh. A slave device never drives KRQAK, but only monitors it to determine when a refresh period begins. Only one SRAM device within the L2 cache is master enabled. The other SRAM devices must be slaves.

During reset, the master SRAM and MTXC tri-state their KRQAK outputs. After the SRAM RESET pin is negated, KRQAK remains tri-stated for one whole refresh interval and is then driven high by the master SRAM. The SRAM signals a refresh request by driving KRQAK low for 1 clock, high the next clock, and then tri-states on the following clock and waits, sampling the KRQAK pin. The MTXC after sampling the SRAM's request on KRQAK and after the SRAM has tri-stated its KRQAK output, waits for a host bus dead clock and grants an L2 refresh by driving its KRQAK pin in an identical fashion to the SRAM's request signaling. When all SRAM's see the refresh grant from the MTXC, they begin their internal refresh cycle for a period of 20 clocks.

4.3. DRAM Interface

The MTXC integrates a DRAM controller that supports a 64-bit memory array from 4 Mbytes to 256 Mbytes of main memory. The MTXC supports Standard Page Mode (FPM), Extended Data Out (EDO) and Synchronous DRAM (SDRAM) memories using 32-bit wide SIMM modules, 64-bit wide unbuffered DIMM modules and 64-bit wide unbuffered SO-DIMM modules. DRAM parity is not supported, and for loading reasons, parity modules should not be used. All three memory types can be mixed and matched. The MTXC generates all DRAM control signals and multiplexed addresses for the DRAM array. The address and data flows through the MTXC for all DRAM accesses. The DRAM controller interface is fully configurable through a set of control registers. Complete descriptions of these registers are given in the MTXC configuration register description. A brief overview of these registers is provided in this section.

The MTXC supports page mode DRAMs and EDO (Extended Data Out) DRAMs; otherwise known as Hyper Page mode. The twelve multiplexed address lines, MA[11:0], allow the MTXC to support 4-Mbit, 16-Mbit, and 64-Mbit memory, both symmetrical and asymmetrical addressing. The MTXC has six RAS# lines enabling the support of up to six rows of DRAM. Eight CAS# lines allow byte control over the array during write operations. The MTXC targets 60 ns (also supports 50 ns and 70 ns) DRAMs, and supports both single- and double-sided Dram modules. The MTXC provides CBR refresh and extended CBR refresh in the normal mode and self refresh or CBR (for EDOs only) during suspend mode.

The MTXC also supports SDRAMs. The fourteen multiplexed address lines, MA[13:0], allow the MTXC to support 16-Mbit and 64-Mbit SDRAM devices. The MTXC has six CS# lines (i.e. muxed onto RAS#[5:0]). Although six CS# signals are provided, due to loading concerns, 5 rows of SDRAM maximum is recommended. Eight DQM lines (i.e., muxed with CAS#[7:0]) allow byte control over the array during the write operation. Two copies of SRAS# and SCAS# signals are provided for encoded SDRAM commands. The MTXC targets 60- and 66-MHz SDRAMs and supports both single- and double-sided SDRAM modules.

The DRAM interface of the MTXC is configured by the DRAM Control Mode Register (DRAMC), DRAM Extended Control Register (DRAMEC), DRAM Timing Register (DRAMT), SDRAM Control Register (SDRAMC), six DRAM Row Boundary (DRB) Registers, and the DRAM Row Type (DRT) Registers. The DRB registers define the size of each row in the memory array.

Seven Programmable Attribute Map (PAM) Registers are used to specify the cacheability, PCI enable, and read/write status of the memory space between 640 Kbytes and 1 Mbytes. Each PAM Register defines a specific address area enabling the system to selectively mark specific memory ranges as cacheable, read only, write only, read/write, or disabled. When a memory range is disabled, all CPU accesses to that range are forwarded to PCI.

The MTXC also supports one of two memory holes, either from 512 KB–640 KB or from 14/15 MB–16 MB in main memory. Accesses to the memory holes are forwarded to PCI. The memory hole can be enabled/disabled through the DRAM Control register. All other memory from 1M to 256 MB is read/write L1 cacheable, and is L2 cacheable up to 64 MB.

An optional Extended SMRAM DRAM memory space is also supported in the 256-MB to 512-MB address range. It consists of the 640-KB–1-MB DRAM area aliased at the 256-MB memory segment, and also an optional 128K/256K/512K/1M DRAM area chopped from the Top-of-DRAM memory and aliased above 256 MB in a similar manner.

4.3.1. DRAM ORGANIZATION

The MTXC integrates a DRAM controller that supports EDO, FPM, and SDRAM. SDRAM, EDO and FPM DRAM's can be mixed between rows, however, a given row must contain only one type of DRAM. When DRAM types are mixed (EDO, FPM and SDRAM) each row will run optimized for that particular type of DRAM.

The MTXC supports six rows of memory (six RAS#/CS# lines). For maximum memory flexibility and performance, it is recommended that a DRAM configuration of four rows be used. This allows 64-Mbit DRAM devices to be used as well as the mixing of SDRAM and EDO/FPM. Figure 6 shows an EDO/FPM configuration using x32 SIMM modules and Figure 7 shows a four row EDO/FPM/SDRAM configuration using x64 DIMM modules (or x64 SO-DIMM).

NOTE

It is not recommended to mix SDRAM (which are 3V devices) with 5V EDO/FPM SIMMs, unless the SDRAM and EDO/FPM are properly isolated (e.g., isolate the memory data lines with Qswitches). Mixing 5V and 3V memory is not recommend for reliability reasons. Not all SDRAMs are 5V tolerant.

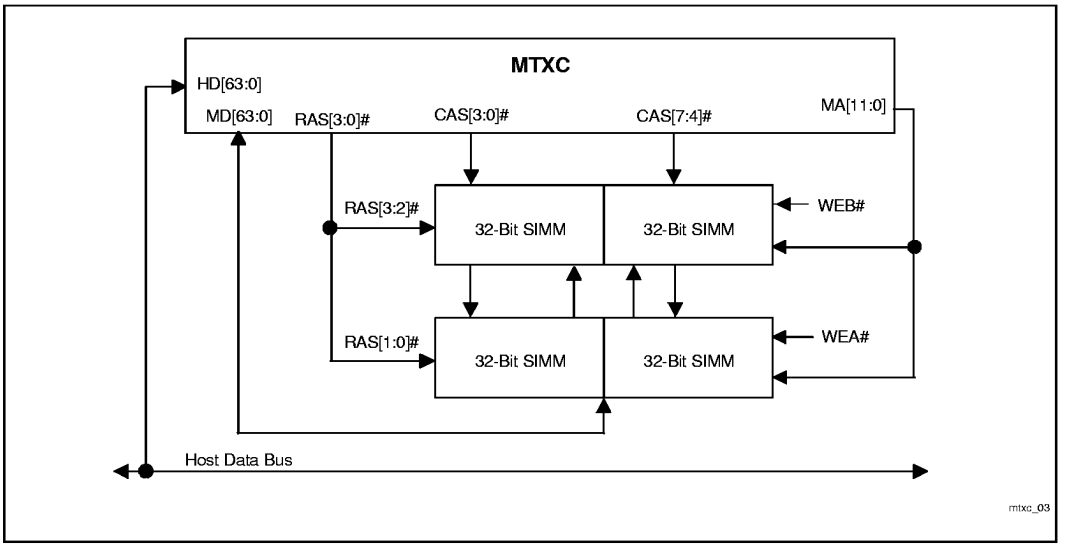
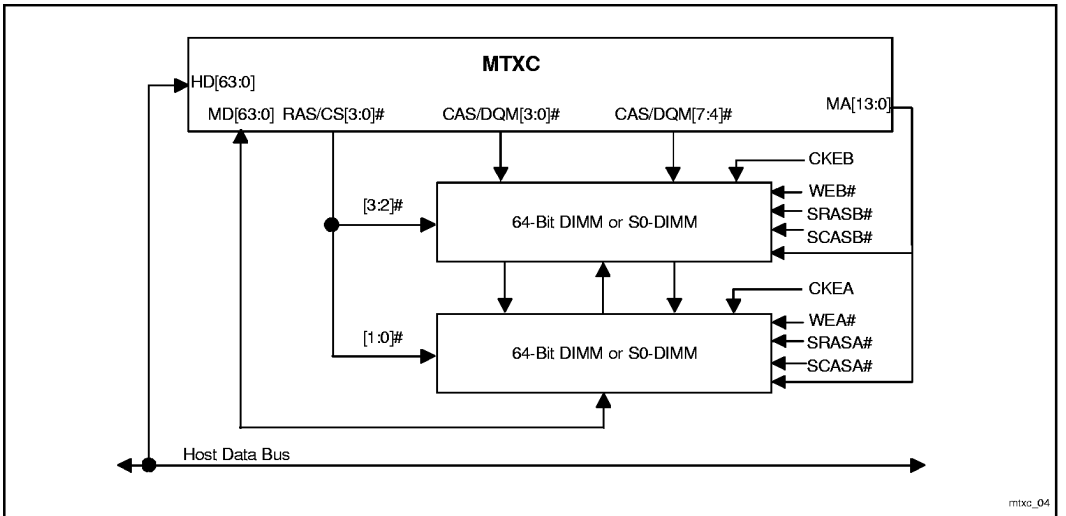


Figure 6. FPM/EDO Four Row SIMM Configuration



NOTES:

1. In a configuration that supports suspend to RAM, only CKE is used. This is because CKEB is not part of the suspend well the MTXC maintains during a suspend to RAM state.
2. In a desktop system that supports EDO/FPM, CKE and CKEB should be used as the second pair of MA0 and MA1 lines. CKE is used as MAA0 and CKEB is used as MAA1. In this case, they should be evenly distributed throughout the system along with the first pair of MA0 and MA1 lines.

Figure 7. FPM/EDO/SDRAM Four Row DIMM or SO-DIMM Configuration

Rules for Populating SIMM Modules (or x32 SO-DIMM modules)

- SIMM sockets can be populated in any order (i.e., memory for RAS0# does not have to be populated before memory for RAS[2:1]# or RAS[4:3]# are used).
- SIMM socket pairs (i.e., two, 32-bit wide SIMMs) need to be populated with the same densities. For example, SIMM sockets for RAS0# should be populated with identical densities. However, SIMM sockets for RAS[2:1]# can be populated with different densities than the SIMM socket pair for RAS0#.
- EDOs and standard page mode can both be used; however, only one type should be used per SIMM socket pair. For example, in the table shown below SIMM sockets for RAS[2:1]# can be populated with EDOs while SIMM sockets for RAS[4:3]# can be populated with standard page mode. If different memory is used for different rows, each row will be optimized for that type of memory.
- The DRAM Timing Register which provides the DRAM speed grade control for the entire memory array must be programmed to use the timings of the slowest DRAMs installed.

Rules for Populating DIMM or SO-DIMM modules

- DIMM or SO-DIMM sockets can be populated in any order (i.e., memory for RAS0# does not have to be populated before memory for RAS[2:1]# or RAS[4:3]# are used).

4.3.2. CONFIGURATION REQUIREMENTS

General Configuration Requirements

- In a system that uses 64-Mbit SDRAM, the RAS4#/CS4#/BA1 and RAS5#/CS5#/MA13 signals are used to provide two additional address lines (BA1 and MA13), and KRQAK/CS4_64# is used to provide the 5th CS# line, if required. To enable 64-Mbit support for four rows of SDRAM, set SDRAMC[bit 1] to 1 (offset 54h). To enable 64-Mbit support for five rows of SDRAM, SDRAMC[bit 1] must be set to 1, and DRAM cache must **not** be present in the system (indicated by CEC[bit 5]=0, offset 53h). In a five row SDRAM system that supports 64-Mbit SDRAM devices, the KRQAK/CS4_64# signal provides the fifth CS# (or CS4_64#) function. This means that a system that supports DRAM Cache, can not support five rows of 64-Mbit SDRAM. However, four rows of 64-Mbit SDRAM with DRAM Cache is supported. In a FPM/EDO only configuration, there are no restrictions on using 64-Mbit devices (i.e., all six rows can support 64-Mbit DRAM devices. However, SDRAMC[bit 1] must be set to 1 if more than four rows of EDO/FPM are used. This allows the RAS4# and RAS5# functions to be used.

	Driven on RAS5#/CS5#/ MA13	Driven on RAS4#/CS4#/ MA13	Driven on KRQAK/ CS4_64#	64-Mbit (SDRAM)	64-Mbit (EDO/FPM)
Bit 1, reg 54h=0	RAS5#/CS5#	RAS4#/CS4#	KRQAK	no	yes (6 rows)
Bit 1, reg 54h=1 and DRAM Cache is present*	MA13	BA1 (Bank Select)	KRQAK	Yes (4 rows)	Yes (4 rows)
Bit 1, reg 54h=1 and DRAM Cache is not present[1]	MA13	BA1 (Bank Select)	RAS4#/ CS4_64#	Yes (5 rows)	Yes (5 rows)

NOTES:

1. The presence of DRAM cache is indicated by the value in bit 5, register 53h.

- Due to loading, using SDRAM x4 devices is not recommended.
- Buffering of SDRAM Rows is not supported
- In a five row system, the 5th row is intended to be implemented with DRAM devices that are soldered down on the motherboard. If a DIMM or a SIMM is used in the 5th row, it should **not** be used as an upgrade path

by the end user; the size and type of DRAM that can be implemented in the 5th row is limited (see the bullets below).

- The total memory supported is 256 MB, even though it is possible to populate the six rows with more than 256 MB. This limit must be ensured by the system BIOS.

EDO/FPM only configuration Requirements

- If more than four rows of x4 DRAM devices + one row of x8 DRAM devices of memory is supported, it is recommended that all six rows be buffered. MA and MWE# enable signals should be buffered. In a system that only supports x8 or x16 devices (i.e., x4 devices not supported), six rows of memory can be supported without buffering.
- Maximum load supported without buffers: Four rows of x4 DRAM devices + one row of x8 DRAM devices.
- A second pair or MA0 and MA1 signals are provided by muxing CKE with MAA0 and CKEB with MAA1. In a desktop system, it is required that the second pair of MA lines be used to support 5-2-2-2 EDO performance in more than two rows of memory. The second pair of MA lines are not required in a mobile system, assuming x4 devices are not used. The MA functionality is selected via DRAMC[bit 2] (67h).

SDRAM only configuration Requirements

- Maximum rows supported; Five rows of x8 devices.

SDRAM/EDO/FPM mixing configuration Requirements

- If SDRAM and EDO/FPM are mixed in a system, the configuration is limited to a maximum of four rows (two rows of x4 EDO/FPM and two rows of x8 or x16 SDRAM). If only x8 or x16 EDO/FPM and SDRAM devices are used (i.e., not x4's), five rows can be supported.
- SDRAMs can be mixed with EDO/FPM on a row by row basis (e.g., row 0 can be populated with SDRAMs while row 3 is populated with EDO/FPM).
- A second pair or MA0 and MA1 signals are provided by muxing CKE with MAA0 and CKEB with MAA1. In a desktop system, it is required that the second pair of MA lines be used to support 5-2-2-2 EDO performance in more than two rows of memory. The second pair of MA lines are not required in a mobile system, assuming x4 devices are not used. The MA functionality is selected via DRAMC[bit 2] (67h).

Table 12 provides a summary of the characteristics of memory configurations supported by the MTXC. Minimum values listed are obtained with single-sided SIMMs or DIMMs. Maximum values are obtained with double-sided SIMMs or DIMMs. Note that, for a 64-bit wide memory array, a minimum of two 32-bit wide DRAM SIMMs are required in any specific row. The minimum values used are also the smallest upgradeable memory size. Please note that EDO/FPM can also come on x64 DIMM modules.

Table 12. Minimum (Upgradeable) and Maximum Memory Size for each configuration (DRAM)

DRAM Tech.	DRAM Density	DRAM Width	DRAM SIMM		DRAM Addressing	Address Size		DRAM Size	
			SS x32	DS x32		Row	Col	Min. (UP) (1 row)	Max. (6 rows)
4M	512K	8	512K	1M	Asymmetric	10	9	4 MB	24 MB
	1M	4	1M	2M	Symmetric	10	10	8 MB	48 MB
16M	1M	16	1M	2M	Symmetric	10	10	8 MB	48 MB
	1M	16	1M	2M	Asymmetric	12	8	8 MB	48 MB
	2M	8	2M	4M	Asymmetric	11	10	16 MB	96 MB
	4M	4	4M	8M	Symmetric	11	11	32 MB	192 MB
	4M	4	4M	8M	Asymmetric	12	10	32 MB	192 MB
64M	2M	32	2M	4M	Asymmetric	12	9	16 MB	96 MB
	4M	16	4M	8M	Symmetric	11	11	32 MB	192 MB
	4M	16	4M	8M	Asymmetric	12	10	32 MB	192 MB
	8M	8	8M	16M	Asymmetric	12	11	64 MB	256 MB
	16M	4	16M	32M	Symmetric	12	12	128 MB	256 MB

Table 13. Minimum (Upgradeable) and Maximum Memory Size for each configuration (SDRAM)

SDRAM Tech.	SDRAM Density	SDRAM Width	SDRAM DIMM		SDRAM Addressing	Address Size		SDRAM Size	
			SS x64	DS x64		Row	Column	Min. (UP) (1 row)	Max. (6 rows)
16M	1M	16	1M	2M	Asymmetric	12	8	8 MB	48 MB
	2M	8	2M	4M	Asymmetric	12	9	16 MB	96 MB
	4M	4[1]	4M	8M	Asymmetric	12	10	32 MB	192 MB
64M	2M	32	2M	4M	Asymmetric	12	9	16 MB	96 MB
	2M	32	2M	4M	Asymmetric	13	8	16 MB	96 MB
	4M	16	4M	8M	Asymmetric	14	8	32 MB	192 MB
	8M	8	8M	16M	Asymmetric	14	9	64 MB	256 MB
	16M	4[1]	16M	32M	Asymmetric	14	10	128 MB	256 MB

NOTES:

1. Functionally the 430TX supports x4 SDRAM devices. However, due to loading reasons, it is not recommended that x4 devices be used in 60-MHz and 66-MHz designs.

The memory organization shown below represents the maximum 256 MB of address space. Accesses to memory space above Top-of-DRAM (< 256 MB), video buffer, or the memory gaps (if enabled) are forwarded to PCI, and these regions are not cacheable. Below 1 MB, there are several memory segments which have selectable cacheability. None of the DRAM space occupied by the video buffer (except for SMM usage) or the memory space gaps is remapped (and is therefore "lost").

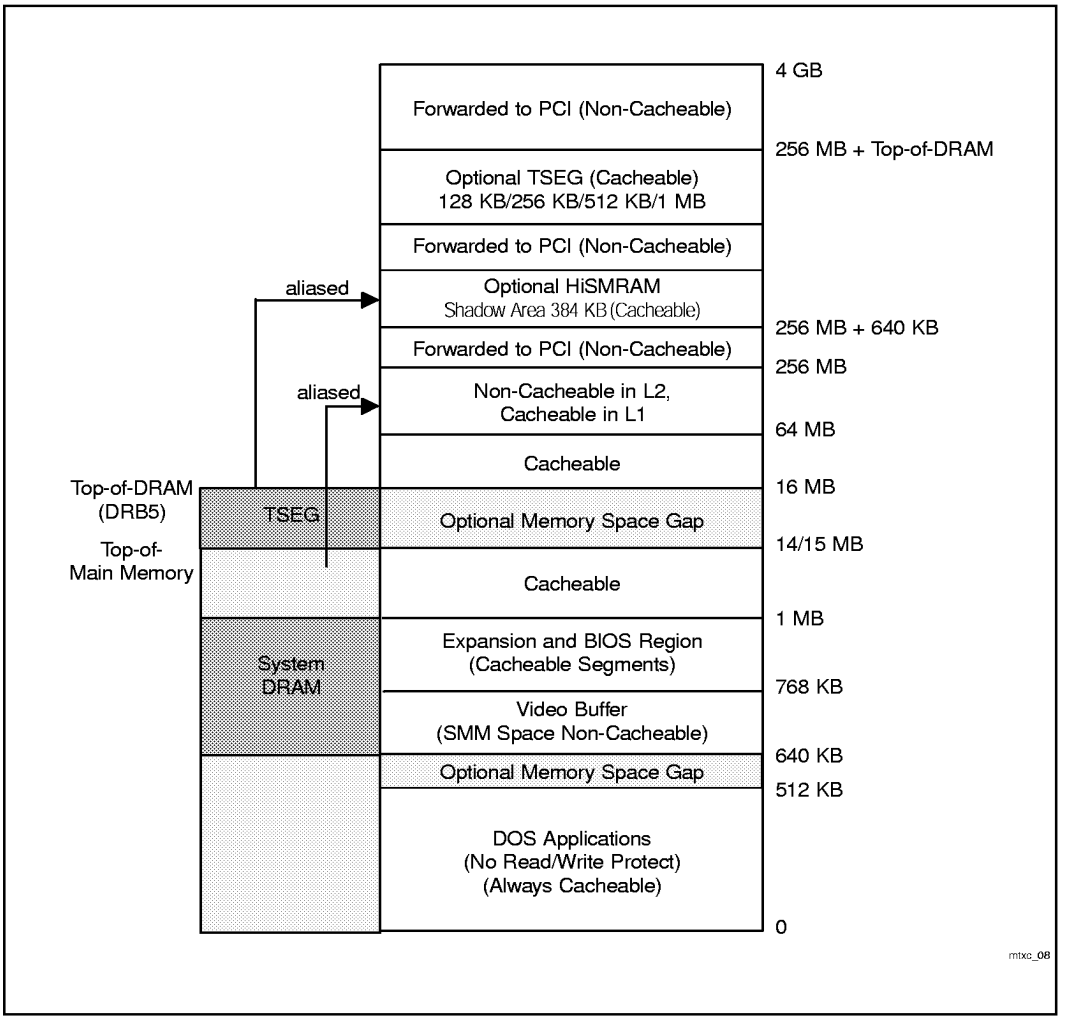


Figure 8. Memory Space Organization

4.3.3. DRAM ADDRESS TRANSLATION

The multiplexed row/column address to the DRAM memory array is provided by the MA[11:0] signals (MA[13:0] for SDRAM 64-Mbit support). The MA bits are derived from the host or PCI address bus as defined by the Table 14. The MTXC supports a 2K byte page size only. The MA lines are translated from the address lines A[26:3] for all memory accesses.

Table 14. MTXC DRAM Address Map Summary

ADDR	MA13	MA12/ BA1	MA11/ BA0	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row	A24	A23	A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Col		A23	A26/ A11	A11/ A25 "V"	A11/ A24/ A26	A11/ A22/ A23/ A25	A10	A9	A8	A7	A6	A5	A4	A3

NOTES:

1. V=Valid level (either 0 or 1) used for SDRAMs. It is 1 during the initialization sequence. It is 0 during normal mode of operation.
2. BA0 and BA1 are the muxed bank selects for SDRAM. Bank select BA1 is required for 64-Mbit SDRAM support.

4.3.4. DRAM PAGING

If DRAMC[bit 4]=1, the MTXC keeps the page open until a page or row miss occurs. If DRAMC[bit 4]=0 (default), the DRAM page is kept open when:

- CPU host bus is non-idle, or
- PCI interface owns the bus.

4.3.5. DRAM TYPES

4.3.5.1. FPM Mode

The MTXC, as a default, supports the standard fast page mode (FPM) DRAM.

4.3.5.2. EDO Mode

Extended Data Out (or Hyper Page Mode) DRAM is designed to improve the DRAM read performance. EDO DRAM holds the memory data valid until the next CAS# falling edge. Compared to standard page mode DRAM which tri-states the memory data when CAS# negates to precharge. With EDO, the CAS# precharge overlaps the memory data valid time. This allows CAS# to negate earlier while still satisfying the memory data valid window time.

4.3.5.3. SDRAM Mode

Synchronous DRAM (SDRAM) implements a fully synchronous interface as compared to a conventional DRAM whose timing delays are related to the rising and falling edges of the RAS#, CAS#, and WE# input signals. The 430TX supports all of the features and timings as shown in the "SDRAM PC" specification. The objective of the *SDRAM* PC Specification is to enable low cost and easily manufactureable SDRAMs for the main stream volume

desktop and Mobile PC's. There are three grade parts defined for the 430TX. All of the speed grade conform to the *SDRAM PC Specification*. For information on the performance of each of the Speed grade parts, refer to the DRAM performance section. The Three speed grade parts are shown in Table 15.

Table 15. SDRAM Speed Grade Parts

Speed Grade	CAS latency (CL)	RAS to CAS (Trcd)	System Frequency
66.67 MHz	3	3	60/66 MHz
66.67 MHz	3	2	60/66 MHz
66.67 MHz	2	2	60/66 MHz

SDRAM Command Reference

The 430TX supports the following commands:

Command
Mode Register Set (MRS)
Activate Bank (ACT)
Read Bank (RD)
Write Bank (WR)
Precharge All Banks (PALL)
Deselect Device

Command
No Operation (NOP)
Auto Refresh CBR (REFR)
Data Write/Output Enable
Data Mask/Output Disable
Self Refresh Entry
Self Refresh Exit

Table 16 MRS command (Mode Register Set) Supported by the MTXC.

Table 16. Command Fields

A11	A10	A9	A8	A7	A[6:4]	A3	A[2:0]
0	0	0	0	0	CL	WT	BL

CAS Latency Field (CL)	
Bits[6:4]	**CAS Latency**
010	2
011	3
All Other	X

Wrap Type Field (WT)	
Bit 3	**Type**
0	X
1	Interleave

The linear order addressing is not supported.

Burst Length Field (BL)	
Bits[2:0]	**Burst Length**
010	4
All Other	X

NOTES:

1. X=Don't Care. These Modes are Don't Care for MTXC specific implementation.

4.3.6. AUTO DETECTION

The SDRAM, FPM, and EDO detection is performed by BIOS. Note that when accessing any of the DRAM related registers (i.e., 54h–68h), refresh should be turned off via the DRAM Control register (DRAMC).

4.3.7. DRAM PERFORMANCE

The DRAM performance is controlled by the DRAM timing register, processor pipelining, and by the type of DRAM used (EDO or FPM or SDRAM). Table 17 depicts both EDO and standard page mode optimum timings. For read cycles, clocks counts are measured from ADS# to BRDY#.

For write cycles, the measurement is broken up into two parts. The first part consists of the rate of posting data in to the CPU to DRAM posted write buffers. This is measured from ADS# to BRDY#. The second part consists of the retire rate from posted write buffers to the DRAM. The leadoff for retiring is measured from the clock after BRDY# assertion to the CAS# assertion.

Table 17 lists the performance summary for 60 ns EDO/FPM DRAMs. The four row column is assuming each row is populated with a maximum of 16, x4 devices=64 DRAM devices. The five row column is assuming each of the first four rows is populated with a maximum of 16, x4 devices and the fifth row is populated with a maximum of eight, x8 devices=72 DRAM devices. The six row column assumes that each of the six rows can be populated with a maximum of 16, x4 devices.

The FELO and SLD bits are used to control the leadoff for read cycles (page hit, row miss, and page miss). Each bit removes one clock from the leadoff, when enabled. Note that FELO impacts EDO only and must be disabled for FPM. The DLT bits are used to control the base starting point for the leadoff for read/write cycles (page miss and row miss, only).

Table 17. EDO/ Standard Page Mode Performance Summary (60 ns DRAMs)

Processor Cycle Type (pipelined)	60/66 MHz w/ four rows	60/66 MHz w/ five rows	60/66 MHz w/ six rows Buffered	DRAM Type
Burst Read Page Hit	5-2-2-2	6-3-3-3	6-3-3-3	EDO
Read Row Miss[1]	8-2-2-2	9-3-3-3	10-3-3-3	EDO
Read Page Miss	11-2-2-2	12-3-3-3	13-3-3-3	EDO
Back-to-Back Burst Reads Page Hit	5-2-2-2-3-2-2-2	6-3-3-3-4-3-3-3	6-3-3-3-4-3-3-3	EDO
Burst Read Page Hit	6-3-3-3	7-4-4-4	7-4-4-4	FPM
Burst Read Row Miss[1]	9-3-3-3	9-4-4-4	9-4-4-4	FPM
Burst Read Page Miss	12-3-3-3	12-4-4-4	12-4-4-4	FPM
Back-to-Back Burst Read Page Hit	6-3-3-3-3-3-3-3	7-4-4-4-4-4-4-4	7-4-4-4-4-4-4-4	FPM
Write Page Hit[2,3,4]	3	3	3	EDO/FPM
Write Row Miss[2,3,4]	6	6	7	EDO/FPM
Write Page Miss[2,3,4]	9	9	10	EDO/FPM
Posted Write[3,4]	3-1-1-1	3-1-1-1	3-1-1-1	EDO/FPM
Write retire rate from Posted Write Buffer	-2-2-2	-3-3-3	-3-3-3	EDO/FPM
Single writes	2	2	3	EDO/FPM
Reg 56h, Bit 4 (SLD)[5]	0	0	0	EDO/FPM
Reg 56h, Bit 5 (FELO)[6]	1	1	1	EDO
Reg 56h, Bit 5 (FELO)[6]	0	0	0	FPM
Reg 58h, Bits[6:5] (DRBT)	2	1	1	EDO/FPM
Reg 58h, Bits[4:3] (DWBT)	2	1	1	EDO/FPM
Reg 58h, Bits[1:0] (DLT)	1	1	0	EDO/FPM
Reg 56h, Bit 6 (RRA)	0	0	0	EDO/FPM

NOTES:

1. The row miss cycles assume that the new page is closed from the prior cycle. Due to the MA[13:0] to RAS# setup requirements, if the page is open, 2 clocks are added to the leadoff.
2. This cycle timing assumes the write buffer(DWB) is empty.
3. Write timing is measured from the clock after BRDY# is returned to the CPU up to CAS# assertion for that cycle.
4. Write data is always posted as 3-1-1-1 (ADS# to BRDY#), if write buffers is available.
5. This bit (SLD) should be set to a 1 (speculative leadoff disable) in systems with cache and to 0 in systems without cache.
6. When set to 1, enables fast timing for EDO timing only. Enables one HCLK pull in for page hit, page miss, and row miss cycles.

Table 18 lists the performance summary for SDRAM. The CL= 3 column represents a CAS latency of 3 part with a RAS to CAS (Trcd) of two clocks. The CL=2 column represents a CAS latency of two part. The performance numbers in Table 18 assume each row is populated with a maximum of eight, x8 devices=40 SDRAM devices.

The SLD bit (page hit, row miss, and page miss) is used to control the leadoff for read cycles. This bit removes one clock from the leadoff, when enabled.

Table 18. SDRAM Performance Summary

Processor Cycle Type	60/66 MHz CL=3 Five Rows (Max)	60/66 MHz CL=2 Five Rows (Max)
Burst Read Page Hit	7-1-1-1	6-1-1-1
Read row Miss[1]	9-1-1-16	8-1-1-1
Read Page Miss	12-1-1-16	11-1-1-1
Back-to-Back Burst Reads Page Hit	7-1-1-1 2-1-1-1	6-1-1-1 2-1-1-1
Write Page Hit[2,3]	3	3
Write Row Miss[2,3]	6	5
Write Page Miss[2,3]	9	8
Posted Write[2,3]	3-1-1-1	3-1-1-1
Write retire rate from Posted Write Buffer	-1-1-1	-1-1-1
Reg 54h, Bit 5 (RCO)[5]	1	0
Reg 54h, Bit 4 (CL)	0	1
Reg 54h, Bit 3 (RT)	0	1
Reg 56h, Bit 4 (SLD)[4]	0	0

NOTES:

1. The row miss cycle assumes that the new page is closed from the prior cycle.
2. This cycle timing assumes the write buffer(DWB) is empty.
3. Write data is always posted as 3-1-1-1 (ADS# to BRDY#), if write buffers is available.
4. This bit (SLD) must be set to a 1 (speculative leadoff disable) in systems with cache and to 0 in systems without cache.
5. For a CL=3 part that can not meet a RAS to CAS timing (Trcd) of two HCLKs, RCO can be set to 0. This will add an HCLK to the leadoff cycle for Row miss and Page miss cycles.

4.3.8. DRAM REFRESH

MTXC supports CAS-before-RAS# (CBR) refresh and Self refresh. The refresh rate is controlled via the DRAM Refresh Rate field in the DRAM Control Register (DRAMC). When a refresh request is generated, it is placed in a four entry queue. The DRAM controller services a refresh request when the refresh queue in not empty and the controller has no other requests pending. When the refresh queue is full, refresh becomes the highest priority request and will be serviced next by the controller.

Refresh is only performed on rows that are populated (i.e., "smart refresh"). The controller determines which rows are populated by looking at the DRB registers. Note that Refresh has to be disabled before the refresh rate is changed.

Refer to bit 5 in the MCTL register (offset 79h) for suspend refresh information.

4.4. PCI CLK Control (CLKRUN#)

4.4.1. CLOCKING STATES

There are three main states in the clocking protocol:

- **Clock Running:** The clock is running and the bus is operational.
- **About to Stop:** The central resource has indicated on the CLKRUN# line that the clock is about to stop.
- **Clock Stopped:** The clock is stopped with CLKRUN# being monitored for a restart

4.4.2. OPERATION

The MTXC is a CLKRUN# Master device and behaves according to the rules for a master device. The PIIX4 companion chip controls the clocks in the system and is the CLKRUN# Central Resource. Please refer to the latest "PCI Mobile Design Guide" for more information.

4.5. SMRAM Memory Space

The MTXC supports the use of main memory as System Management RAM (SMRAM), enabling the use of System Management Mode. The MTXC supports two SMRAM options; Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM).

4.5.1. COMPATIBLE SMRAM (C_SMRAM)

This is the traditional SMRAM feature supported in Intel PCIsets. When this function is enabled via C_BASE_SEG[2:0]=010 and G_SMRAME=1 of the SMRAMC register, the MTXC reserves 000A0000h through 000BFFFFh (A and B segments) of the main memory for use as Noncacheable SMRAM. CPU accesses to segments A and B while not in SMM (i.e., SMIACT# is negated) are always forwarded to the PCI bus. CPU accesses to segments A and B while in SMM (i.e., SMIACT# is asserted) are forwarded to either DRAM or PCI bus, depending on the value of bits[6:0] of the SMRAMC register. PCI masters cannot access the SMRAM area of the main memory. When a PCI master tries to access the SMRAM space, the MTXC does not respond to the PCI cycle (i.e., DEVSEL# is not asserted).

4.5.2. EXTENDED SMRAM (E_SMRAM)

This feature in the MTXC extends the SMRAM space up to 1 Mbytes and provide writeback cacheability. This feature requires that SMI handlers execute above 1 Mbytes which will require rewriting the existing code to

operate properly above 1 Mbytes. However once this is done, then SMI handlers execute at full processor performance.

An error status bit is set in the Extended SMRAM Control register if the CPU tries to access the extended SMRAM space while SMIACT# is negated and D_OPEN bit is 0. This access is forwarded to PCI bus and may result in a Master Abort condition.

Extended SMRAM feature allows up to 1 Mbyte of SMRAM space to be writeback cacheable. This memory space consists of any DRAM not used by the system (as shadow space etc.) between 640 Kbytes and 1 Mbyte (this memory space is referred to as High Memory in this document), and an optional block of memory referred to as the "TSEG". The TSEG is either a 128 Kbyte, 256 Kbyte, 512 Kbytes, or 1 Mbytes block of memory, as defined by TSEG_SZ[1:0] of the SMRAMC register. When TSEG is enabled, the TSEG block of memory is disabled from the top of memory and the system BIOS should report a main memory size of (memorize - TSEG) to the OS.

The two areas of memory available for SMRAM when Extended SMRAM is enabled are:

Physical Address	DRAM Address	
100A0000h to 100FFFFFh	000A0000h to 000FFFFFh	(High Mem)
10000000h plus TOM minus TSEG_SZ to 10000000h plus TOM	TOM minus TSEG_SZ to TOM	(TSEG)

Extended SMRAM option has the following DRAM memory available to it:

Table 19. Extended SMRAM DRAM memory regions

DRAM Area	Size/Availability
A Segment	64 Kbytes always available if enabled (i.e., H_SMRAM=1 and G_SMRAME=1)
B Segment	64 Kbytes always available if enabled (i.e., H_SMRAM=1 and G_SMRAME=1)
C Segment	64 Kbytes available if not used for shadowing (as defined by PAM register) and enabled (i.e., H_SMRAM=1 and G_SMRAME=1)
D Segment	64 Kbytes available if not used for shadowing (as defined by PAM register) and enabled (i.e., H_SMRAM=1 and G_SMRAME=1)
E Segment	64 Kbytes available if not used for shadowing (as defined by PAM register) and enabled (i.e., H_SMRAM=1 and G_SMRAME=1)
F Segment	64 Kbytes only available for suspend/resume (as defined by PAM register) if enabled (i.e., H_SMRAM=1 and G_SMRAME=1)
TSEG	128K, 256K, 512K or 1M bytes available if enabled (i.e., TSEG_EN=1 and G_SMRAME=1)

As with the Compatible SMRAM solution, MTXC does not claim any bus master access to the Extended SMRAM memory ranges defined above. The CPU can access these memory ranges by one of the following mechanisms:

- The processor generating an access to one of the defined memory ranges while in the SMM (SMIACT# is active). A processor access to any of the defined ranges while not in SMM (SMIACT# is inactive) and with the D_OPN bit reset will be forwarded to PCI bus and a status bit is set in the SMRAMC register.
- The processor generating an access to one of the defined memory ranges while the D_OPN bit is set.
- Any modified write access of the processor is allowed to write into the SMRAM space, regardless of the state of the D_OPN, D_CLS, or SMIACT# signals.

The cacheability of SMRAM space is dependent on how much physical DRAM is available in the system. If the system has less than 32 Mbytes of DRAM, the SMRAM is cached in both the L1 and L2. If the system has more than 32 Mbytes of DRAM, the SMRAM is cached in only the L1.

4.5.3. SMRAM PROGRAMMING CONSIDERATIONS

When using the Extended SMRAM configuration, the SMI handler software must be extremely careful when accessing DRAM memory in the 100A0000h to 100FFFFFh memory range. First, if this area of memory is accessed while the CPU is not in SMM mode and the D_OPN bit is not set, the MTXC will forward the cycle to PCI bus which may cause a fatal system error and system shutdown. Second, only areas within the 100A0000h to 100FFFFFh region that have been selected as SMRAM space should be accessed; otherwise, the L1 and L2 caches will become incoherent, which will cause a future system error. Any memory in normal DRAM space that is not used in OS or application space can be used as SMRAM memory.

4.6. Low Power States

MTXC supports five types of low power states: Chip Standby, Power On Suspend (POS), Suspend to RAM (STR), Suspend to Disk (STD), and dynamic stop clock. The Table 20 summarizes the various MTXC's Low power states.

Table 20. 430TX Low Power State Summary

PM Mode	Description	Exit Latency Target
Chip Standby	When MTXC's CPU and PCI busses are both idle, MTXC enters this state.	No delay
Dynamic Stop Clock	MTXC provides provisions that enable transitioning the CPU in and out of the stop clock state in an active system. This includes the ability to disable the system arbiter and transition the memory controller in and out of the suspend refresh state.	<10 ms
Powered On Suspend (POS)	System PLLs are powered down, only running clock is the RTC clock and the SUSCLK. MTXC maintains DRAM refresh using SUSCLK.	<10 ms
Suspend to RAM (STR)	CPU complex (CPU and L2) and PCI interface are powered off. Only the RTC clock and SUSCLK are running. MTXC maintains DRAM refresh using SUSCLK.	~1 sec
Suspend to Disk(STD)	CPU complex (CPU and L2), DRAM and PCI interface are powered off.	~30 sec

The 430TX system maintains a very low power CPU complex by utilizing the different power down features available from the CPU, cache data RAMs and utilizing leading edge low power design techniques in the 430TX system components. The 430TX components work in unison to dynamically control the CPU complexes power state without adversely affecting performance. The following gives a brief description of how the 430TX system components achieve these low power states.

The MTXC and PIIX4 work in unison to maintain a very low power L2 subsystem without adversely affecting peak performance.

NOTE

There are some system restrictions when DRAM Cache is implemented in a system that supports STP_CLK, POS, and STR power management modes. Since KRQAK is not implemented in the "Suspend Well," the correct operation of KRQAK is not guaranteed when the system enters the above mentioned power management modes. To avoid data corruption in the L2 cache, a system that implements the STP_CLK, POS, and STR modes must abide by the following rules:

1. Before entering these power management modes, the DRAM cache must be flushed so that all modified lines end up in system memory.
2. After exiting these power management modes, the DRAM Cache must be reinitialized.

4.6.1. CHIP STANDBY

The MTXC also supports a chip standby mode. When the MTXC determines that both its CPU interface and PCI interface are idle, it will dynamically place itself into a very low power state. While in chip standby state the MTXC is able to respond to new CPU or PCI bus master accesses with no performance penalty. This provides very optimized power/performance characteristics because the CPU interface are idle for large periods of time. The MTXC enters Chip Standby mode when the following conditions are true:

- Host Bus idle
- PCI bus Idle
- Normal Mode (i.e., not Test Mode)
- Not in RESET state
- Internal operations idle

Entering the Chip Standby state is not dependent on any timer expiration. When the above conditions are met, the MTXC can enter the chip standby state as soon as it can.

4.6.2. SUSPEND/RESUME

The MTXC supports POS, STR, STD and SOFF (Soft Off) suspend states. The MTXC supports the POS mode by maintaining all of its power planes when in the suspend state. The MTXC supports the STR modes by isolating its CPU and PCI interfaces, and only maintaining the DRAM refresh off the SUSCLK signal. When exiting the STR modes, the MTXC's core well is reset and its context is lost (the power management context is not lost however). The MTXC supports the STD and SOFF modes by being totally powered off.

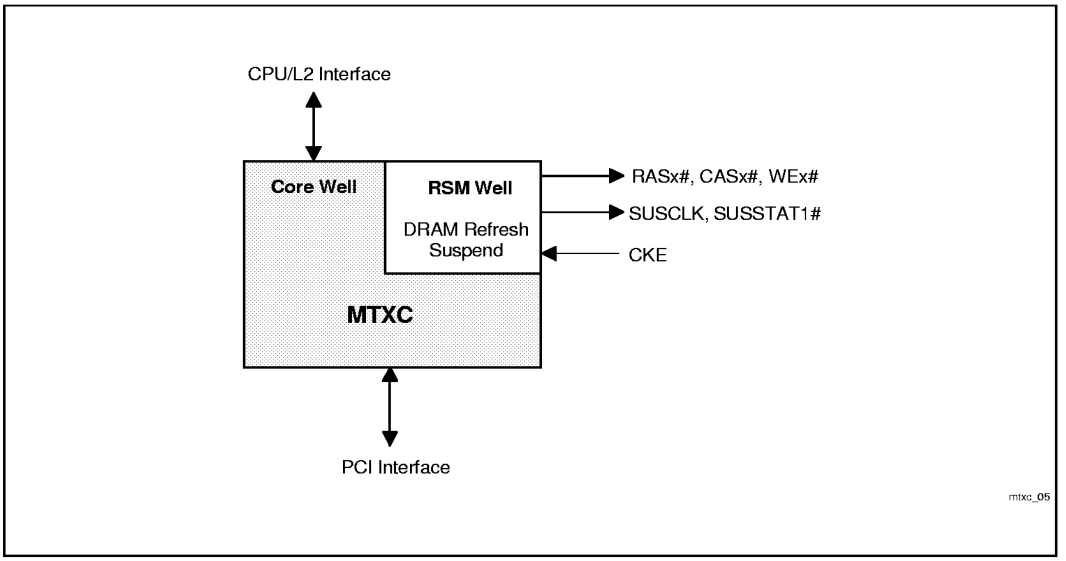


Figure 9. MTXC Power Planes

4.6.2.1. Power Transition Changes

The MTXC supports several suspend modes that support the PIIX4 system suspend states. Table 21 illustrates what suspend mode the MTXC enters upon the appropriate PIIX4 suspend mode.

Table 21. Power Transition States

PIIX4 Suspend State	MTXC Suspend State	MTXC Description
POS	PonS	All interfaces enabled, clocks stopped.
STR	PoffS	CPU, L2, PCI interfaces disabled
STD	Off	Chip is off.
Off/Soft Off	Off	Chip is off.

The core logic should be reset when the PCI bus is reset. This means that the refresh logic and power sequencing logic is not reset during resumes (part of the resume well).

4.7. PCI Interface

The MTXC integrates a high performance interface to the PCI local bus taking full advantage of the high bandwidth and low latency of PCI. The MTXC is fully PCI 2.1 compliant. Table 22 lists the PCI bus commands supported. Five PCI masters are supported by the integrated arbiter including the PIIX4 and four general PCI masters. The MTXC acts as a PCI master for CPU accesses to PCI. The PCI bus is clocked at one half the frequency of the CPU clock. This divided synchronous interface minimizes latency for CPU-to-PCI cycles and PCI-to-main memory cycles.

The MTXC integrates posted write buffers for CPU memory writes to PCI. Back-to-back sequential memory writes to PCI are converted to burst writes on PCI. This feature allows the CPU to continue posting DWord writes at the maximum bandwidth for the Pentium processor for the highest possible transfer rates to the graphics frame buffer.

Read prefetch and write posting buffers in the MTXC enable PCI masters to access main memory at up to 120 MB/sec. The MTXC incorporates a snoop ahead feature that allows PCI masters to continue bursting on both reads and writes even as the bursts cross cache line boundaries.

The MTXC forwards each of the CPU shutdown, Halt, and Stop Grant cycles to the PCI bus as special cycles. These cycles are terminated on PCI as master abort and a BRDY# is returned to the CPU. The Stop Grant cycle is propagated with 0002h in the message field and 0012h in the message dependent data field.

Table 22. PCI Commands

C/BE#	Command	Target Support	Initiator Support
0000	Interrupt Acknowledge	NO	YES
0001	Special cycle	NO	YES
0010	I/O read	YES	YES
0011	I/O write	YES	YES
0100	reserved	NO	NO
0101	reserved	NO	NO
0110	Memory read	YES	YES
0111	Memory write	YES	YES
1000	reserved	NO	NO
1001	reserved	NO	NO
1010	Configuration Read	NO	YES
1011	Configuration Write	NO	YES
1100	Memory Read Multiple	As Memory Read	NO
1101	Dual Address Cycle	NO	NO
1110	Memory Read Line	As Memory Read	NO
1111	Memory Write and Invalidate	As Memory Write	NO

4.8. System Arbitration

The MTXC's PCI Bus Arbiter allows PCI peer-to-peer traffic concurrent with CPU main memory/second level cache cycles. The arbiter supports five PCI masters. REQ[3:0]#/GNT[3:0]# are used by PCI masters other than the PCI-to-ISA expansion bridge (PIIX4). PHLD#/PHLDA# are the arbitration request/grant signals for the PIIX4 and provide guaranteed access time capability for ISA masters. PHLD#/PHLDA# also optimize system performance based on the PIIX4 known policies.

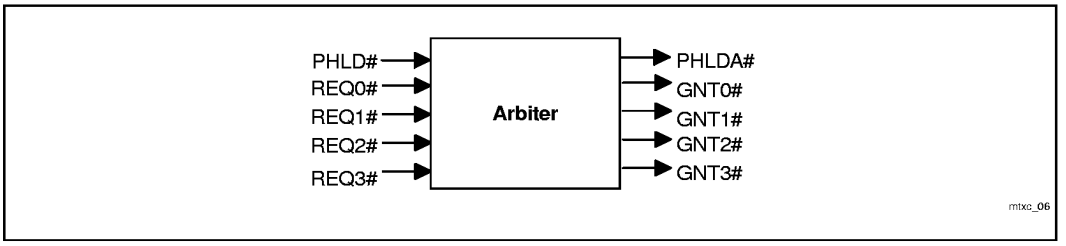
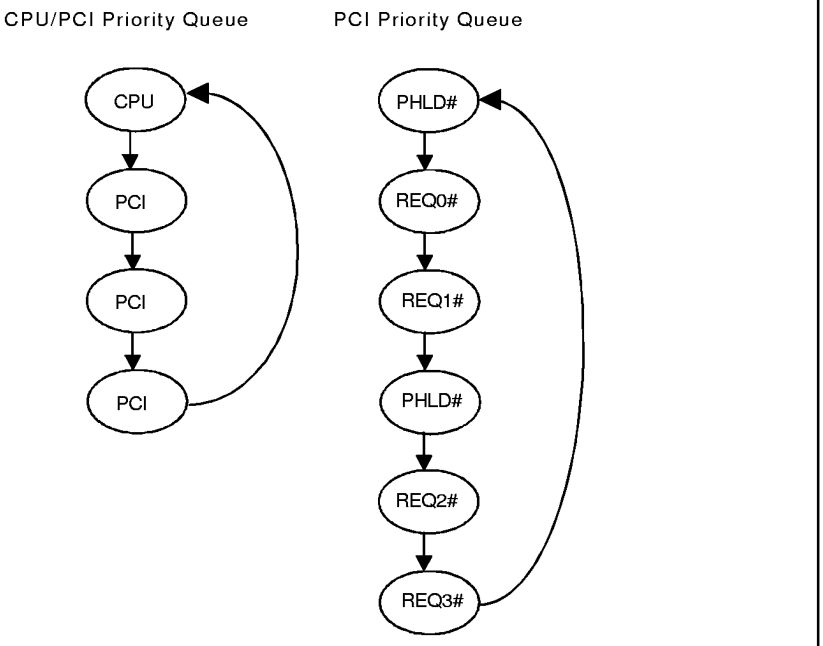


Figure 10. PCI Arbiter

4.8.1. PRIORITY SCHEME AND BUS GRANT

The highest priority requester is determined by a fixed order queue together with a highest priority pointer. Although the priority ring is fixed, the highest priority pointer moves to determine which PCI agent is at the top (and bottom) of the queue. The arbiter counts three grant assertions to requesters different than the one it is currently granting (and all grants within MTT are collapsed to one) to decide when it's time to let the host in.

The grant signals (GNTx#) are normally negated after recognition of FRAME# assertion, or 16 PCLKs from grant assertion, if no cycle has started.



NOTES:

1. In the PCI Priority Queue, the last agent granted is always dropped to the bottom of the queue for the next arbitration cycle, but the order of the chain is always preserved.
2. In the PCI Priority Queue, if PHLD is at the bottom of the queue, the upper PHLD slot is masked. This prevents back-to-back PHLD grants, if other PCI request are pending.
3. In the CPU/PCI priority Queue, the CPU is granted high priority status after 3 consecutive PCI grants. If three consecutive PCI grants have not been counted down, then the CPU can be granted the bus as the low priority agent.

Figure 11. Arbitration Priority Rotation

Multi-Transaction Timer (MTT)

The priority chain algorithm has been enhanced by the Multi-Transaction Timer (MTT) mechanism. Once a PCI agent is granted, the MTT is started. This timer then counts down in PCI clocks from its preset value to zero. Until the timer expires, that agent will be promoted to being the highest priority PCI agent for the next grant event.

4.8.2. CPU POLICIES

The CPU never explicitly requests the bus. Instead, the arbiter grants the bus to the CPU when:

- The CPU is the highest priority
- PCI agents do not require main memory (peer-to-peer transfers or bus idle) and the PCI bus is not currently locked by a PCI master

When the CPU is granted as highest priority, the MLT timer is used to guarantee a minimum amount of system resources to the CPU before another requesting PCI agent is granted.

5.0. CLOCKS AND RESET

5.1. Clock Generation and distribution

The MTXC and CPU should be clocked from one clock driver output to minimize skew between the CPU & MTXC.

5.2. RESET Sequencing

The MTXC is asynchronously reset when the RST# signal is asserted.

The MTXC arbiter includes support for PCI central resource functions. These functions include driving the AD[31:0],C/BE[3:0]#, and the PAR signals when no one is granted the PCI bus and the PCI bus is idle. The MTXC drives 0's on these signals during these times, plus during RESET.

6.0. PINOUT INFORMATION

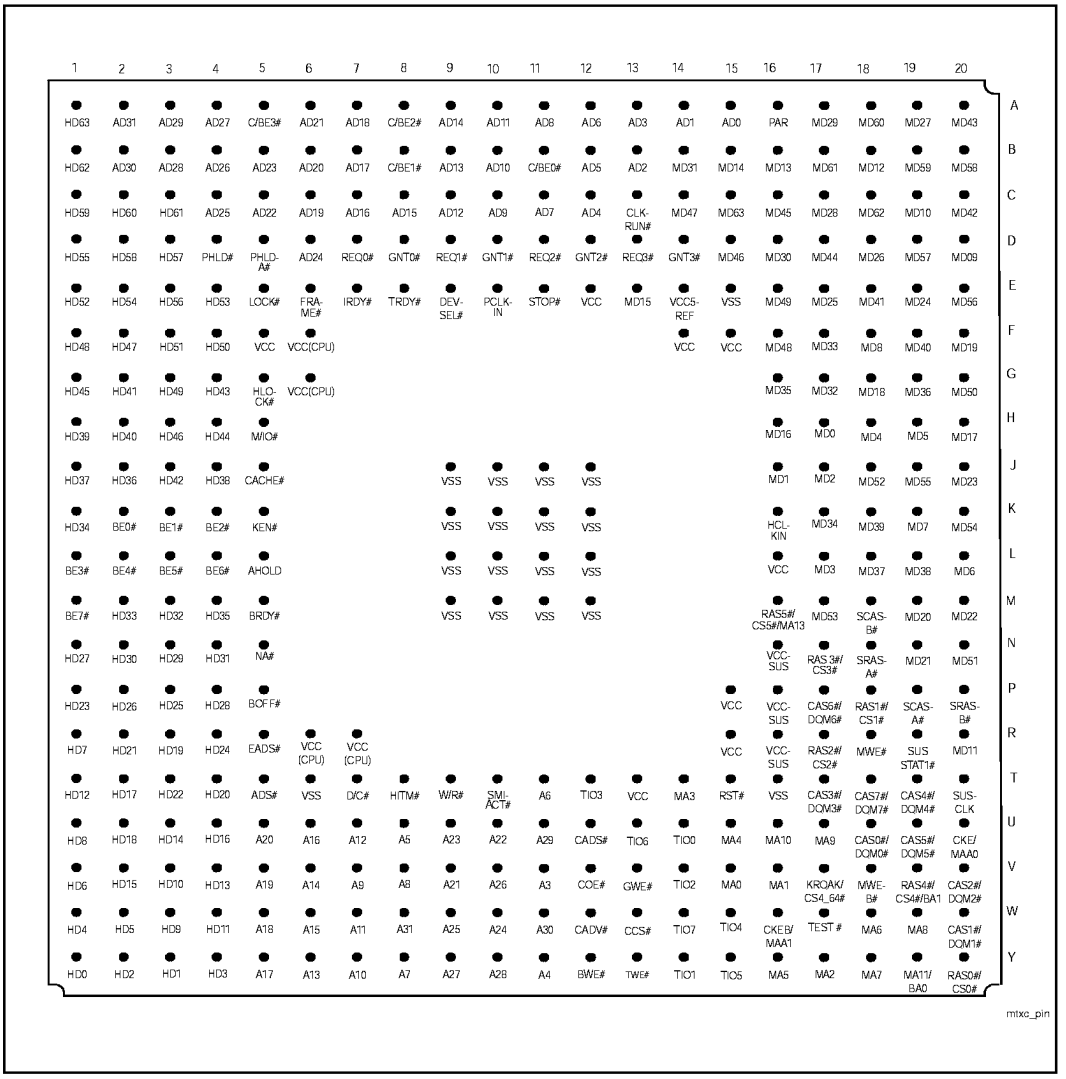


Figure 12. MTXC Pinout (Top View)

Table 23. MTXC Alphabetical Pin List

Pin	Ball
A10	Y07
A11	W07
A12	U07
A13	Y06
A14	V06
A15	W06
A16	U06
A17	Y05
A18	W05
A19	V05
A20	U05
A21	V09
A22	U10
A23	U09
A24	W10
A25	W09
A26	V10
A27	Y09
A28	Y10
A29	U11
A3	V11
A30	W11
A31	W08
A4	Y11
A5	U08
A6	T11
A7	Y08
A8	V08
A9	V07

Table 23. MTXC Alphabetical Pin List

Pin	Ball
AD0	A15
AD1	A14
AD10	B10
AD11	A10
AD12	C09
AD13	B09
AD14	A09
AD15	C08
AD16	C07
AD17	B07
AD18	A07
AD19	C06
AD2	B13
AD20	B06
AD21	A06
AD22	C05
AD23	B05
AD24	D06
AD25	C04
AD26	B04
AD27	A04
AD28	B03
AD29	A03
AD3	A13
AD30	B02
AD31	A02
AD4	C12
AD5	B12
AD6	A12

Table 23. MTXC Alphabetical Pin List

Pin	Ball
AD7	C11
AD8	A11
AD9	C10
ADS#	T05
AHOLD	L05
BE0#	K02
BE1#	K03
BE2#	K04
BE3#	L01
BE4#	L02
BE5#	L03
BE6#	L04
BE7#	M01
BOFF#	P05
BRDY#	M05
BWE#	Y12
C/BE0#	B11
C/BE1#	B08
C/BE2#	A08
C/BE3#	A05
CACHE#	J05
CADS#	U12
CADV#	W12
CAS0#/DQM0#	U18
CAS1#/DQM1#	W20
CAS2#/DQM2#	V20
CAS3#/DQM3#	T17
CAS4#/DQM4#	T19
CAS5#/DQM5#	U19

Table 23. MTXC Alphabetical Pin List

Pin	Ball
CAS6#/DQM6#	P17
CAS7#/DQM7#	T18
CCS#	W13
CKE/MAA0	U20
CKEB/MAA1	W16
CLKRUN#	C13
COE#	V12
D/C#	T07
DEVSEL#	E09
EADS#	R05
FRAME#	E06
GNT0#	D08
GNT1#	D10
GNT2#	D12
GNT3#	D14
GWE#	V13
HCLKIN	K16
HD0	Y01
HD1	Y03
HD10	V03
HD11	W04
HD12	T01
HD13	V04
HD14	U03
HD15	V02
HD16	U04
HD17	T02
HD18	U02
HD19	R03

Table 23. MTXC Alphabetical Pin List

Pin	Ball
HD2	Y02
HD20	T04
HD21	R02
HD22	T03
HD23	P01
HD24	R04
HD25	P03
HD26	P02
HD27	N01
HD28	P04
HD29	N03
HD3	Y04
HD30	N02
HD31	N04
HD32	M03
HD33	M02
HD34	K01
HD35	M04
HD36	J02
HD37	J01
HD38	J04
HD39	H01
HD4	W01
HD40	H02
HD41	G02
HD42	J03
HD43	G04
HD44	H04
HD45	G01

Table 23. MTXC Alphabetical Pin List

Pin	Ball
HD46	H03
HD47	F02
HD48	F01
HD49	G03
HD5	W02
HD50	F04
HD51	F03
HD52	E01
HD53	E04
HD54	E02
HD55	D01
HD56	E03
HD57	D03
HD58	D02
HD59	C01
HD6	V01
HD60	C02
HD61	C03
HD62	B01
HD63	A01
HD7	R01
HD8	U01
HD9	W03
HITM#	T08
HLOCK#	G05
IRDY#	E07
KEN#	K05
KRQAK/ CS4_64#	V17
LOCK#	E05

Table 23. MTXC Alphabetical Pin List

Pin	Ball
M/IO#	H05
MA0	V15
MA1	V16
MA10	U16
MA11/BA0	Y19
MA2	Y17
MA3	T14
MA4	U15
MA5	Y16
MA6	W18
MA7	Y18
MA8	W19
MA9	U17
MD0	H17
MD1	J16
MD10	C19
MD11	R20
MD12	B18
MD13	B16
MD14	B15
MD15	E13
MD16	H16
MD17	H20
MD18	G18
MD19	F20
MD2	J17
MD20	M19
MD21	N19
MD22	M20

Table 23. MTXC Alphabetical Pin List

Pin	Ball
MD23	J20
MD24	E19
MD25	E17
MD26	D18
MD27	A19
MD28	C17
MD29	A17
MD3	L17
MD30	D16
MD31	B14
MD32	G17
MD33	F17
MD34	K17
MD35	G16
MD36	G19
MD37	L18
MD38	L19
MD39	K18
MD4	H18
MD40	F19
MD41	E18
MD42	C20
MD43	A20
MD44	D17
MD45	C16
MD46	D15
MD47	C14
MD48	F16
MD49	E16

Table 23. MTXC Alphabetical Pin List

Pin	Ball
MD5	H19
MD50	G20
MD51	N20
MD52	J18
MD53	M17
MD54	K20
MD55	J19
MD56	E20
MD57	D19
MD58	B20
MD59	B19
MD6	L20
MD60	A18
MD61	B17
MD62	C18
MD63	C15
MD7	K19
MD8	F18
MD9	D20
MWE#	R18
MWEB#	V18
NA#	N05
PAR	A16
PCLKIN	E10
PHLD#	D04
PHLDA#	D05
RAS0#/CS0#	Y20
RAS1#/CS1#	P18
RAS2#/CS2/#	R17

Table 23. MTXC Alphabetical Pin List

Pin	Ball
RAS3#/CS3#	N17
RAS4#/CS4#/ BA1	V19
RAS5#/CS5#/ MA13	M16
REQ0#	D07
REQ1#	D09
REQ2#	D11
REQ3#	D13
RST#	T15
SCASA#	P19
SCASB#	M18
SMIACT#	T10
SRASA#	N18
SRASB#	P20
STOP#	E11
SUSCLK	T20
SUSSTAT1#	R19

Table 23. MTXC Alphabetical Pin List

Pin	Ball
TEST#	W17
TIO0	U14
TIO1	Y14
TIO2	V14
TIO3	T12
TIO4	W15
TIO5	Y15
TIO6	U13
TIO7	W14
TRDY#	E08
TWE#	Y13
W/R#	T09
V_{CC}	F05, L16, R15, F15, E12, P15, F14, T13

Table 23. MTXC Alphabetical Pin List

Pin	Ball
V_{CC} (CPU)	F06, G06, R07, R06
V_{CC} (SUS)	R16, N16, P16
V_{CC}5REF	E14
V_{SS}	E15, J9, J10 J11, J12, K09, K10, K11, K12, L09, L10, L11, L12, M09, M10, M11, M12, T06, T16

7.0. MTXC PACKAGE INFORMATION

This specification outlines the mechanical dimensions for the MTXC. The package is a 324 pin ball grid array (BGA).

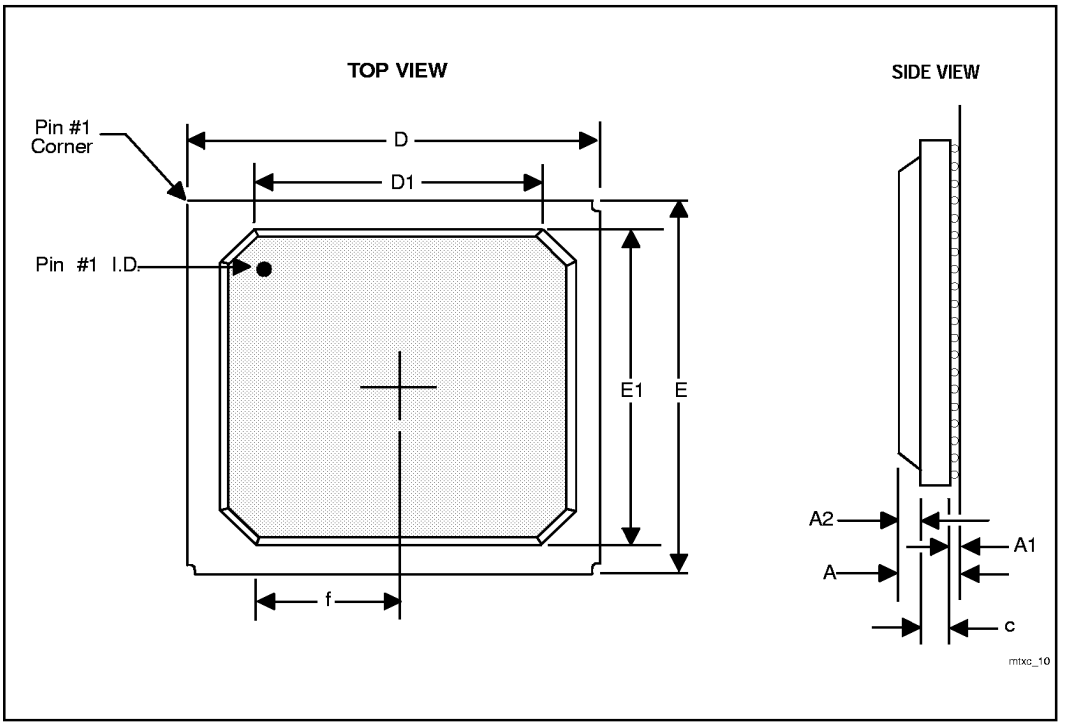


Figure 13. MTXC 324-pin Ball Grid Array (BGA)

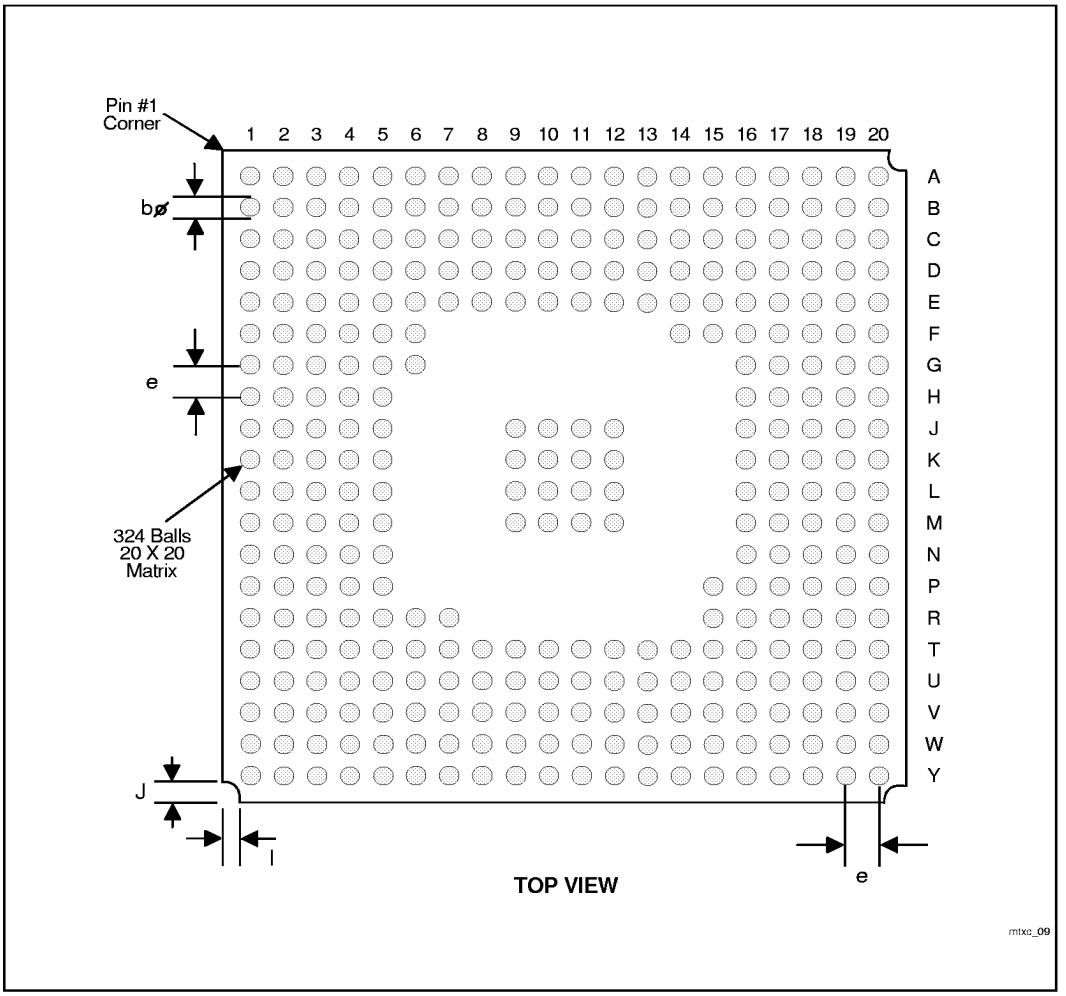


Figure 14. MTXC 324-pin Ball Grid Array (BGA) Ball Pattern

Table 24. MTXC 324-pin Ball Grid Array (BGA)

Symbol	e=1.27 (solder ball pitch)		
	Min[1]	Nominal[1]	Max[1]
A	1.95	2.13	2.28
A1	0.50	0.60	0.70
A2	1.12	1.17	1.22
D	26.80	27.00	27.20
D1		24.00	24.70
E	26.80	27.00	27.20
E1		24.00	24.70
I	1.44 REF.		
J	1.44 REF.		
M[2]	20 (Depopulated)		
N[3]	324		
b	0.60	0.76	0.90
c	0.32	0.36	0.40
f	8.05 REF.		
Remark	2 Layer		

NOTES:
1. All dimensions are in millimeters.
2. 'M' represents the maximum solder ball matrix size.
3. 'N' represents the maximum allowable number of solder balls.

8.0. TESTABILITY

8.1. NAND Tree Mode

A NAND tree mode is provided for Automated Test Equipment (ATE) board level testing. The NAND tree allows the tester to set the connectivity of each of the MTXC's signal pins. In Mobile/desktop mode, the NAND tree mode is activated by driving the test pin TEST# low when REQx# pins are at 0010. If TEST# is negated at any time, the test mode is deactivated and the MTXC goes back to normal operation. There is no guarantee that upon re-entering normal operation the chip will function properly, if the test mode was entered while the MTXC was not in a completely idle state.

The MTXC has several test modes to improve board manufacturing. If the TEST# signal is asserted (driven low), the value on the REQ[3:0]# indicates the test mode to enable. The test mode enabled at the falling edge of TEST# will remain enabled until TEST# is negated.

Table 25 shows each test mode and the value of REQ#[3:0] required to enable it. All other values of REQ[3:0]# while TEST# is active, are reserved and should not be asserted by the customer.

Table 25. Test Modes

REQ[3:0]#	TEST#	PHLD#	TEST Mode	Description
0010	0	x	NAND Chain	Float outputs, enable NAND chains on GNT[3:0]#
1110	0	1	ID/REV code	Drives Device ID on AD[31:16] and revision ID on AD[7:0]
1110	0	0	MID Code	Drives Manufacture ID on AD[31:0]
1111	0	x	Disable test mode[1]	Disables any active test mode, puts MTXC back into normal mode

NOTES:

1. It is recommended to assert RST# if this mode is used, to guarantee pins and PCIset will function normally.

8.2. NAND Chain Mode

In NAND Tree mode, all outputs are tri-stated, except for GNT#[3:0]. These pins contain the NAND Chain. Note, also, that the internal pull-ups and pull-downs are still active. Because of the 282 pins in the NAND Chain, it must be separated into 4 chains. Two chains contain 72 pins each, 1 chain contains 70 pins, and 1 chain contains 68 pins. The MTXC remains in this mode until a new test mode is selected or RST# is asserted. The HCLK and PCLK are part of the NAND Chain and *must* be deactivated during this test.

HCLK and PCLK need to run for a few clocks in the beginning to put the MTXC in the NAND chain mode. During the testing of chains 2 and 3, SUSSTAT# will be held high throughout the test. RST#, TEST#, and SUSSTAT1# are not part of the NAND chain. The following tables show the pin order for each chain:

Table 26. Chain #0 (GNT#0)

Pin Name	Chain Element
A25	CH0_00
A7	CH0_01
A10	CH0_02
A21	CH0_03
A23	CH0_04
SMIACT#	CH0_05
A31	CH0_06
A18	CH0_07
HD3	CH0_08
A12	CH0_09
A14	CH0_10
HD11	CH0_11
A19	CH0_12
A16	CH0_13
HITM#	CH0_14
HD13	CH0_15
D/C#	CH0_16
HD0	CH0_17
HD10	CH0_18
HD16	CH0_19
HD6	CH0_20
HD14	CH0_21
BOFF#	CH0_22
HD18	CH0_23

Table 26. Chain #0 (GNT#0)

Pin Name	Chain Element
HD24	CH0_24
HD8	CH0_25
HD19	CH0_26
HD7	CH0_27
HD31	CH0_28
HD26	CH0_29
HD27	CH0_30
HD33	CH0_31
AHOLD	CH0_32
BE5#	CH0_33
BE6#	CH0_34
HD34	CH0_35
BE2#	CH0_36
BE0#	CH0_37
HD37	CH0_38
BE1#	CH0_39
HD36	CH0_40
HD41	CH0_41
HD52	CH0_42
CACHE#	CH0_43
HD47	CH0_44
HD44	CH0_45
HD49	CH0_46
HD54	CH0_47

Table 26. Chain #0 (GNT#0)

Pin Name	Chain Element
HD55	CH0_48
HD57	CH0_49
HLOCK#	CH0_50
HD53	CH0_51
HD60	CH0_52
HD62	CH0_53
HD61	CH0_54
AD30	CH0_55
AD25	CH0_56
AD22	CH0_57
AD24	CH0_58
AD27	CH0_59
AD19	CH0_60
C/BE3#	CH0_61
REQ0#	CH0_62
AD20	CH0_63
AD21	CH0_64
TRDY#	CH0_65
AD16	CH0_66
C/BE2#	CH0_67
C/BE1#	CH0_68
AD14	CH0_69
AD12	CH0_70
AD13	CH0_71

Table 27. Chain #1 (GNT#1)

Pin Name	Chain Element
A24	CH1_00
A27	CH1_01
A26	CH1_02
A13	CH1_03
A8	CH1_04
W/R#	CH1_05
A11	CH1_06
A17	CH1_07
A15	CH1_08
A5	CH1_09
A9	CH1_10
HD1	CH1_11
HD9	CH1_12
A20	CH1_13
HD2	CH1_14
HD5	CH1_15
HD4	CH1_16
ADS#	CH1_17
HD15	CH1_18
EADS#	CH1_19
HD20	CH1_20
HD17	CH1_21
HD22	CH1_22
HD12	CH1_23

Table 27. Chain #1 (GNT#1)

Pin Name	Chain Element
HD28	CH1_24
HD21	CH1_25
NA#	CH1_26
HD25	CH1_27
BRDY#	CH1_28
HD23	CH1_29
HD35	CH1_30
HD29	CH1_31
HD30	CH1_32
BE7#	CH1_33
HD32	CH1_34
BE3#	CH1_35
BE4#	CH1_36
HD39	CH1_37
HD45	CH1_38
HD42	CH1_39
HD38	CH1_40
HD40	CH1_41
HD48	CH1_42
KEN#	CH1_43
HD46	CH1_44
HD43	CH1_45
HD51	CH1_46
HD58	CH1_47

Table 27. Chain #1 (GNT#1)

Pin Name	Chain Element
HD56	CH1_48
HD50	CH1_49
M/IO#	CH1_50
HD59	CH1_51
HD63	CH1_52
PHLD#	CH1_53
AD31	CH1_54
LOCK#	CH1_55
AD28	CH1_56
FRAME#	CH1_57
AD29	CH1_58
PHLDA#	CH1_59
IRDY#	CH1_60
AD26	CH1_61
AD23	CH1_62
AD17	CH1_63
DEVSEL#	CH1_64
AD18	CH1_65
REQ1#	CH1_66
AD15	CH1_67
PCLKIN	CH1_68
AD11	CH1_69
AD10	CH1_70
AD9	CH1_71

Table 28. Chain #2 (GNT#2)

Pin Name	Chain Element
A28	CH2_00
A29	CH2_01
A3	CH2_02
A30	CH2_03
A4	CH2_04
COE#	CH2_05
BWE#	CH2_06
CCS#	CH2_07
MA5	CH2_08
MA10	CH2_09
KRQAK/ CS4_64#	CH2_10
MA7	CH2_11
MA11	CH2_12
MA6	CH2_13
MA9	CH2_14
MWEB#	CH2_15
RAS0#	CH2_16
RAS4#	CH2_17
RAS2#	CH2_18
CAS7#	CH2_19
CAS5#	CH2_20
CAS6#	CH2_21
CKE/MAA0	CH2_22

Table 28. Chain #2 (GNT#2)

Pin Name	Chain Element
CAS4#	CH2_23
SUSCLK	CH2_24
SRASA	CH2_25
MD11	CH2_26
MD53	CH2_27
SCASB#	CH2_28
MD22	CH2_29
MD6	CH2_30
MD34	CH2_31
MD39	CH2_32
MD7	CH2_33
MD54	CH2_34
HCLKIN	CH2_35
MD55	CH2_36
MD5	CH2_37
MD17	CH2_38
MD2	CH2_39
MD50	CH2_40
MD1	CH2_41
MD0	CH2_42
MD18	CH2_43
MD16	CH2_44
MD19	CH2_45
MD40	CH2_46

Table 28. Chain #2 (GNT#2)

Pin Name	Chain Element
MD32	CH2_47
MD25	CH2_48
MD26	CH2_49
MD42	CH2_50
MD48	CH2_51
MD49	CH2_52
MD59	CH2_53
MD43	CH2_54
MD30	CH2_55
MD27	CH2_56
MD28	CH2_57
MD12	CH2_58
MD60	CH2_59
CLKRUN#	CH2_60
AD0	CH2_61
AD2	CH2_62
STOP#	CH2_63
AD4	CH2_64
AD3	CH2_65
AD5	CH2_66
AD7	CH2_67
AD6	CH2_68
REQ2#	CH2_69

Table 29. Chain #3 (GNT#3)

Pin Name	Chain Element
A22	CH3_00
CADV#	CH3_01
A6	CH3_02
TWE#	CH3_03
GWE#	CH3_04
CADS#	CH3_05
TIO1	CH3_06
TIO3	CH3_07
TIO7	CH3_08
TIO6	CH3_09
TIO2	CH3_10
TIO5	CH3_11
TIO4	CH3_12
TIO0	CH3_13
MA0	CH3_14
MA2	CH3_15
MA4	CH3_16
CKEB/ MAA1	CH3_17
MA1	CH3_18
MA3	CH3_19
MA8	CH3_20
CAS1#	CH3_21
CAS3#	CH3_22

Table 29. Chain #3 (GNT#3)

Pin Name	Chain Element
CAS0#	CH3_23
CAS2#	CH3_24
MWEB#	CH3_25
RAS1#	CH3_26
RAS3#	CH3_27
RAS5#	CH3_28
SCASA	CH3_29
MD21	CH3_30
SRASB#	CH3_31
MD51	CH3_32
MD20	CH3_33
MD37	CH3_34
MD38	CH3_35
MD3	CH3_36
MD52	CH3_37
MD23	CH3_38
MD4	CH3_39
MD36	CH3_40
MD56	CH3_41
MD8	CH3_42
MD9	CH3_43
MD33	CH3_44
MD24	CH3_45

Table 29. Chain #3 (GNT#3)

Pin Name	Chain Element
MD41	CH3_46
MD57	CH3_47
MD35	CH3_48
MD58	CH3_49
MD10	CH3_50
MD44	CH3_51
MD62	CH3_52
MD15	CH3_53
MD46	CH3_54
MD45	CH3_55
MD61	CH3_56
MD63	CH3_57
MD29	CH3_58
MD13	CH3_59
MD47	CH3_60
REQ3#	CH3_61
MD14	CH3_62
PAR	CH3_63
MD31	CH3_64
AD1	CH3_65
C/BE0#	CH3_66
AD8	CH3_67