REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
E	Added vendor cage 88379 for device types 01 through 05. Figure 1; Added the pin reference numbers on the top view of case outline Y to indicate the pin orientation. -sld	99-03-29	K. A. Cottongim

REV																			
SHEET																			
REV	E	E	E	E	E	E	E												
SHEET	15	16	17	18	19	20	21												

REV STATUS OF SHEETS															
REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
95-12-12

REVISION LEVEL
E

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, MEMORY, DIGITAL, FLASH EPROM, 128K X 8-BIT, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-96690**

SHEET 1 OF 21

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes, class D (lowest reliability), class E, (exceptions), class G (lowest high reliability), class H (high reliability), and class K, (highest reliability) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:

5962	-	96690	01	H	X	X
Federal stock class designator		RHA designator (see 1.2.1)	Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

Drawing number

1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	WMF128K8-150CQ5, ACT-F128K8N-150P4Q	FLASH EPROM, 128K x 8-bit	150 ns
02	WMF128K8-120CQ5, ACT-F128K8N-120P4Q	FLASH EPROM, 128K x 8-bit	120 ns
03	WMF128K8-90CQ5, ACT-F128K8N-090P4Q	FLASH EPROM, 128K x 8-bit	90 ns
04	WMF128K8-70CQ5, ACT-F128K8N-070P4Q	FLASH EPROM, 128K x 8-bit	70 ns
05	WMF128K8-60CQ5, ACT-F128K8N-060P4Q	FLASH EPROM, 128K x 8-bit	60 ns

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device performance documentation
D, E, G, H, or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
T	See figure 1	32	Flatpack, ceramic, single cavity
U	See figure 1	32	Flatpack, ceramic, single cavity, lead formed
X	See figure 1	32	SOJ, ceramic, single cavity
Y	See figure 1	32	DIP, ceramic, single cavity

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) 2/	-2.0 V dc to +7.0 V dc
Signal voltage range (any pin except A9) 2/	-2.0 V dc to +7.0 V dc
Power dissipation (P_D)	275 mW
Storage temperature range	-65 C to +150 C
Lead temperature (soldering, 10 seconds)	+300 C
Data retention	10 years minimum
Endurance (write/erase cycles)	10,000 cycles minimum
A9 voltage for sector protect (V_{ID}) 3/	-2.0 V dc to +14.0 V dc

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input low voltage range (V_{IL})	-0.5 V dc to +0.8 V dc
Input high voltage range (V_{IH})	+2.0 V dc to V_{CC} + 0.3 V dc
Case operating temperature range (T_C)	-55 C to +125 C
A9 voltage for sector protect (V_{ID})	+11.5 V dc to +12.5 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. Unless otherwise specified, the following specification, standards, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

PERFORMANCE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of the specification, standards, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Minimum DC voltage in input or I/O pins is -0.5 V dc. During voltage transitions, inputs may overshoot V_{SS} to -2.0 V dc for periods up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} +0.5 V dc. During voltage transitions, outputs may overshoot to V_{CC} +2.0 V dc for periods up to 20 ns.
3/ Minimum DC input voltage on A9 is -0.5 V dc. During voltage transitions, A9 may overshoot V_{SS} to -2.0 V dc for periods up to 20 ns. Maximum DC input voltage on A9 is +13.5 V dc which may overshoot to +14.0 V dc for periods up to 20 ns.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38534 and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figures 4, 5 and 6.

3.2.5 Block diagram. The block diagram shall be as specified on figure 7.

3.2.6 Output load circuit. The output load circuit shall be as specified on figure 8.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Programming procedure. The programming procedure shall be as specified by the manufacturer and shall be available upon request.

3.6 Marking of Device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in QML-38534.

3.7 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.8 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance submitted to DSCC-VA shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38534 and the requirements herein.

3.9 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

3.10 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for the initial characterization and after any design process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase cycles listed in section 1.3 herein over the full military temperature range. The vendors procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity.

3.11 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which amy affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ -55 C T_A +125 C unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
DC parameters							
Input leakage current	I_{LI}	V_{CC} = 5.5 V dc, V_{IN} = GND to V_{CC}	1,2,3	All		10	A
Output leakage current	I_{LO}	V_{CC} = 5.5 V dc, V_{IN} = GND to V_{CC}	1,2,3	All		10	A
V_{CC} active current for read	I_{CC1}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}	1,2,3	All		35	mA
V_{CC} active current for program or erase 3/	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}	1,2,3	All		50	mA
V_{CC} standby current	I_{CC3}	V_{CC} = 5.5 Vdc, $\overline{CS}$ = V_{IH} f = 5 MHz	1,2,3	All		1.6	mA
Input low level 3/	V_{IL}		1,2,3	All		0.8	V
Input high level 3/	V_{IH}		1,2,3	All	2.0		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V dc, I_{OL} = 12.0mA	1,2,3	All		0.45	V
Output high voltage	V_{OH1}	V_{CC} = 4.5 V dc, I_{OH} = -2.5mA	1,2,3	All	0.85 x V_{CC}		V
	V_{OH2}	V_{CC} = 4.5 V dc, I_{OH} = -100 A	1,2,3	All	V_{CC} - 0.4 Vdc		V
Dynamic characteristics							
$\overline{OE}$ capacitance 3/	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25 C	4	All		15	pF
A0-16 capacitance 3/	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25 C	4	All		15	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ -55 C T_A +125 C unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Dynamic characteristics - continued.							
$\overline{CS}$ capacitance 3/	C_{CS}	V_{IN} = 0 V dc, f = 1.0 MHz, T_A = +25 C	4	All		15	pF
$\overline{WE}$ capacitance 3/	C_{WE}	V_{IN} = 0 V dc, f = 1.0 MHz, T_A = +25 C	4	All		15	pF
I/O0-I/O7 capacitance 3/	$C_{I/O}$	V_{IN} = 0 V dc, f = 1.0 MHz, T_A = +25 C	4	All		15	pF
Functional testing							
Functional tests		See 4.3.1c	7,8A,8B	All			
Read cycle AC timing characteristics							
Read cycle time 3/	t_{RC}	See figure 4	9,10,11	01 02 03 04 05	150 120 90 70 60		ns
Address access time	t_{ACC}	See figure 4	9,10,11	01 02 03 04 05		150 120 90 70 60	ns
Chip select access time	t_{CE}	See figure 4	9,10,11	01 02 03 04 05		150 120 90 70 60	ns
Output Enable to output valid	t_{OE}	See figure 4	9,10,11	01 02 03 04 05		55 50 40 35 30	ns
Chip select to output high Z 3/	t_{DF}	See figure 4	9,10,11	01 02 03 04,05		35 30 25 20	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ -55 C T_A +125 C unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Read cycle AC timing - continued.							
Output Enable to output high Z 3/	t_{DF}	See figure 4	9,10,11	01 02 03 04,05		35 30 25 20	ns
Output hold from address, $\overline{CS}$ or $\overline{OE}$ change, whichever is first 3/	t_{OH}	See figure 4	9,10,11	All	0		ns
Write cycle AC timing - Write/Erase/Program operations $\overline{WE}$ controlled.							
Write cycle time 3/	t_{WC}	See figure 5	9,10,11	01 02 03 04 05	150 120 90 70 60		ns
Chip select setup time	t_{CS}	See figure 5	9,10,11	All	0		ns
Write Enable pulse width	t_{WP}	See figure 5	9,10,11	01 02 03 04 05	50 50 45 35 30		ns
Address setup time	t_{AS}	See figure 5	9,10,11	All	0		ns
Data setup time	t_{DS}	See figure 5	9,10,11	01,02 03 04,05	50 45 30		ns
Data hold time	t_{DH}	See figure 5	9,10,11	All	0		ns
Address hold time	t_{AH}	See figure 5	9,10,11	01,02 03,04, 05	50 45		ns
Write enable pulse 3/ width high	t_{WPH}	See figure 5	9,10,11	All	20		ns
Read recovery 3/ before write	t_{GHWL}	See figure 5	9,10,11	All	0		ns

See footnotes at end of table.

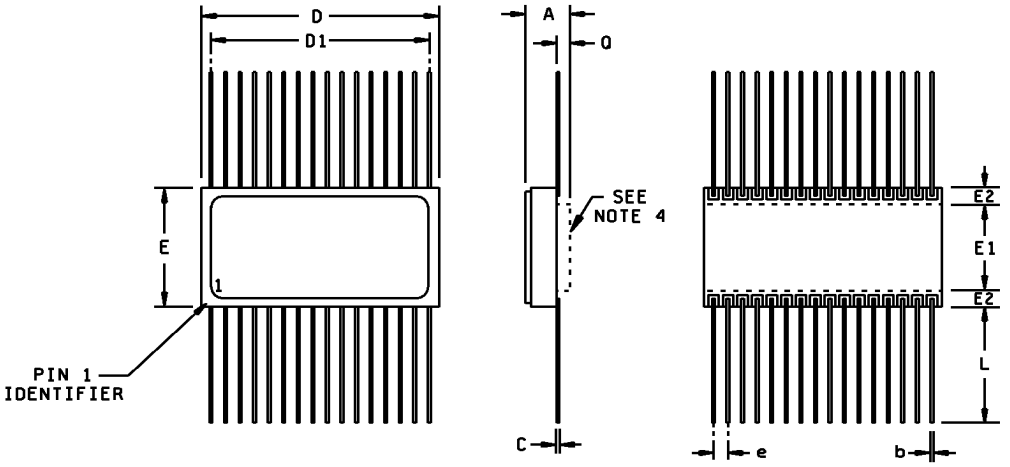
TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ -55 C T_A +125 C unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Write cycle AC timing - Write/Erase/Program operations $\overline{CS}$ controlled.							
Write cycle time 3/	t_{WC}	See figure 6	9,10,11	01 02 03 04 05	150 120 90 70 60		ns
Write Enable setup time	t_{WS}	See figure 6	9,10,11	All	0		ns
Address setup time	t_{AS}	See figure 6	9,10,11	All	0		ns
Data setup time	t_{DS}	See figure 6	9,10,11	01,02 03 04,05	50 45 30		ns
Data hold time	t_{DH}	See figure 6	9,10,11	All	0		ns
Address hold time	t_{AH}	See figure 6	9,10,11	01,02 03,04, 05	50 45		ns
Chip Select pulse width	t_{CP}	See figure 6	9,10,11	01,02 03 04 05	50 45 35 30		ns
Chip Select pulse width high 3/	t_{CPH}	See figure 6	9,10,11	All	20		ns
Read recovery before write 3/	t_{GHEL}	See figure 6	9,10,11	All	0		ns

1/ Unless otherwise specified, 4.5 V V_{CC} 5.5 V and V_{SS} = 0 V.
2/ Unless otherwise specified, the DC test conditions are as follows:
Input pulse levels: $V_{IH} = V_{CC}$ - 0.3 V and V_{IL} = 0.3 V.
Unless otherwise specified, the AC test conditions are as follows:
Input pulse levels: V_{IL} = 0 V and V_{IH} = 3.0 V.
Input rise and fall times: 5 nanoseconds.
Input and output timing reference levels: 1.5 V.

3/ Parameters shall be tested as part of device characterization and after design and process changes. Parameters shall be tested to the limits specified in table I for all lots not specifically tested.

Case outline T



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		3.18		.125
b	0.38	0.48	.015	.019
C	0.10	0.18	.004	.007
D	20.57	21.08	.810	.830
D1	18.92	19.18	.745	.755
E	10.29	10.41	.405	.415
E1	7.75	8.00	.305	.315
E2	1.27 TYP		.050 TYP	
e	1.27 TYP		.050 TYP	
L	9.65	10.67	.380	.420
Q	0.56	0.71	.022	.028

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. For solder lead finish, dimensions b and C will increase by +.003 inches (+0.08 mm).
3. Pin numbers are for reference only.
4. The case outline T is available in either a pedestal or non-pedestal package. The Q dimension only applies to the pedestal version of case outline T.

FIGURE 1. Case outline(s).

Case outline U

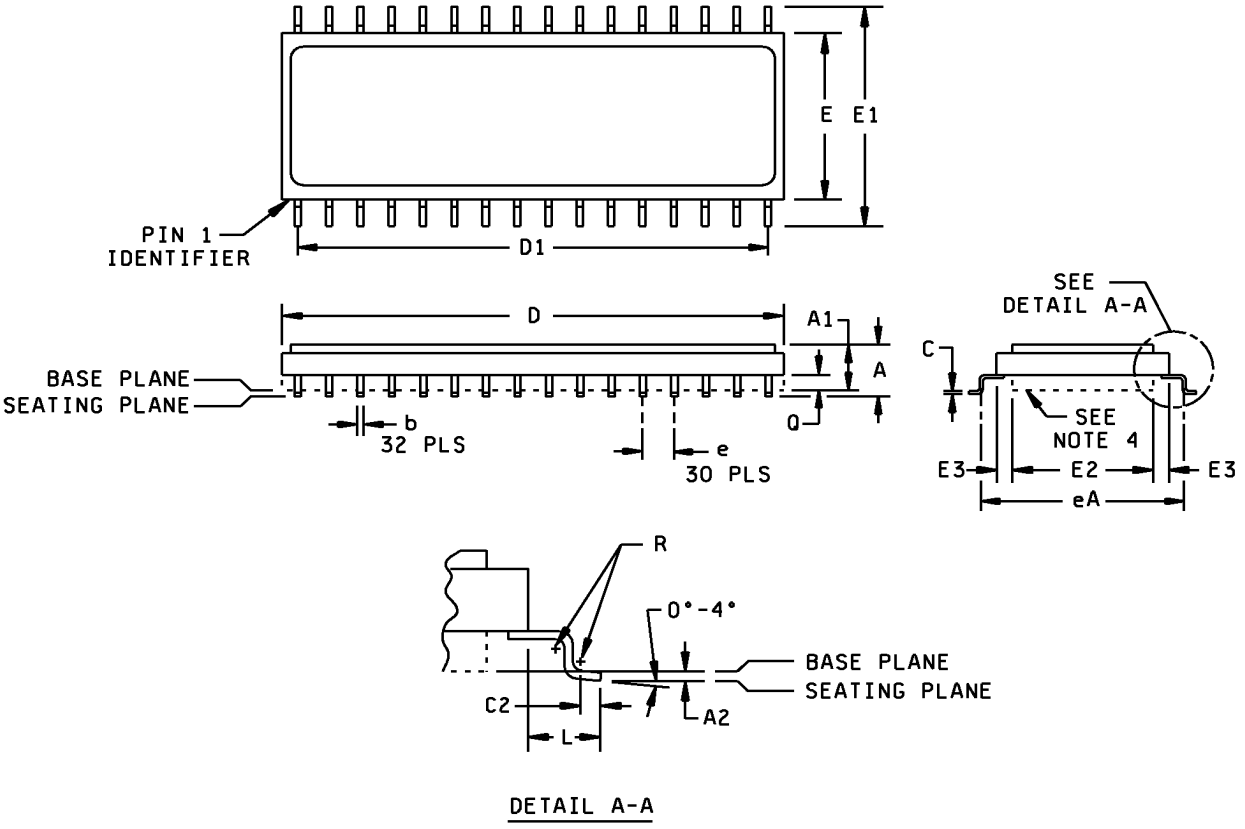


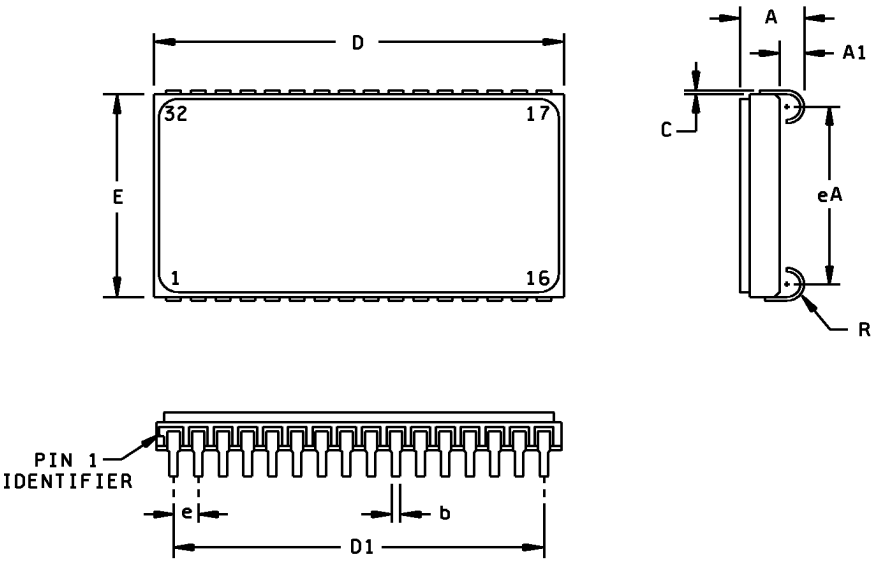
FIGURE 1. Case outline(s) - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		3.35		.132
A1	2.41	3.18	.095	.125
A2	0.08	0.18	.003	.007
b	0.38	0.48	.015	.019
C	0.10	0.18	.004	.007
C2	0.76 TYP		.030 TYP	
D	20.57	21.08	.810	.830
D1	19.05 TYP		.750 TYP	
E	10.29	10.54	.405	.415
E1	13.34	13.59	.525	.535
E2	7.75	8.00	.305	.315
E3	1.27 TYP		.050 TYP	
e	1.27 TYP		.050 TYP	
eA	11.07 TYP		.436 TYP	
L	1.52 TYP		.060 TYP	
Q	0.56	0.71	.022	.028
R	0.18 TYP		.007 TYP	

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. For solder lead finish, dimensions b and C will increase by +.003 inches (+0.08 mm).
3. Pin numbers are for reference only.
4. The case outline U is available in either a pedestal or non-pedestal package. The Q dimension only applies to the pedestal version of case outline U.

FIGURE 1. Case outline(s) - Continued.

Case outline X

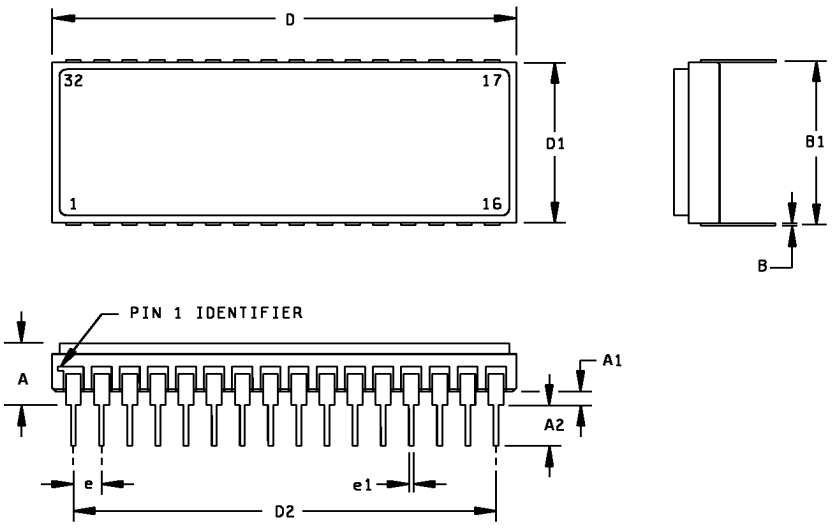


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.70	3.70	.106	.156
A1	1.02	1.52	.040	.060
b	0.38	0.48	.015	.019
C	0.15	0.25	.006	.010
D	20.83	21.34	.820	.840
D1	18.92	19.18	.745	.755
E	10.80	11.05	.425	.435
e	1.27 TYP		.050 TYP	
eA	9.30	9.80	.366	.386
R	0.89 TYP		.035 TYP	

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. For solder lead finish, dimensions b and C will increase by +.003 inches (+0.08 mm).

FIGURE 1. Case outline(s) - continued.

Case outline Y



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.56	5.13	.140	.202
A1	0.48	1.19	.019	.047
A2	3.18	4.90	.125	.193
B	0.23	0.30	.009	.012
B1	14.99	15.49	.590	.610
D	42.01	42.82	1.654	1.686
D1	14.73	15.34	.580	.604
D2	37.90	38.30	1.492	1.508
e	2.41	2.67	.095	.105
e1	0.41	0.51	.016	.020

NOTES:
1. The U.S preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. For solder lead finish, dimensions B and e1 will increase by +.003 inches (+0.08mm).
3. Pin numbers are for reference only.

Figure 1. Case outline(s) - continued.

Device types	All	Device types	All
Case outline	All	Case outline	All
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	17	I/O3
2	A16	18	I/O4
3	A15	19	I/O5
4	A12	20	I/O6
5	A7	21	I/O7
6	A6	22	$\overline{CS}$
7	A5	23	A10
8	A4	24	$\overline{OE}$
9	A3	25	A11
10	A2	26	A9
11	A1	27	A8
12	A0	28	A13
13	I/O0	29	A14
14	I/O1	30	NC
15	I/O2	31	$\overline{WE}$
16	V_{SS}	32	V_{CC}

FIGURE 2. Terminal connections.

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Device Current
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	L	WrIte	Data In	Active

Notes:
1. H = V_{IH} = High Logic Level
2. L = V_{IL} = Low Logic Level
3. X = Do not care (either high or low)
4. High Z = High Impedance state

FIGURE 3. Truth table.

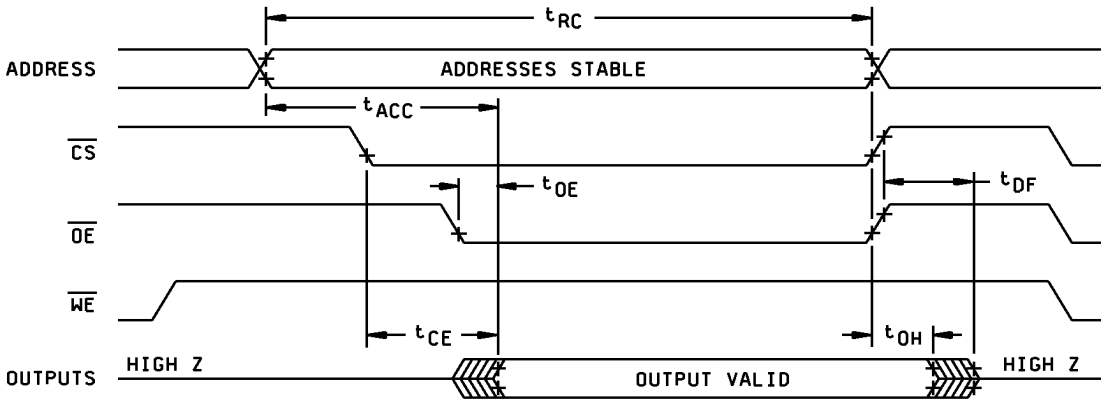


FIGURE 4. Read cycle timing diagram.

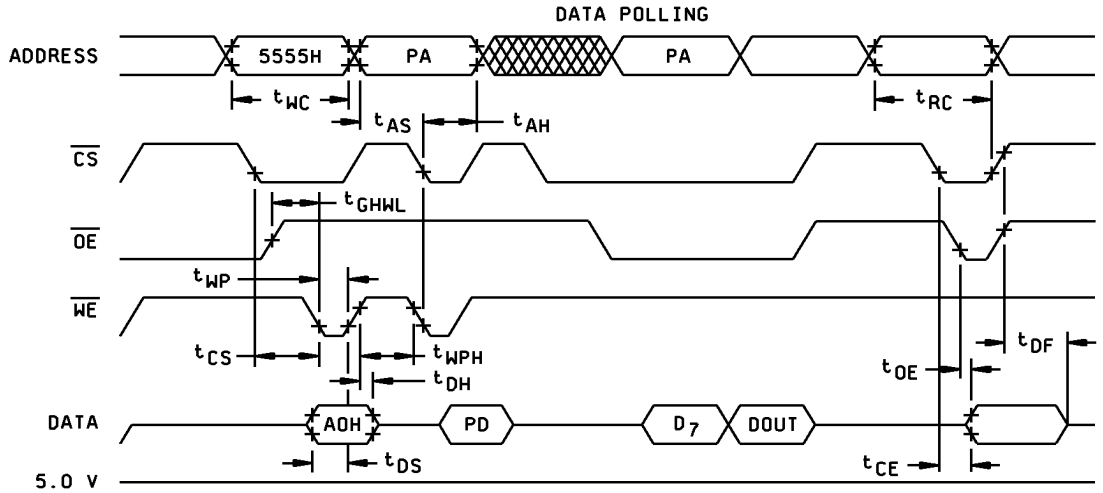
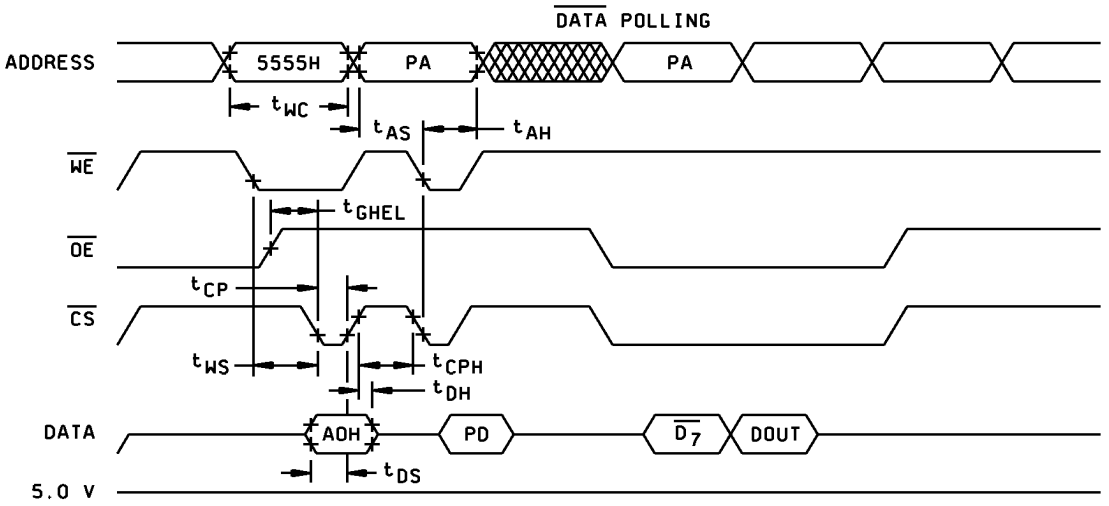


FIGURE 5. Write/Erase/Program operations, $\overline{WE}$ controlled.



Notes:
1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7 is the output of the complement of the data written to the device
4. D_{OUT} is the output of the data written to the device.
5. Figures indicate the last two bus cycles of a four bus cycle sequence.

FIGURE 6. Write/Erase operations, $\overline{CS}$ controlled.

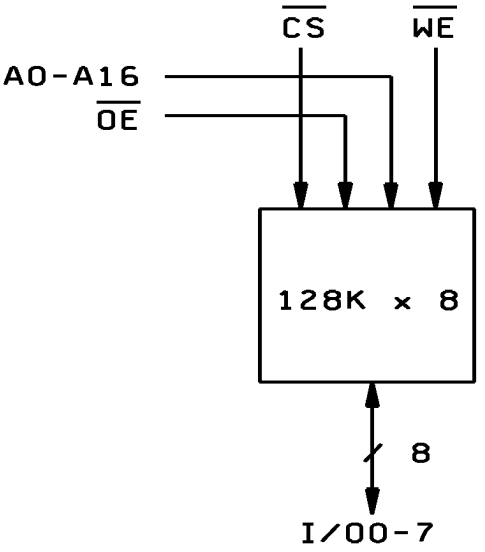


FIGURE 7. Block diagram.

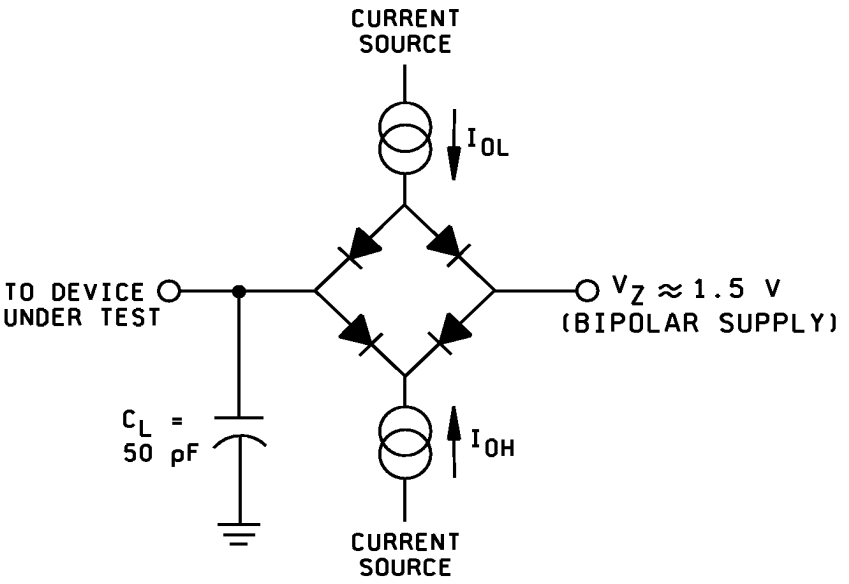


FIGURE 8. Typical output test circuit.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table
Interim electrical parameters	1,4,7,9
Final electrical test parameters	1*,2,3,4,7,8A,8B,9,10, 11
Group A test requirements	1,2,3,4,7,8A,8B,9,10 11
Group C end-point electrical parameters	1,2,3,4,7,8A,8B,9,10 11
MIL-STD-883, group E end-point electrical parameters for RHA devices	Subgroups ** (in accordance with method 5005, group A test table)

* PDA applies to subgroup 1.
** When applicable to this standard microcircuit drawing, the subgroups shall be defined.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection(CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table on figure 3.

4.3.2 Group B inspection(PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection(PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection(PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes H and K shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes H and K for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table II herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

d. For device classes H and K, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25 C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0526.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 99-03-29

Approved sources of supply for SMD 5962-96690 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9669001HTA	54230	WMF128K8-150FEQ5
5962-9669001HTC	54230	WMF128K8-150FEQ5
5962-9669001HUA	54230	WMF128K8-150FFQ5
5962-9669001HUC	54230	WMF128K8-150FFQ5
5962-9669001HXA	54230	WMF128K8-150DEQ5
5962-9669001HXC	54230	WMF128K8-150DEQ5
5962-9669001HYA	54230	WMF128K8-150CQ5
5962-9669001HYA	88379	ACT-F128K8N-150P4Q
5962-9669001HYC	54230	WMF128K8-150CQ5
5962-9669001HYC	88379	ACT-F128K8N-150P4Q
5962-9669002HTA	54230	WMF128K8-120FEQ5
5962-9669002HTC	54230	WMF128K8-120FEQ5
5962-9669002HUA	54230	WMF128K8-120FFQ5
5962-9669002HUC	54230	WMF128K8-120FFQ5
5962-9669002HXA	54230	WMF128K8-120DEQ5
5962-9669002HXC	54230	WMF128K8-120DEQ5
5962-9669002HYA	54230	WMF128K8-120CQ5
5962-9669002HYA	88379	ACT-F128K8N-120P4Q
5962-9669002HYC	54230	WMF128K8-120CQ5
5962-9669002HYC	88379	ACT-F128K8N-120P4Q
5962-9669003HTA	54230	WMF128K8-90FEQ5
5962-9669003HTC	54230	WMF128K8-90FEQ5
5962-9669003HUA	54230	WMF128K8-90FFQ5
5962-9669003HUC	54230	WMF128K8-90FFQ5
5962-9669003HXA	54230	WMF128K8-90DEQ5
5962-9669003HXC	54230	WMF128K8-90DEQ5
5962-9669003HYA	54230	WMF128K8-90CQ5
5962-9669003HYA	88379	ACT-F128K8N-090P4Q
5962-9669003HYC	54230	WMF128K8-90CQ5
5962-9669003HYC	88379	ACT-F128K8N-090P4Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

DATE: 99-03-29

Approved sources of supply for SMD 5962-96690 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9669004HTA	54230	WMF128K8-70FEQ5
5962-9669004HTC	54230	WMF128K8-70FEQ5
5962-9669004HUA	54230	WMF128K8-70FFQ5
5962-9669004HUC	54230	WMF128K8-70FFQ5
5962-9669004HXA	54230	WMF128K8-70DEQ5
5962-9669004HXC	54230	WMF128K8-70DEQ5
5962-9669004HYA	54230	WMF128K8-70CQ5
5962-9669004HYA	88379	ACT-F128K8N-070P4Q
5962-9669004HYC	54230	WMF128K8-70CQ5
5962-9669004HYC	88379	ACT-F128K8N-070P4Q
5962-9669005HTA	54230	WMF128K8-60FEQ5
5962-9669005HTC	54230	WMF128K8-60FEQ5
5962-9669005HUA	54230	WMF128K8-60FFQ5
5962-9669005HUC	54230	WMF128K8-60FFQ5
5962-9669005HXA	54230	WMF128K8-60DEQ5
5962-9669005HXC	54230	WMF128K8-60DEQ5
5962-9669005HYA	54230	WMF128K8-60CQ5
5962-9669005HYA	88379	ACT-F128K8N-060P4Q
5962-9669005HYC	54230	WMF128K8-60CQ5
5962-9669005HYC	88379	ACT-F128K8N-060P4Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
54230	White Electronic Designs Corporation 3601 East University Drive Phoenix, AZ 85034
88379	Aeroflex Circuit Technology 35 South Service Road Painview, NY 11803

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.