



## QUICKSD™ ESP FAMILY

### PROGRAMMABLE HIGH-SPEED SERIAL INTERFACE DEVICES



#### QUICKSD FAMILY HIGHLIGHTS

- **High Performance** — Delivers up to 8 Gb/s serial data throughput rates
- **Complete Serial Communications Solution:**
  - Multiple Bus LVDS Serial Links
  - Integrated Programmable Fabric
  - Embedded Dual-Port SRAM
  - Programmable "Back-End" I/Os
- **Flexible:**
  - Serial-to-parallel/parallel-to-serial conversion rates from 1:1 to 1:20
  - Embedded or separately transmitted clocks
  - Point-to-point, multi-point, multi-drop support

The QuickSD™ family of Bus LVDS SERDES Embedded Standard Products (ESPs) is the first complete solution for developing customized high-speed serial communications applications. QuickSD devices integrate multi-channel serial communications links with clock/data recovery, embedded memory, multiply/accumulate blocks, customizable logic, and programmable I/Os.

The embedded portion of the device contains high-performance, Bus LVDS transceivers that deliver up to 8 Gb/s serial data transfer rate for fast chip-to-chip, board-to-board and box-to-box communications. The customizable portion of the device consists of 658,000 system gates of programmable logic and 83,000 bits of dual-port SRAM.

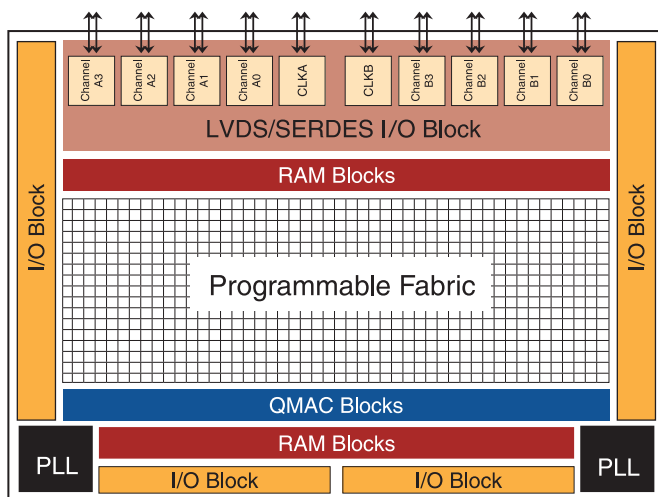
#### QUICKSD FAMILY FEATURES

Device	SERDES Data Channels	LVDS Clock Channel	Programmable Fabric Flip-Flops	Packages	Temp. Grade	Supply Voltage
QL81SD	6	2	1,920	208-PQFP, 280-FPBGA, 484-PBGA	C, I	2.5V
QL82SD	8	2	4,032	208-PQFP, 280-FPBGA, 484-PBGA, 516-PBGA	C, I	2.5V
QL84SD	8	2	8,064	280-FPBGA, 484-PBGA, 516-PBGA, 672-PBGA	C, I	2.5V

QuickSD devices are designed to support both transmit and receive requirements in a single chip, thereby providing multiple-channel support in a variety of modes and translation widths. This makes the devices ideal for applications where performance is critical and customization is required. Examples include 3G wireless base stations, telecom switches, Internet routers, and video transmission systems.

### HIGHEST PERFORMANCE

The largest QuickSD devices include eight serial data channels, each operating at up to 1 Gb/s for a total bandwidth of 8 Gb/s on the high-speed serial data channels alone. Each channel can be configured to provide various serial-to-parallel (or parallel-to-serial)



QuickSD Family Block Diagram

compression rates, including 1:1, 1:4, 1:7, 1:8 with an external clock and 1:10 and 1:20 with an embedded clock. This "back-end" flexibility allows the programmable fabric and embedded memory to easily implement a wide range of communication standards and other functions including Utopia II, Utopia III, Utopia IV, ATM and SONET framers, PCI interfaces, SDRAM controllers and network processor interfaces.

### COMPLETE SERIAL SYSTEM SOLUTION

- **Embedded Bus LVDS Serial Links** — Up to 8 independent serial transceivers with integrated SERDES, 2 independent clock/data serial transceivers, integrated clock & data recovery (CDR) with bypass option
- **Programmable Fabric** — Over 8,000 flip-flops in user-customizable logic cells
- **Dual-Port SRAM** — 83k bits, configurable as RAMs, ROMs or FIFOs
- **Programmable "Back-End" I/Os** — LVTTTL, LVCMOS, PCI, GTL+, SSTL2, SSTL3, LVDS, LVPECL

### REFERENCE DEVELOPMENT KIT

The QuickSD family's Reference Development Kit (RDK) allows system engineers to test their design in hardware while developing their system logic and software, significantly reducing overall development time.

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