CYM1423

CYPRESS SEMICONDUCTOR

128K x 8 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 45 ns**
- **32-pin, 0.6-inch-wide DIP package**
- **JEDEC-compatible pinout**
- **Low active power**
  - **1.2W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Commercial temperature range**
- **Small PCB footprint**
  - **1.1 sq. in.**

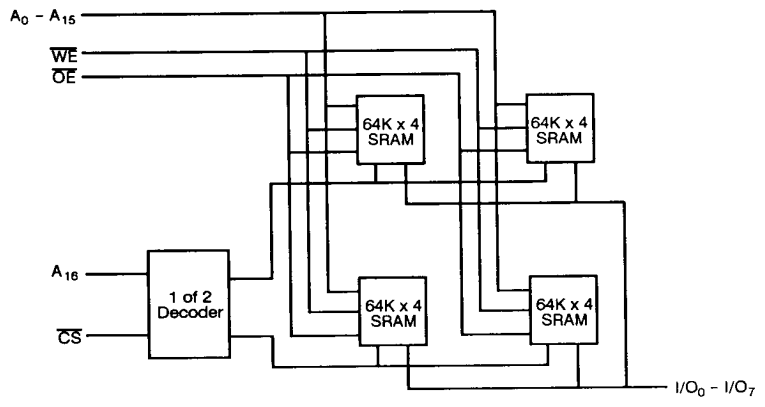
Functional Description

The CYM1423 is a high-performance 1-megabit static RAM module organized as 128K words by 8 bits. This module is constructed using four 64K x 4 static RAMs in SOJ packages mounted onto an epoxy laminate board with pins. A decoder is used to interpret the higher-order address and select two of the four RAMs.

Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{16}). Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{16}) will appear on the eight input/output pins (I/O_0 through I/O_7).

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



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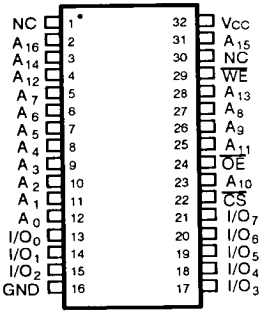
Pin Configuration

DIP
Top View



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Selection Guide

	1423PD-45	1423PD-55	1423PD-70
Maximum Access Time (ns)	45	55	70
Maximum Operating Current (mA)	210	210	210
Maximum Standby Current (mA)	80	80	80

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... -45°C to +150°C

Ambient Temperature with Power Applied ..... -10°C to +85°C

Supply Voltage to Ground Potential ..... -0.3V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... -0.3V to +7.0V

DC Input Voltage ..... -0.3V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1423PD		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		-0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	-10	+ 10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	-10	+ 10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		210	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		80	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V		80	mA

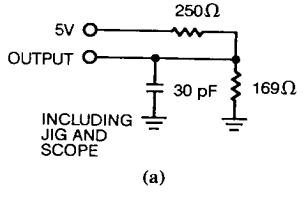
Capacitance[1]

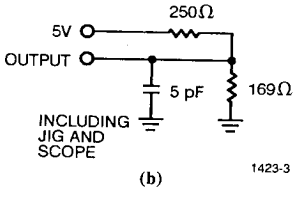
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		25	pF

Note:

1. Tested on a sample basis.

AC Test Loads and Waveforms





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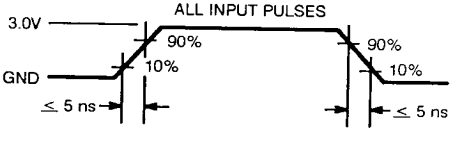

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Switching Characteristics Over the Operating Range [2]

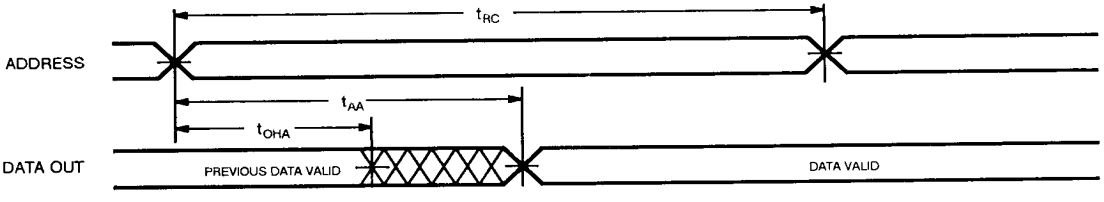
Parameters	Description	1423PD-45		1423PD-55		1423PD-70		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	45		55		70		ns
t_{AA}	Address to Data Valid		45		55		70	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		45		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		20		30		35	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z	5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		20		25		30	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[3]		20		25		30	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	45		55		70		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	40		45		60		ns
t_{AW}	Address Set-Up to Write End	40		45		60		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up from Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		35		40		ns
t_{SD}	Data Set-Up to Write End	35		35		40		ns
t_{HD}	Data Hold from Write End	2		2		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[3]	0	15	0	25	0	30	ns

Notes:

2. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
3. t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. $\overline{WE}$ is HIGH for read cycle.
6. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
7. Address valid prior to or coincident with $\overline{CS}$ transition low.
8. Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

Read Cycle No. 1 [5, 6]



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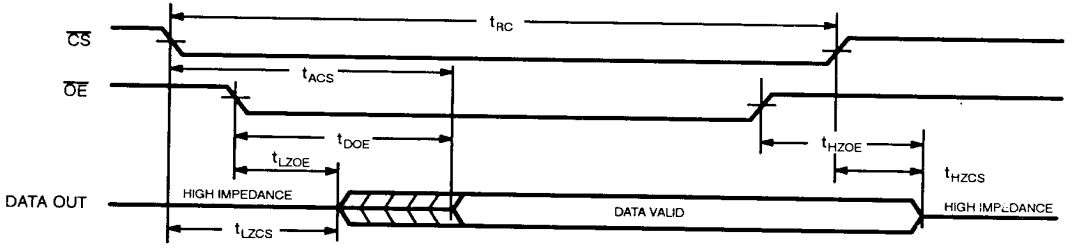
Switching Waveforms (continued)

Read Cycle No. 2 [5, 7]



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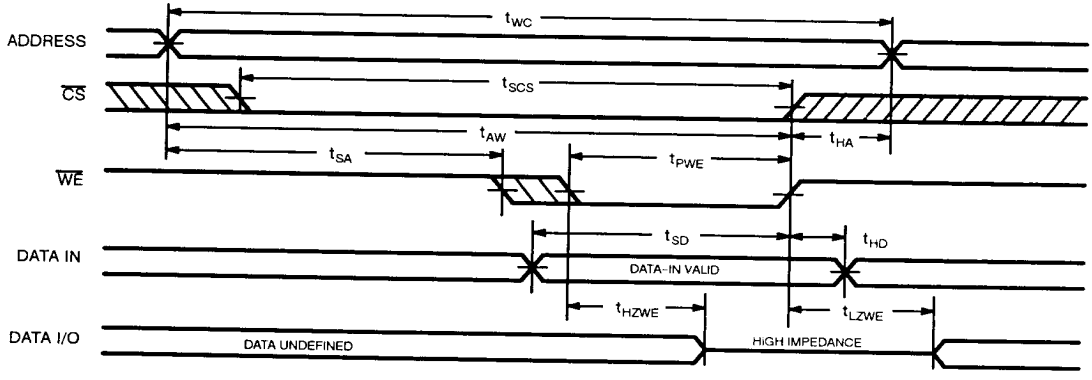
Write Cycle No. 1 ($\overline{WE}$ Controlled) [4, 8]



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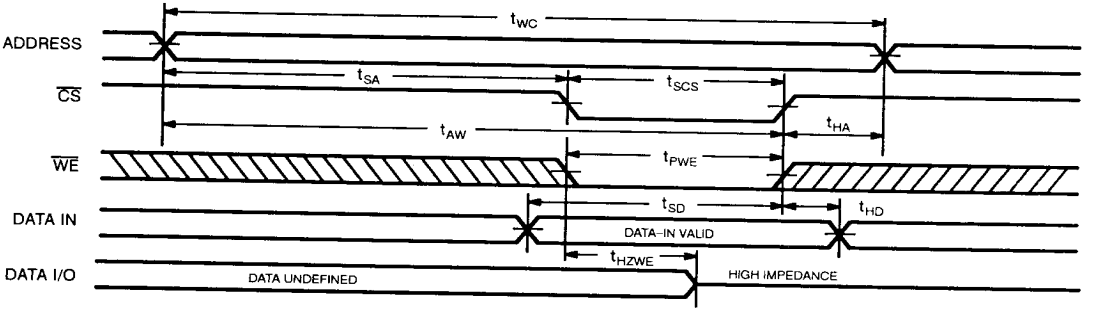
Write Cycle No. 2 ($\overline{CS}$ Controlled) [4, 8, 9]



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Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
45	CYM1423PD-45C	PD01	Commercial
55	CYM1423PD-55C	PD01	Commercial
70	CYM1423PD-70C	PD01	Commercial

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