

T-52-31



Advanced  
Micro  
Devices

# Am29833A/Am29853A

## Parity Bus Transceivers

### DISTINCTIVE CHARACTERISTICS

- High-speed bidirectional bus transceivers for processor organized devices
  - T-R delay = 6 ns typical
  - R-Parity delay = 9 ns typical
- Error flag with open-collector output
- Generates odd parity for all-zero protection
- 200 mV minimum input hysteresis (Commercial) on input data ports
- High drive capability:
  - 48 mA Commercial IOL
- Higher speed, lower power versions of the Am29833 & Am29853

### GENERAL DESCRIPTION

The Am29833A and Am29853A are high-performance parity bus transceivers designed for two-way communications. Each device can be used as an 8-bit transceiver, as well as a 9-bit parity checker/generator. In the transmit mode, data is read at the R port and output at the T port with a parity bit. In the receive mode, data and parity are read at the T port, and the data is output at the R port along with an  $\overline{\text{ERR}}$  flag showing the result of the parity test.

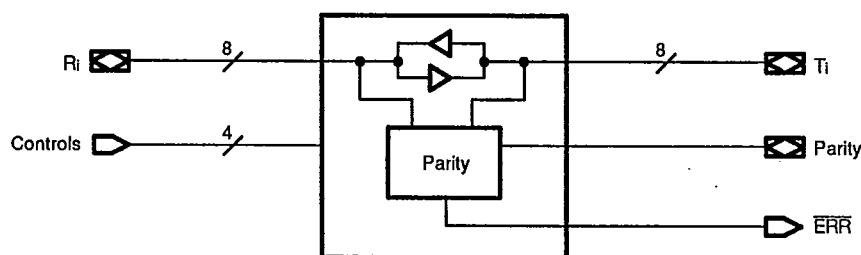
In the Am29833A, the error flag is clocked and stored in a register which is read at the open-collector  $\overline{\text{ERR}}$  output. The  $\overline{\text{CLR}}$  input is used to clear the error flag register. In the Am29853A, a latch replaces this register, and the  $\overline{\text{EN}}$  and  $\overline{\text{CLR}}$  controls are used to pass, store, sample or clear the error flag output. When both output enables

are disabled in the Am29853A and Am29833A, the parity logic defaults to the transmit mode, so that the  $\overline{\text{ERR}}$  pin reflects the parity of the R port.

The output enables,  $\overline{\text{OER}}$  and  $\overline{\text{OET}}$ , are used to force the port outputs to the high-impedance state so that other devices can drive bus lines directly. In addition, the user can force a parity error by enabling both  $\overline{\text{OER}}$  and  $\overline{\text{OET}}$  simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability.

Each of these devices is produced with AMD's proprietary IMOX™ bipolar process, and features typical propagation delays of 6 ns, as well as high-capacitive drive capability.

### SIMPLIFIED BLOCK DIAGRAM

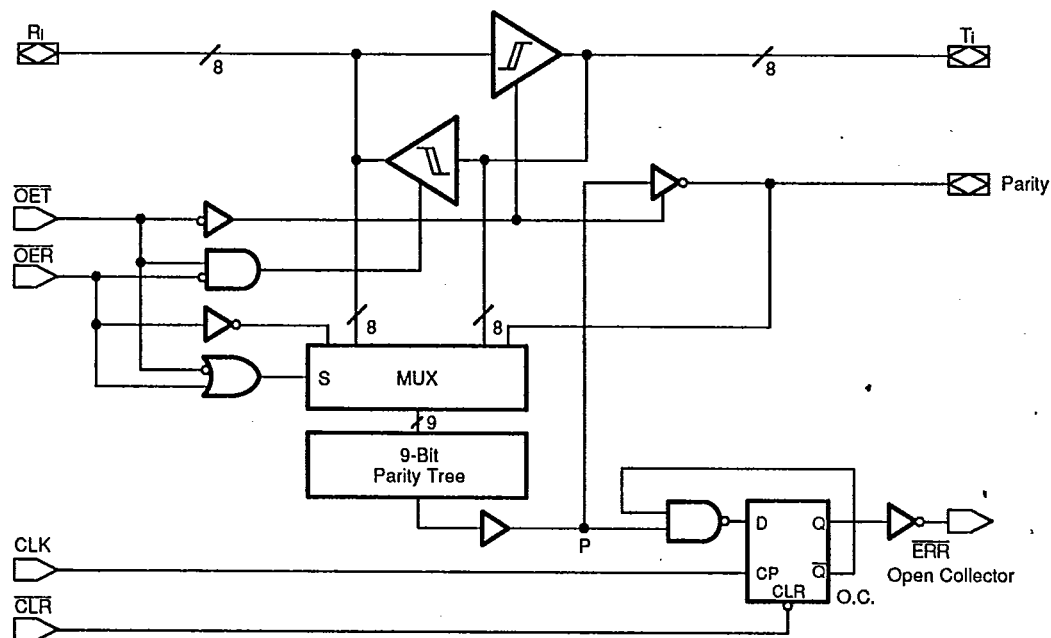


07140-001A

## BLOCK DIAGRAMS

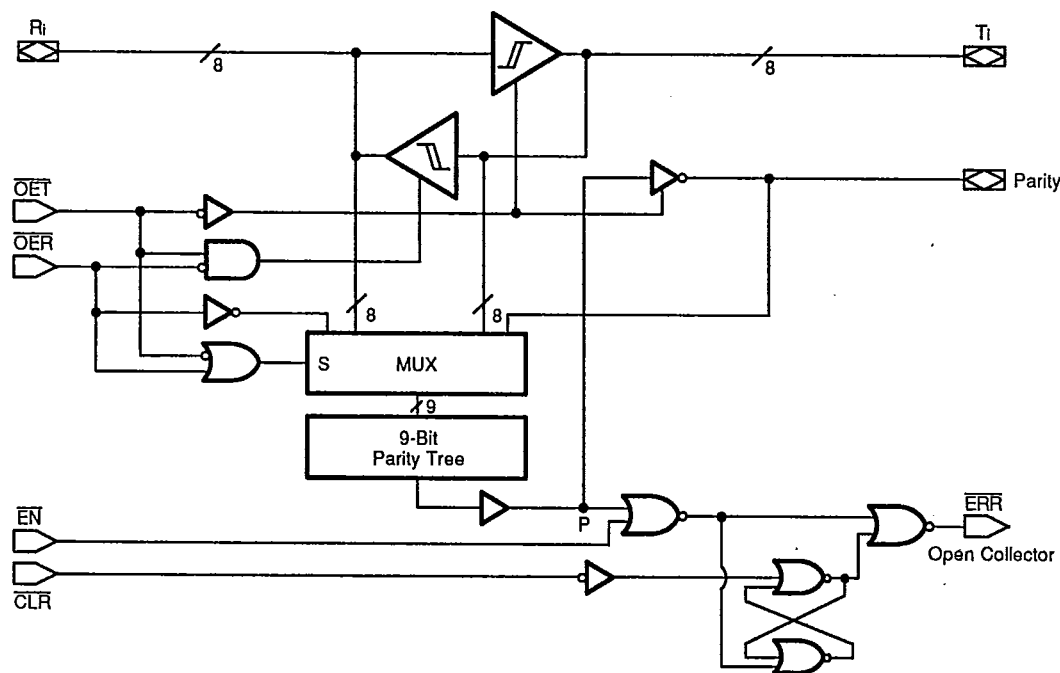
T-52-31

## Am29833A



07140-002A

## Am29853A

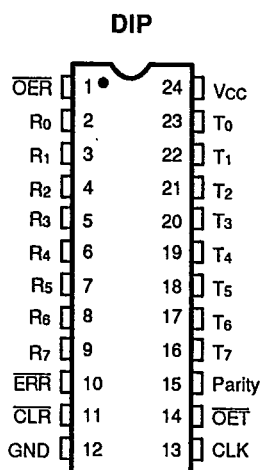


07140-003A

CONNECTION DIAGRAMS  
(Top View)

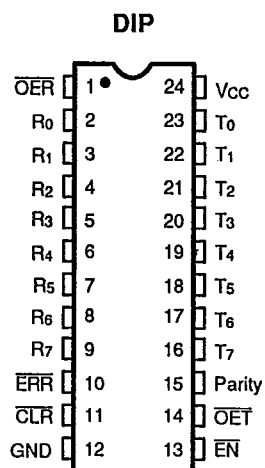
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Am29833A



07140-004A

Am29853A



07140-005A

**FUNCTION TABLE**  
**Am29833A (Register Option)**

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| Inputs           |                  |                  |     |                |                              |                |                                      | Outputs        |                |        |                  | Function                                                                                                                |
|------------------|------------------|------------------|-----|----------------|------------------------------|----------------|--------------------------------------|----------------|----------------|--------|------------------|-------------------------------------------------------------------------------------------------------------------------|
| $\overline{OET}$ | $\overline{OER}$ | $\overline{CLR}$ | CLK | R <sub>i</sub> | Sum of H's of R <sub>i</sub> | T <sub>i</sub> | Sum of H's (T <sub>i</sub> + Parity) | R <sub>i</sub> | T <sub>i</sub> | Parity | $\overline{ERR}$ |                                                                                                                         |
| L                | H                | X                | X   | H              | ODD                          | NA             | NA                                   | NA             | H              | L      | NA               | Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.                       |
| L                | H                | X                | X   | H              | EVEN                         | NA             | NA                                   | NA             | H              | H      | NA               |                                                                                                                         |
| L                | H                | X                | X   | L              | ODD                          | NA             | NA                                   | NA             | L              | L      | NA               |                                                                                                                         |
| L                | H                | X                | X   | L              | EVEN                         | NA             | NA                                   | NA             | L              | H      | NA               |                                                                                                                         |
| H                | L                | H                | ↑   | NA             | NA                           | H              | ODD                                  | H              | NA             | NA     | H                | Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled. |
| H                | L                | H                | ↑   | NA             | NA                           | H              | EVEN                                 | H              | NA             | NA     | L                |                                                                                                                         |
| H                | L                | H                | ↑   | NA             | NA                           | L              | ODD                                  | L              | NA             | NA     | H                |                                                                                                                         |
| H                | L                | H                | ↑   | NA             | NA                           | L              | EVEN                                 | L              | NA             | NA     | L                |                                                                                                                         |
| X                | X                | L                | X   | X              | X                            | X              | X                                    | X              | X              | X      | H                | Clear error flag register.                                                                                              |
| H                | H                | H                | X   | X              | X                            | X              | X                                    | Z              | Z              | Z      | *                | Both transmitting and receiving paths are disabled.                                                                     |
| H                | H                | L                | X   | X              | X                            | X              | X                                    | Z              | Z              | Z      | H                |                                                                                                                         |
| H                | H                | H                | ↑   | L              | ODD                          | X              | X                                    | Z              | Z              | Z      | H                | Parity logic defaults to transmit mode. Forced-error checking.                                                          |
| H                | H                | H                | ↑   | H              | EVEN                         | X              | X                                    | Z              | Z              | Z      | L                |                                                                                                                         |
| L                | L                | X                | X   | H              | ODD                          | NA             | NA                                   | NA             | H              | H      | NA               |                                                                                                                         |
| L                | L                | X                | X   | H              | EVEN                         | NA             | NA                                   | NA             | H              | L      | NA               |                                                                                                                         |
| L                | L                | X                | X   | L              | ODD                          | NA             | NA                                   | NA             | L              | H      | NA               |                                                                                                                         |
| L                | L                | X                | X   | L              | EVEN                         | NA             | NA                                   | NA             | L              | L      | NA               |                                                                                                                         |

H = HIGH

L = LOW

↑ = LOW-to-HIGH Transition

X = Don't Care

Z = High Impedance

NA = Not Applicable

\* = Store the State of the Last Receive Cycle

ODD = Odd Number

EVEN = Even Number

i = 0, 1, 2, 3, 4, 5, 6, 7

**FUNCTION TABLE**  
**Am29853A (Latch Option)**

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| Inputs           |                  |                  |                 |       |                     |       |                              | Outputs |       |        |                  | Function                                                                                                                   |
|------------------|------------------|------------------|-----------------|-------|---------------------|-------|------------------------------|---------|-------|--------|------------------|----------------------------------------------------------------------------------------------------------------------------|
| $\overline{OET}$ | $\overline{OER}$ | $\overline{CLR}$ | $\overline{EN}$ | $R_i$ | Sum of H's of $R_i$ | $T_i$ | Sum of H's ( $T_i$ + Parity) | $R_i$   | $T_i$ | Parity | $\overline{ERR}$ |                                                                                                                            |
| L                | H                | X                | X               | H     | ODD                 | NA    | NA                           | NA      | H     | L      | NA               | Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.                          |
| L                | H                | X                | X               | H     | EVEN                | NA    | NA                           | NA      | H     | H      | NA               |                                                                                                                            |
| L                | H                | X                | X               | L     | ODD                 | NA    | NA                           | NA      | L     | L      | NA               |                                                                                                                            |
| L                | H                | X                | X               | L     | EVEN                | NA    | NA                           | NA      | L     | H      | NA               |                                                                                                                            |
| H                | L                | L                | L               | NA    | NA                  | H     | ODD                          | H       | NA    | NA     | H                | Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.    |
| H                | L                | L                | L               | NA    | NA                  | H     | EVEN                         | H       | NA    | NA     | L                |                                                                                                                            |
| H                | L                | L                | L               | NA    | NA                  | L     | ODD                          | L       | NA    | NA     | H                |                                                                                                                            |
| H                | L                | L                | L               | NA    | NA                  | L     | EVEN                         | L       | NA    | NA     | L                |                                                                                                                            |
| H                | L                | H                | L               | NA    | NA                  | H     | ODD                          | H       | NA    | NA     | H                | Receive mode: transmits data from T port to R port, passes parity test resulting in error flag. Transmit path is disabled. |
| H                | L                | H                | L               | NA    | NA                  | H     | EVEN                         | H       | NA    | NA     | L                |                                                                                                                            |
| H                | L                | H                | L               | NA    | NA                  | L     | ODD                          | L       | NA    | NA     | H                |                                                                                                                            |
| H                | L                | H                | L               | NA    | NA                  | L     | EVEN                         | L       | NA    | NA     | L                |                                                                                                                            |
| H                | L                | H                | H               | NA    | NA                  | X     | X                            | X       | NA    | NA     | *                | Store the state of error flag latch.                                                                                       |
| X                | X                | L                | H               | X     | X                   | X     | X                            | X       | NA    | NA     | H                | Clear error flag latch.                                                                                                    |
| H                | H                | H                | H               | X     | X                   | X     | X                            | Z       | Z     | Z      | *                | Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.                                |
| H                | H                | L                | H               | X     | X                   | X     | X                            | Z       | Z     | Z      | H                |                                                                                                                            |
| H                | H                | X                | L               | L     | ODD                 | X     | X                            | Z       | Z     | Z      | H                |                                                                                                                            |
| H                | H                | X                | L               | H     | EVEN                | X     | X                            | Z       | Z     | Z      | L                |                                                                                                                            |
| L                | L                | X                | X               | H     | ODD                 | NA    | NA                           | NA      | H     | H      | NA               | Forced-error checking.                                                                                                     |
| L                | L                | X                | X               | H     | EVEN                | NA    | NA                           | NA      | H     | L      | NA               |                                                                                                                            |
| L                | L                | X                | X               | L     | ODD                 | NA    | NA                           | NA      | L     | H      | NA               |                                                                                                                            |
| L                | L                | X                | X               | L     | EVEN                | NA    | NA                           | NA      | L     | L      | NA               |                                                                                                                            |

H = HIGH

L = LOW

↑ = LOW-to-HIGH Transition

X = Don't Care

Z = High Impedance

NA = Not Applicable

\* = Store the State of the Last Receive Cycle

ODD = Odd Number

EVEN = Even Number

i = 0, 1, 2, 3, 4, 5, 6, 7

## TRUTH TABLES

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## Error Flag Output

## Am29833A

| Inputs |            | Internal to Device | Outputs Pre-state      | Output           | Function             |
|--------|------------|--------------------|------------------------|------------------|----------------------|
| CLR    | CLK        | Point "P"          | $\overline{ERR}_{n-1}$ | $\overline{ERR}$ |                      |
| H      | $\uparrow$ | H                  | H                      | H                | Sample (1's Capture) |
| H      | $\uparrow$ | X                  | L                      | L                |                      |
| H      | $\uparrow$ | L                  | X                      | L                |                      |
| L      | X          | X                  | X                      | H                | Clear                |

## Note:

 $\overline{OET}$  is HIGH and  $\overline{OER}$  is LOW.

## Am29853A

| Inputs |     | Internal to Device | Outputs Pre-state      | Output           | Function             |
|--------|-----|--------------------|------------------------|------------------|----------------------|
| EN     | CLR | Point "P"          | $\overline{ERR}_{n-1}$ | $\overline{ERR}$ |                      |
| L      | L   | L                  | X                      | L                | Pass                 |
| L      | L   | H                  | X                      | H                |                      |
| L      | H   | L                  | X                      | L                | Sample (1's Capture) |
| L      | H   | X                  | L                      | L                |                      |
| L      | H   | H                  | H                      | H                |                      |
| H      | L   | X                  | X                      | H                | Clear                |
| H      | H   | X                  | L                      | L                | Store                |
| H      | H   | X                  | H                      | H                |                      |

## Note:

 $\overline{OET}$  is HIGH and  $\overline{OER}$  is LOW.

## ORDERING INFORMATION

### Standard Products

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AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (If applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing

AM29833A  
AM29853A

P

C

e. OPTIONAL PROCESSING  
Blank = Standard processing

d. TEMPERATURE RANGE  
C = Commercial (0 to +70°C)

c. PACKAGE TYPE  
P = 24-Pin (300-mil) Plastic DIP (PD3024)

b. SPEED OPTION  
Not Applicable

a. DEVICE NUMBER/DESCRIPTION  
Am29833A  
Parity Transceiver, Register Option  
Am29853A  
Parity Transceiver, Latch Option

| Valid Combinations |    |
|--------------------|----|
| AM29833A           | PC |
| AM29853A           |    |

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## PIN DESCRIPTION

## Am29833A/Am29853A

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OER**Output Enable Receive (Input, Active LOW)**

When LOW in conjunction with  $\overline{\text{OET}}$  HIGH, the devices are in the Receive mode ( $R_i$  are outputs,  $T_i$  and Parity are inputs).

OET**Output Enable Transmit (Input, Active LOW)**

When LOW in conjunction with  $\overline{\text{OER}}$  HIGH, the devices are in the Transmit mode ( $R_i$  are inputs,  $T_i$  and Parity are outputs).

 $R_i$ **Receive Port (Input/Output, Three-State)**

$R_i$  are the 8-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

 $T_i$ **Transmit Port (Input/Output, Three-State)**

$T_i$  are the 8-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

**Parity****Parity Flag (Input/Output, Three-State)**

In the Transmit mode, the Parity signal is an active output used to generate odd parity. In the Receive mode, the  $T_i$  and Parity inputs are combined and checked for odd parity. When both output enables are HIGH, the Parity Flag is in the high impedance state. When both output enables are LOW, the Parity bit forces a parity error.

## Am29833A Only

ERR**Error Flag (Output, Open Collector)**

In the Receive mode, the parity of the  $T_i$  bits is calculated and compared to the Parity input.  $\overline{\text{ERR}}$  goes LOW when the comparison indicates a parity error.  $\overline{\text{ERR}}$  stays LOW until the register is cleared.

CLR**Clear (Input, Active LOW)**

When  $\overline{\text{CLR}}$  goes LOW, the Error Flag Register is cleared ( $\overline{\text{ERR}}$  goes HIGH).

**CLK****Clock (Input, Positive Edge-Triggered)**

This pin is the clock input for the Error Flag register.

## Am29853A Only

ERR**Error Flag (Output, Open Collector)**

In the Receive mode, the parity of the  $T_i$  bits is calculated and compared to the Parity input.  $\overline{\text{ERR}}$  goes LOW when the comparison indicates a parity error.  $\overline{\text{ERR}}$  stays LOW until the latch is cleared.

CLR**Clear (Input, Active LOW)**

When  $\overline{\text{CLR}}$  goes LOW, and  $\overline{\text{EN}}$  is HIGH, the Error Flag latch is cleared ( $\overline{\text{ERR}}$  goes HIGH).

EN**Latch Enable (Input, Active LOW)**

This pin is the latch enable for the Error Flag latch.



**ABSOLUTE MAXIMUM RATINGS**

|                                                     |                   |
|-----------------------------------------------------|-------------------|
| Storage Temperature                                 | -65°C to +150°C   |
| Ambient Temperature with Power Applied              | -55 to +125°C     |
| Supply Voltage to Ground Potential Continuous       | -0.5 V to +7.0 V  |
| DC Voltage Applied to Outputs For High Output State | -0.5 V to +5.5 V  |
| DC Input Voltage                                    | -1.5 V to +6.0 V  |
| DC Output Current, Into Outputs                     | 100 mA            |
| DC Input Current                                    | -30 mA to +5.0 mA |

**OPERATING RANGES****Commercial (C) Devices**

|                                       |                |
|---------------------------------------|----------------|
| Ambient Temperature (T <sub>A</sub> ) | 0 to +70°C     |
| Supply Voltage (V <sub>CC</sub> )     | +4.5 to +5.5 V |

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Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**DC CHARACTERISTICS over operating range unless otherwise specified**

| Parameter Symbol  | Parameter Description                                 | Test Conditions                                                                  |                                                                          | Min.       | Max.       | Unit |
|-------------------|-------------------------------------------------------|----------------------------------------------------------------------------------|--------------------------------------------------------------------------|------------|------------|------|
| V <sub>OH</sub>   | Output HIGH Voltage<br>Except (ERR)                   | V <sub>CC</sub> = 4.5 V,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | I <sub>OH</sub> = -15 mA<br>I <sub>OH</sub> = -24 mA                     | 2.4<br>2.0 |            | V    |
| V <sub>OL</sub>   | Output LOW Voltage                                    | V <sub>CC</sub> = 4.5 V,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | ERR I <sub>OL</sub> = 48 mA<br>All Other Outputs I <sub>OL</sub> = 48 mA |            | 0.5<br>0.5 | V    |
| V <sub>IH</sub>   | Input HIGH Voltage                                    | Guaranteed Input Logical HIGH Voltage for all inputs (Note 1)                    |                                                                          | 2.0        |            | V    |
| V <sub>IL</sub>   | Input LOW Voltage                                     | Guaranteed Input Logical LOW Voltage for all inputs (Note 1)                     |                                                                          |            | 0.8        | V    |
| V <sub>I</sub>    | Input Clamp Voltage                                   | V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA                                |                                                                          |            | -1.2       | V    |
| V <sub>HYST</sub> | Hysteresis for Inputs R <sub>i</sub> , T <sub>i</sub> |                                                                                  |                                                                          | 200        |            | mV   |
| I <sub>ZL</sub>   | I/O Port LOW Current                                  | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V                                 |                                                                          |            | -550       | μA   |
| I <sub>IL</sub>   | Input LOW Current                                     | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V                                 |                                                                          |            | -0.5       | mA   |
| I <sub>IH</sub>   | Input HIGH Current                                    | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V                                 |                                                                          |            | 50         | μA   |
| I <sub>I</sub>    | Input HIGH Current                                    | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V                                 |                                                                          |            | 100        | μA   |
| I <sub>ZH</sub>   | I/O Port HIGH Current                                 | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V                                 |                                                                          |            | 100        | μA   |
| I <sub>ZI</sub>   | I/O Port HIGH Current                                 | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V                                 |                                                                          |            | 150        | μA   |
| I <sub>SC</sub>   | Output Short-Circuit Current                          | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V (Note 2)                           |                                                                          | -75        | -250       | mA   |
| I <sub>OFF</sub>  | Bus Leakage Current                                   | V <sub>CC</sub> = 0 V, V <sub>O</sub> = 2.9 V                                    |                                                                          |            | 100        | μA   |
| I <sub>CC</sub>   | Power Supply Current                                  | V <sub>CC</sub> = 5.5 V                                                          | Outputs LOW                                                              |            | 180        | mA   |
|                   |                                                       | Outputs Loaded                                                                   | Outputs HIGH                                                             |            | 155        |      |
|                   |                                                       |                                                                                  | Outputs Hi-Z                                                             |            | 170        |      |

**Notes:**

1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.
2. Not more than one output shorted at a time. Duration of the short-circuit test should not exceed one second.

## SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified T-52-31

| Parameter Symbol | Parameter Description                                                                                                                   |      | Test Conditions*                       | Min. | Max. | Unit |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------|------|----------------------------------------|------|------|------|
| tPLH             | Propagation Delay to Ri to Ti,                                                                                                          |      | CL = 50 pF<br>R1 = 500 Ω<br>R2 = 500 Ω |      | 10   | ns   |
| tPHL             | Ti to Ri                                                                                                                                |      |                                        |      | 10   | ns   |
| tPLH             | Propagation Delay Ri to Parity                                                                                                          |      |                                        |      | 15   | ns   |
| tPHL             |                                                                                                                                         |      |                                        |      | 15   | ns   |
| tZH              | Output Enable Time $\overline{OER}$ , $\overline{OET}$ to Ri, Ti and Parity                                                             |      |                                        | 12   |      | ns   |
| tZL              |                                                                                                                                         |      |                                        |      | 12   | ns   |
| tHZ              | Output Disable Time $\overline{OER}$ , $\overline{OET}$ to Ri, Ti and Parity                                                            |      |                                        | 12   |      | ns   |
| tLZ              |                                                                                                                                         |      |                                        |      | 12   | ns   |
| ts               | Ti, Parity to CLK Setup Time (Note 1)                                                                                                   |      |                                        | 12   |      | ns   |
| tH               | Ti, Parity to CLK Hold Time (Note 1)                                                                                                    |      |                                        | 0    |      | ns   |
| tREC             | Clear ( $\overline{CLR}$  ) to CLK Setup Time (Note 2) |      |                                        | 15   |      | ns   |
| tPWH             | Clock Pulse Width (Note 1)                                                                                                              | HIGH |                                        | 7    |      | ns   |
| tPWL             |                                                                                                                                         | LOW  |                                        | 7    |      | ns   |
| tPWL             | Clear Pulse Width                                                                                                                       | LOW  |                                        | 7    |      | ns   |
| tPHL             | Propagation Delay CLK to $\overline{ERR}$ (Note 1)                                                                                      |      |                                        |      | 12   | ns   |
| tPLH             | Propagation Delay $\overline{CLR}$ to $\overline{ERR}$                                                                                  |      |                                        |      | 16   | ns   |
| tPLH             | Propagation Delay Ti, Parity to $\overline{ERR}$                                                                                        |      |                                        |      | 22   | ns   |
| tPHL             | (PASS Mode Only) Am29853A                                                                                                               |      |                                        |      | 18   | ns   |
| tPLH             | Propagation Delay $\overline{OER}$ to Parity                                                                                            |      |                                        |      | 15   | ns   |
| tPHL             |                                                                                                                                         |      |                                        |      | 15   | ns   |

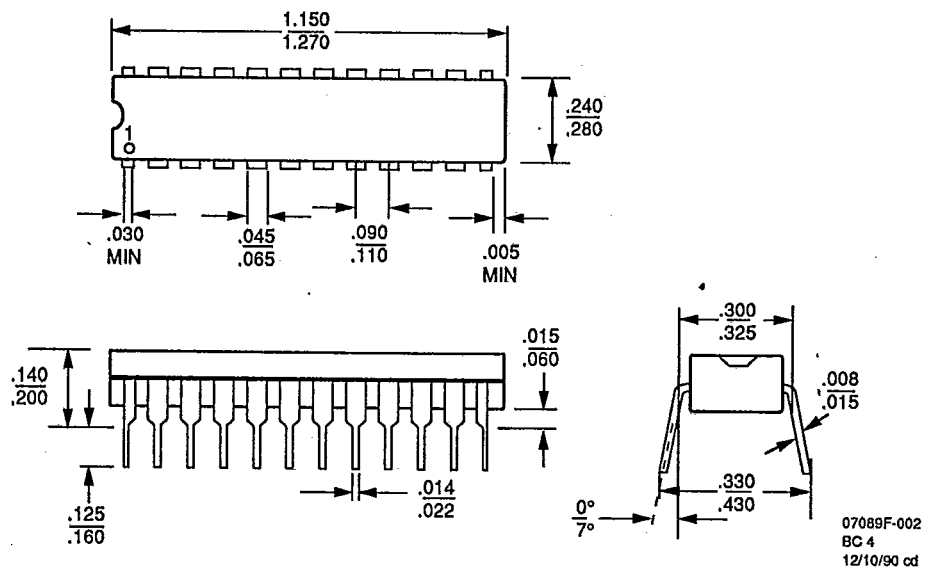
\*See test circuit and waveforms (Chapter 2).

**Notes:**

1. For Am29853A, replace CLK with  $\overline{EN}$ .
2. Not applicable to Am29853A.

**PD3024****24-Pin 300-mil Plastic SKINNYDIP**

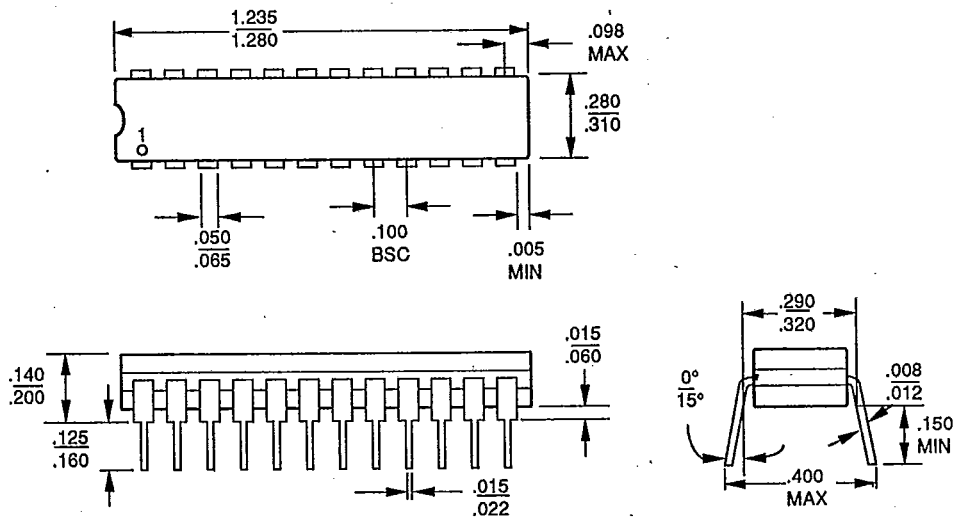
T-90-20

**Note:**

For reference only. All dimensions measured in inches. BSC is an ANSI standard for Basic Space Centering.

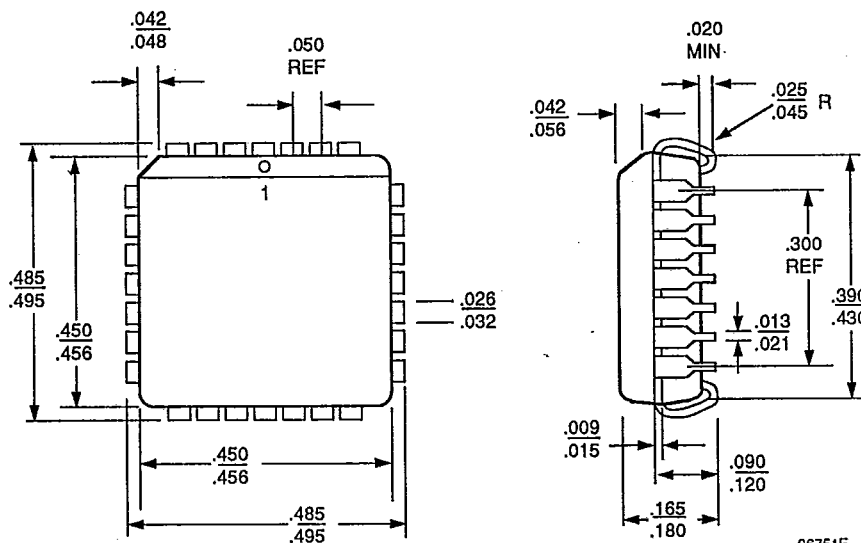
T-90-20

**CD3024**  
**24-Pin 300-mil Ceramic SKINNYDIP**



06850C

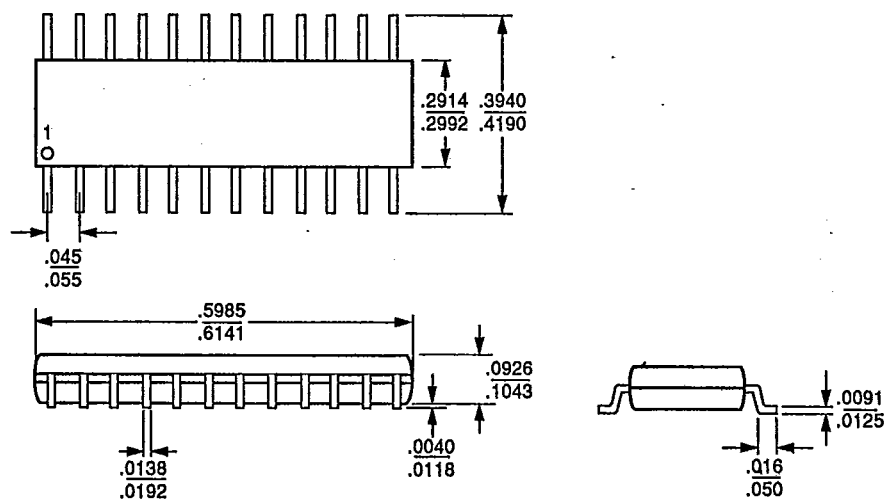
**PL 028**  
**28-Pin Plastic Leaded Chip Carrier**



06751E

**SO 024**  
**24-Pin Plastic Small Outline Package**

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09310B