Document Title

LCD Controller-Driver

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	March 13, 2000	Preliminary
0.1	Error correction: Pad assignment & Boot capacitor connection: C1+ → C1- C1- → C1+ C2+ → C2- C2- → C2+	December 7, 2000	

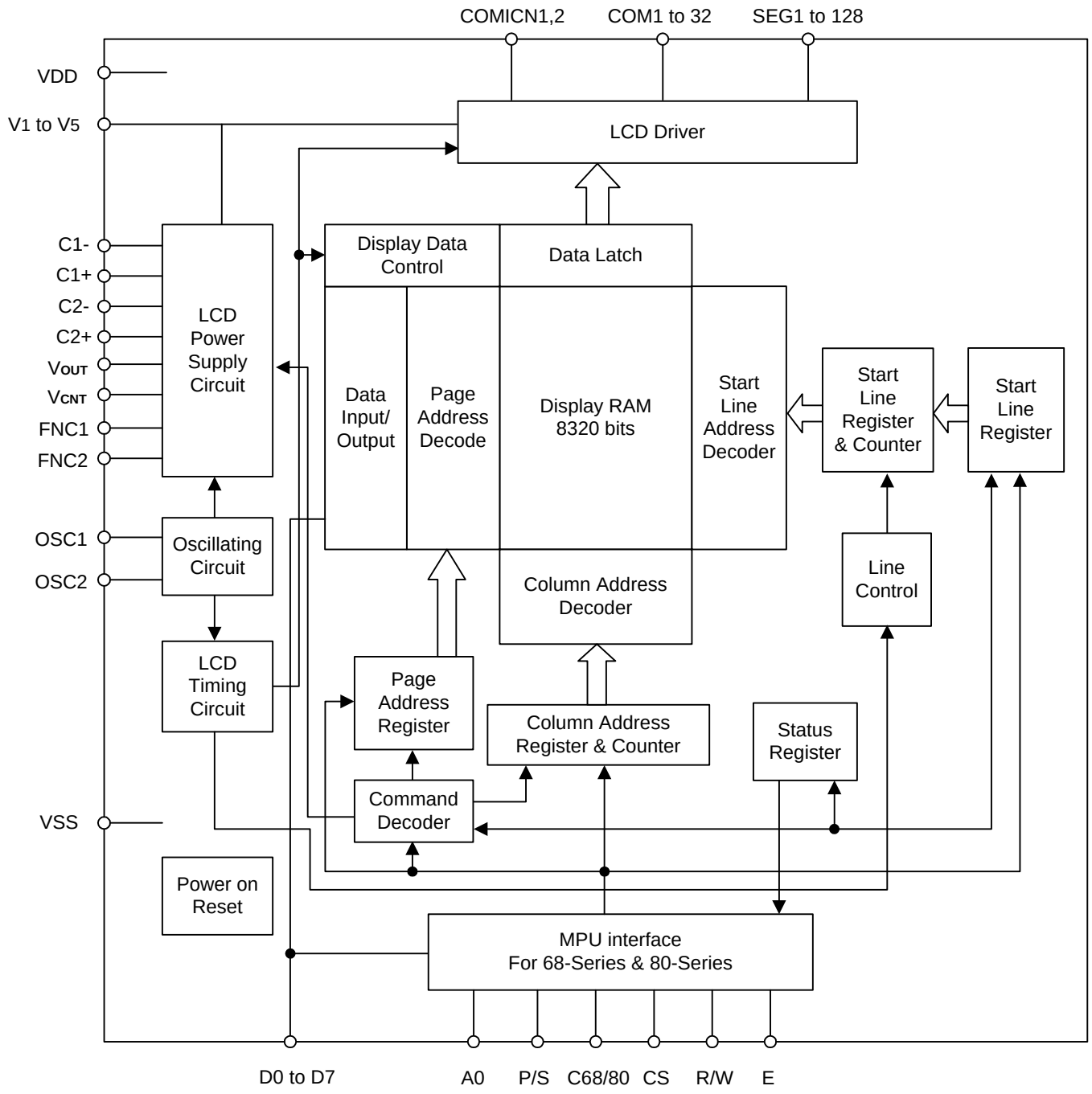
Features

- Power supply range : 2.4V to 5.5V
  2.7V to 11.0V (LCD drive)
- Internal LCD drivers :
  128 segment signal drivers
  17 /33 commons signal drivers
- Power save current (<1uA)
- On chip 128 x 65 Display Data RAM
- 8 BIT 80/68-Series Parallel interface ,Serial interface
- Build-in RC oscillator or external clock input (18KHz)
- 1:4 / 1:5 / 1:6.7(default) Bias Ratio
- 1:2 to 1:4 Bias Ratio (external)
- 16 level internal contrast control
- Build-in temperature compensation circuit
- On chip internal DC/DC converter / External Power supply
- Dual/ Triple booster
- 2 internal Icon common Output systems
- TCP package, Gold bumps

The A31W33128 is a CMOS LCD driver, which has 128 segment, and 17 or 33 common graphic display. It has 80/68-series 8 bit parallel and serial interface capability for operating with general CPU. The internal 65 x 128 display data RAM makes the display of both graphics and characters possible. Besides the general LCD driver features, it has on chip LCD bias divider circuit such that minimize external component required in system application.

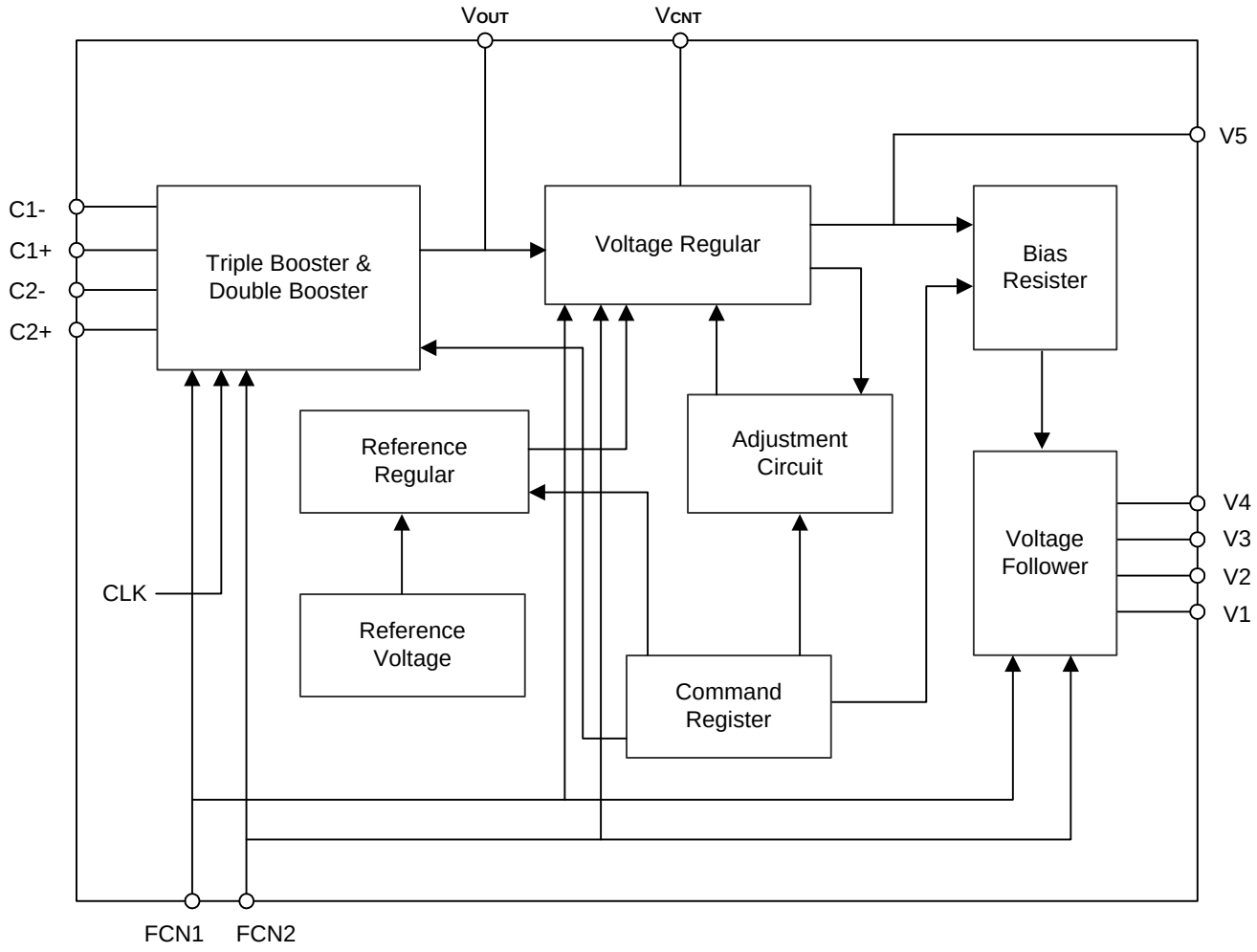
Block Diagram

1. Block Overview

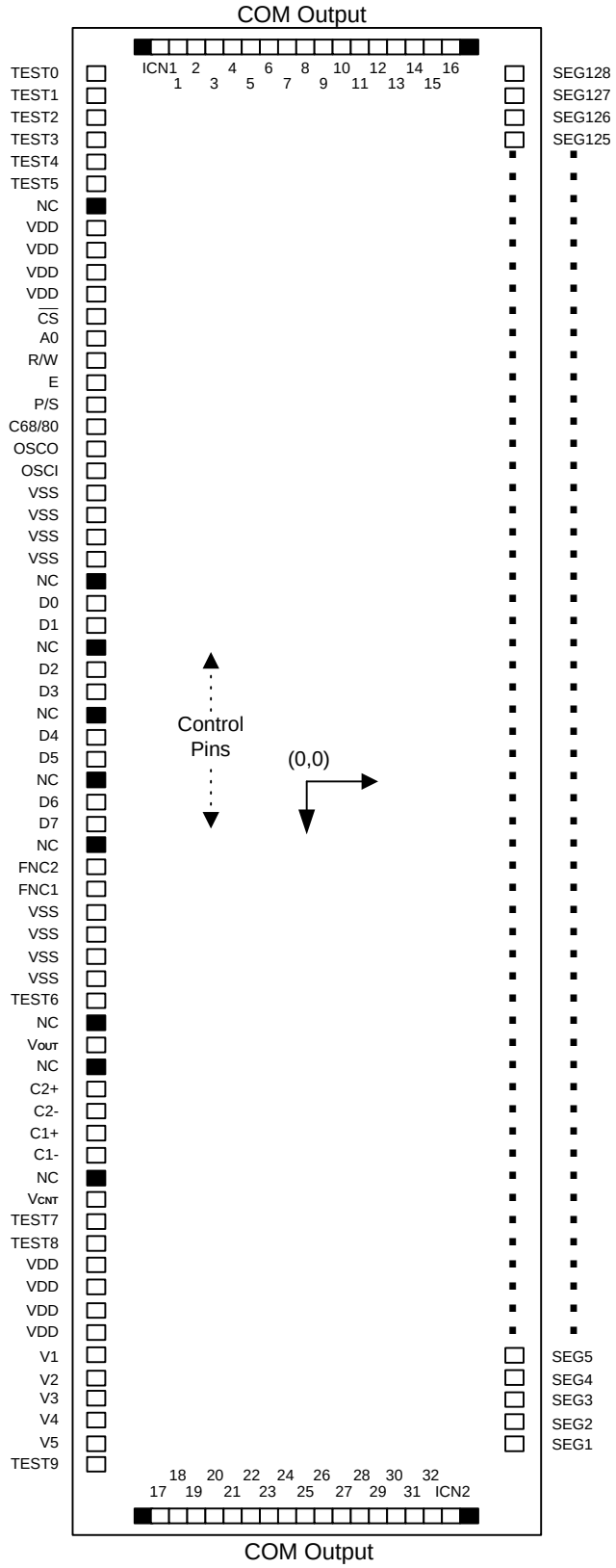


Block Diagram

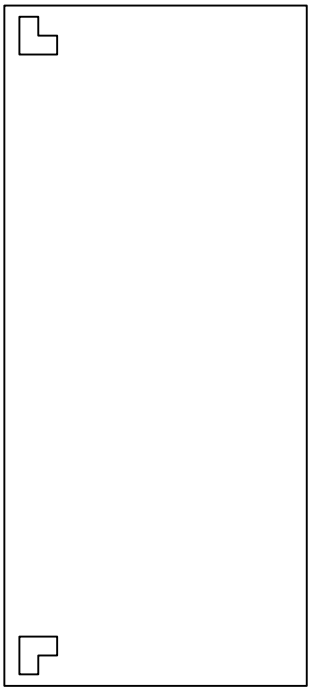
2. LCD Power Supply Circuit Block Diagram



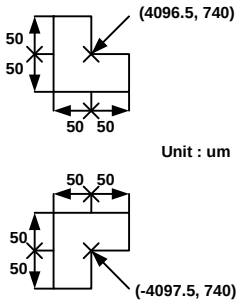
Pad Assignment



Chip Identification Marks



(The identification marks are larger than the actual scaling)



(The identification marks are made of Al patterns)

. Pad pitch
  - Segment driver 65um
  - Comon driver 65um
  - Control pad 120um

. Gold bump size
  - Drive 43x85um
  - Input pin 72x85um

. Gold bump height 18um (Typ.)

Pad Coordinates

Unit: μm (The origin is the center of the chip)

No.	Pin Name	X	Y	No.	Pin Name	X	Y
1	TEST0	-3877.5	-897.5	64	TEST9	3877.7	-897.5
2	TEST1	-3807.5	-897.5	65	NC	4103.5	-717.5
3	TEST2	-3737.5	-897.5	66	COM17	4103.5	-647.5
4	TEST3	-3667.5	-897.5	67	COM18	4103.5	-577.5
5	TEST4	-3597.5	-897.5	68	COM19	4103.5	-507.5
6	TEST5	-3527.5	-897.5	69	COM20	4103.5	-437.5
7	NC	-3457.5	-897.5	70	COM21	4103.5	-367.5
8	VDD	-3371.5	-897.5	71	COM22	4103.5	-297.5
9	VDD	-3251.5	-897.5	72	COM23	4103.5	-227.5
10	VDD	-3131.5	-897.5	73	COM24	4103.5	-157.5
11	VDD	-3011.5	-897.5	74	COM25	4103.5	-87.5
12	$\overline{CS}$	-2891.4	-897.5	75	COM26	4103.5	-17.5
13	A0	-2763.6	-897.5	76	COM27	4103.5	52.5
14	R/W	-2635.8	-897.5	77	COM28	4103.5	122.5
15	E	-2508	-897.5	78	COM29	4103.5	192.5
16	P/S	-2380.2	-897.5	79	COM30	4103.5	262.5
17	C68/80	-2252.4	-897.5	80	COM31	4103.5	332.5
18	OSCO	-2124.6	-897.5	81	COM32	4103.5	402.5
19	OSCI	-1996.8	-897.5	82	COMICN2	4103.5	472.5
20	VSS	-1876.8	-897.5	83	NC	4103.5	548.5
21	VSS	-1756.8	-897.5	84	SEG1	4127.5	897.5
22	VSS	-1636.8	-897.5	85	SEG2	4062.5	897.5
23	VSS	-1516.8	-897.5	86	SEG3	3997.5	897.5
24	NC	-1430.8	-897.5	87	SEG4	3932.5	897.5
25	D0	-1264.2	-897.5	88	SEG5	3867.5	897.5
26	D1	-999.8	-897.5	89	SEG6	3802.5	897.5
27	NC	-835.2	-897.5	90	SEG7	3737.5	897.5
28	D2	-670.6	-897.5	91	SEG8	3672.5	897.5
29	D3	-406.2	-897.5	92	SEG9	3607.5	897.5
30	NC	-241.6	-897.5	93	SEG10	3542.5	897.5
31	D4	-77	-897.5	94	SEG11	3477.5	897.5
32	D5	187.4	-897.5	95	SEG12	3412.5	897.5
33	NC	352	-897.5	96	SEG13	3347.5	897.5
34	D6	516.6	-897.5	97	SEG14	3282.5	897.5
35	D7	781	-897.5	98	SEG15	3217.5	897.5
36	NC	945.6	-897.5	99	SEG16	3152.5	897.5
37	FNC2	1049.2	-897.5	100	SEG17	3087.5	897.5
38	FNC1	1177	-897.5	101	SEG18	3022.5	897.5
39	VSS	1298.7	-897.5	102	SEG19	2957.5	897.5
40	VSS	1418.7	-897.5	103	SEG20	2892.5	897.5
41	VSS	1538.7	-897.5	104	SEG21	2827.5	897.5
42	VSS	1658.7	-897.5	105	SEG22	2762.5	897.5
43	TEST6	1744.7	-897.5	106	SEG23	2697.5	897.5
44	NC	1814.7	-897.5	107	SEG24	2632.5	897.5
45	V_{OUT}	1900.7	-897.5	108	SEG25	2567.5	897.5
46	NC	1981.7	-897.5	109	SEG26	2502.5	897.5
47	C2+	2062.7	-897.5	110	SEG27	2437.5	897.5
48	C2-	2182.7	-897.5	111	SEG28	2372.5	897.5
49	C1+	2302.7	-897.5	112	SEG29	2307.5	897.5
50	C1-	2422.7	-897.5	113	SEG30	2242.5	897.5
51	NC	2503.7	-897.5	114	SEG31	2177.5	897.5
52	V_{CNT}	2589.7	-897.5	115	SEG32	2112.5	897.5
53	TEST7	2675.7	-897.5	116	SEG33	2047.5	897.5
54	TEST8	2745.7	-897.5	117	SEG34	1982.5	897.5
55	VDD	2831.7	-897.5	118	SEG35	1917.5	897.5
56	VDD	2951.7	-897.5	119	SEG36	1852.5	897.5
57	VDD	3071.7	-897.5	120	SEG37	1787.5	897.5
58	VDD	3191.7	-897.5	121	SEG38	1722.5	897.5
59	V1	3311.7	-897.5	122	SEG39	1657.5	897.5
60	V2	3431.7	-897.5	123	SEG40	1592.5	897.5
61	V3	3551.7	-897.5	124	SEG41	1527.5	897.5
62	V4	3671.7	-897.5	125	SEG42	1462.5	897.5
63	V5	3791.7	-897.5	126	SEG43	1397.5	897.5

Pad Coordinates (continued)

Unit: μm (The origin is the center of the chip)

No.	Pin Name	X	Y	No.	Pin Name	X	Y
127	SEG44	1332.5	897.5	190	SEG107	-2762.5	897.5
128	SEG45	1267.5	897.5	191	SEG108	-2827.5	897.5
129	SEG46	1202.5	897.5	192	SEG109	-2892.5	897.5
130	SEG47	1137.5	897.5	193	SEG110	-2957.5	897.5
131	SEG48	1072.5	897.5	194	SEG111	-3022.5	897.5
132	SEG49	1007.5	897.5	195	SEG112	-3087.5	897.5
133	SEG50	942.5	897.5	196	SEG113	-3152.5	897.5
134	SEG51	877.5	897.5	197	SEG114	-3217.5	897.5
135	SEG52	812.5	897.5	198	SEG115	-3282.5	897.5
136	SEG53	747.5	897.5	199	SEG116	-3347.5	897.5
137	SEG54	682.5	897.5	200	SEG117	-3412.5	897.5
138	SEG55	617.5	897.5	201	SEG118	-3477.5	897.5
139	SEG56	552.5	897.5	202	SEG119	-3542.5	897.5
140	SEG57	487.5	897.5	203	SEG120	-3607.5	897.5
141	SEG58	422.5	897.5	204	SEG121	-3672.5	897.5
142	SEG59	357.5	897.5	205	SEG122	-3737.5	897.5
143	SEG60	292.5	897.5	206	SEG123	-3802.5	897.5
144	SEG61	227.5	897.5	207	SEG124	-3867.5	897.5
145	SEG62	162.5	897.5	208	SEG125	-3932.5	897.5
146	SEG63	97.5	897.5	209	SEG126	-3997.5	897.5
147	SEG64	32.5	897.5	210	SEG127	-4062.5	897.5
148	SEG65	-32.5	897.5	211	SEG128	-4127.5	897.5
149	SEG66	-97.5	897.5	212	NC	-4103.5	542.5
150	SEG67	-162.5	897.5	213	COM16	-4103.5	472.5
151	SEG68	-227.5	897.5	214	COM15	-4103.5	402.5
152	SEG69	-292.5	897.5	215	COM14	-4103.5	332.5
153	SEG70	-357.5	897.5	216	COM13	-4103.5	262.5
154	SEG71	-422.5	897.5	217	COM12	-4103.5	192.5
155	SEG72	-487.5	897.5	218	COM11	-4103.5	122.5
156	SEG73	-552.5	897.5	219	COM10	-4103.5	52.5
157	SEG74	-617.5	897.5	220	COM9	-4103.5	-17.5
158	SEG75	-682.5	897.5	221	COM8	-4103.5	-87.5
159	SEG76	-747.5	897.5	222	COM7	-4103.5	-157.5
160	SEG77	-812.5	897.5	223	COM6	-4103.5	-227.5
161	SEG78	-877.5	897.5	224	COM5	-4103.5	-297.5
162	SEG79	-942.5	897.5	225	COM4	-4103.5	-367.5
163	SEG80	-1007.5	897.5	226	COM3	-4103.5	-437.5
164	SEG81	-1072.5	897.5	227	COM2	-4103.5	-507.5
165	SEG82	-1137.5	897.5	228	COM1	-4103.5	-577.5
166	SEG83	-1202.5	897.5	229	COMICN1	-4103.5	-647.5
167	SEG84	-1267.5	897.5	230	NC	-4103.5	-717.5
168	SEG85	-1332.5	897.5				
169	SEG86	-1397.5	897.5				
170	SEG87	-1462.5	897.5				
171	SEG88	-1527.5	897.5				
172	SEG89	-1592.5	897.5				
173	SEG90	-1657.5	897.5				
174	SEG91	-1722.5	897.5				
175	SEG92	-1787.5	897.5				
176	SEG93	-1852.5	897.5				
177	SEG94	-1917.5	897.5				
178	SEG95	-1982.5	897.5				
179	SEG96	-2047.5	897.5				
180	SEG97	-2112.5	897.5				
181	SEG98	-2177.5	897.5				
182	SEG99	-2242.5	897.5				
183	SEG100	-2307.5	897.5				
184	SEG101	-2372.5	897.5				
185	SEG102	-2437.5	897.5				
186	SEG103	-2502.5	897.5				
187	SEG104	-2567.5	897.5				
188	SEG105	-2632.5	897.5				
189	SEG106	-2697.5	897.5				

Input/Output Pin Function

Pin No.	Symbol	Type	Description
20-23, 39-42	VSS	Supply	GROUND
8-11, 55-58	VDD	Supply	Power supply pin
18	OSCO	Output	Oscillator output
19	OSCI	Input	Oscillator input
12	$\overline{CS}$	Input	Chip select input, low active
13	A0	Input	A0=Low: Command input. A0=High: Display data input and outputs
14	R/W	Input	68-Series R/W=High: Read, R/W=Low : Write
			80-Series : Write enable, Active Low
15	E	Input	68-Series : Enable clock signal input, Active High
			80-Series : Read enable, Active Low
16	P/S	Input	Parallel/serial interface select input High : 8-bit parallel interface Low : Serial interface
17	C68/80	Input	Microprocessor interface select input High : 68-Series interface is selected Low : 80-Series interface is selected
25-26, 28-29, 31-32, 34-35	D0-7	Input/ Output	8bit bi-directional data bus to be connected to microprocessor's data bus P/S=High : 8-bit configuration data bus connection P/S=Low : Serial interface connection D0 Serial data input D1 Serial clock input D2 Serial data output
84-211	SEG1-SEG128	Output	Provide the LCD segment driving signal
66-81 213-228	COM1-COM32	Output	Provide the LCD common driving signal
229 82	COMICN1 COMCN2	Output	Provide the Icon common driving signal COMICN1 and COMICN2 output the same phase waveform.
37	FNC2	Input	LCD power control input pin
38	FNC1	Input	LCD power control input pin
42	V_{OUT}	Output	Boosting voltage output
47	C2+	Input	2nd-step boosting capacitor negative connection
48	C2-	Input	2nd-step boosting capacitor positive connection
49	C1+	Input	1 st-step boosting capacitor negative connection
50	C1-	Input	1 st-step boosting capacitor positive connection
52	V_{CNT}	Input	LCD power supply voltage control

Input/Output Pin Function (continued)

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>59</td><td>V1</td><td>Input</td><td rowspan="5">LCD driver bias voltage. They can be supplied externally or generated by the internal bias divider.
<table><tr><th></th><th>1: 4 bias</th><th>1: 5 bias</th><th>1: 6.75 bias</th></tr><tr><td>V1</td><td>1/4 x V5</td><td>1/5 x V5</td><td>1/6.75 x V5</td></tr><tr><td>V2</td><td>2/4 x V5</td><td>2/5 x V5</td><td>2/6.75 x V5</td></tr><tr><td>V3</td><td>2/4 x V5</td><td>3/5 x V5</td><td>4.75/6.75 x V5</td></tr><tr><td>V4</td><td>3/4 x V5</td><td>4/5 x V5</td><td>5.75/6.75 x V5</td></tr></table>• Inputs LCD drive bias voltage when using an external LCD power supply circuit.
V5 ≥ V4, V3, V2, V1 > VSS</td></tr>
<tr><td>60</td><td>V2</td><td>Input</td></tr>
<tr><td>61</td><td>V3</td><td>Input</td></tr>
<tr><td>62</td><td>V4</td><td>Input</td></tr>
<tr><td>63</td><td>V5</td><td>Input</td></tr>
<tr><td>1-7, 24, 27, 30, 33, 36, 43-44, 46, 51, 53-54, 64-65, 83, 212, 230</td><td>NC</td><td>Open</td><td>No Connection</td></tr>
<tr><td>1</td><td>TEST0</td><td rowspan="10">Open</td><td rowspan="10">Cannot be wired to the outside</td></tr>
<tr><td>2</td><td>TEST1</td></tr>
<tr><td>3</td><td>TEST2</td></tr>
<tr><td>4</td><td>TEST3</td></tr>
<tr><td>5</td><td>TEST4</td></tr>
<tr><td>6</td><td>TEST5</td></tr>
<tr><td>43</td><td>TEST6</td></tr>
<tr><td>53</td><td>TEST7</td></tr>
<tr><td>54</td><td>TEST8</td></tr>
<tr><td>64</td><td>TEST9</td></tr>
</table>

Commands Table

Command	Bit pattern											Comment
	A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	D0:0 Display OFF: Display goes out, regardless of the content of the display data RAM D0:1 Display ON: Normal Display
Set Display Start Line	0	1	0	0	1	Display start line address						Sets the line address of the display data RAM output to COM1
Page Address Set	0	1	0	1	0	1	1	Page Address				Sets the page address of the display data RAM. Page 8 is assigned to the icon display
Upper 3 bits of Column Address Set	0	1	0	0	0	0	1	0	Upper 3 bits of Column Address			Sets upper 3 bits of the display data RAM Column Address
Lower 4 bits of the Column Address Set	0	1	0	0	0	0	0	Lower 4 bits of the Column Address				Lower 4 bits of display data RAM column Address
Status Read	0	0	1	Status								Status Read
Display Data Write	1	1	0	Write Data in Display Data RAM								Writes data of D0 to D7 in the display data RAM
Display Data Read	1	0	1	Read Data from Display Data RAM								Reads data from D0 to D7 from the display data RAM
ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Reverses upper or lower display data RAM column address D0:0 Normal: Column addresses 00 to 7FH correspond to segment outputs 1 to 128 D0:1 Reverse: Column addresses 00 to 7FH correspond to segment outputs 128 to 1
Display Normal/Reverse	0	1	0	1	0	1	0	0	1	1	0 1	D0:0 Normal : "1" makes the display be lit D0:1 Reverse : "0" makes the display be lit The icon display is not reversed
Display All-Lit ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	D0:0 Normal Display D0:1 Display All-Lit
Duty Selection/ Alternate Common Output	0	1	0	1	0	1	0	1	0	* 0 1	0 1 1	D0:0 1/17 Duty D0:1 1/33 Duty D1:0 Common output order: In a numerical order D1:1 Common output order: Alternate output to right and left of the chip.
Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments display data RAM column address only during writing
End	0	1	0	1	1	1	0	1	1	1	0	Read Modify Write Release.
Reset	0	1	0	1	1	1	0	0	0	1	0	It does not affect the contents of the display data RAM. After resetting, display starts according to the reset value: 1.Resets the display start line register to the 1st line. 2.Resets the column address counter to address 0. 3.Resets the page address counter to page 0. 4.Clears the serial interface counter. 5.Turns OFF the Read Modify Write.

Commands Table (continued)

Command	Bit pattern										Comment
	A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	
Bias Selection	0	1	0	0	0	1	0	1	0	D1	D0	D1,D0:0, 0 1/6.75 Bias Selection D1,D0:0, 1 1/5 Bias Selection D1,D0:1, 0 1/4 Bias Selection D1,D0:1, 1 Don't care
LCD Voltage Command Fine Adjustment Data	0	1	0	1	0	0	0	0 . 1	0 . 1	0 . 1	0 . 1	Minimum value (default) Maximum value
LCD Power Supply Circuit ON/OFF	0	1	0	0	0	1	0	0	1	0	0 1	D0: 0 LCD power supply circuit OFF D0: 1 LCD power supply circuit ON The LCD power supply circuit connected to pinsFNC1, FNC2 starts its operation earlier than the LCD POWER Supply circuit ON/OFF command.
Icon Only Display	0	1	0	1	1	0	0	0	D2	Boosting Control Data		D2: 0 Normal Display D2: 1 Icon Only Display Boosting control data: Selects boosting Frequency
Reference Voltage Temperature Coefficient Selection	0	1	0	1	1	1	0	0	1	*	0 1	D0:0 -0.13%/°C D0:1 +0.01%/ °C
Power save												Display OFF, Display all-lit ON

Operation of LCD Display Driver

1. Powering ON setting sequence

Recommended Command Setting Sequence:

(1) Set Display OFF : In order to prevent unnecessary characters from being displayed during powering ON of the power .
The state is changed to the " Power save mode" after turning on the Display All-Lit ON with the display OFF.

(2) Set Display All-Lit OFF: Normal display operation and the oscillation start.

(3) Set LCD Power Supply Circuit ON

(4) Set Bias Select

(5) Set Reference Voltage Temperature Compensation Coefficient

(6) End Command Input

(7) Set Duty Select/Alternate Common Output

(8) Set Display Normal/Reverse :

D0 : 0 Normal Display data "1" makes the display be lit.

D0 : 1 Reverse Display data "0" makes the display be lit.

(9) Set Display Start Line address: Changing the display start line allows for page change on the display screen as well as vertical smooth scroll.

(10) Common Output Sequence

(11) Icon Only Display

(12) Display Data Write: After writing the display data, the column address is automatically incremented. To write the display data in succession after setting the 1st column address to be written by the COLUMN ADDRESS SETTING command, the column address is not needed to be set each time. The icon display data is valid for only D0.
Write "L" or data to be displayed in all display data RAM before turning the display ON.

(13) Display ON

2. Set Powering OFF, Power Save Mode

Set Powering OFF sequence:

(1) Set Display OFF

(2) Set LCD Power Supply Circuit OFF

Power Save Mode:

When in Power save mode, the command sleeps the system :

- Internal oscillating circuit and LCD power supply circuit are stopped.
- The Segment and Common outputs are fixed at VSS level.
- The LCD display goes out.
- The contents of the display data RAM, the command and the address before the power save mode do not change.

Combination of Commands		State
Display ON	Display All-Lit OFF	Normal display operation
Display ON	Display All-Lit ON	All-lit display
Display OFF	Display All-Lit OFF	AII-OFF
Display OFF	Display All-Lit ON	Power save

3. MPU Interface Select

The parallel 68-series, 80-series interface or serial interface can be selected by P/S, C68/80 pin setup:

P/S Pin	C68/80 Pin	MPU Interface
H	L	80-series Interface selected
	H	68-series Interface selected
L	don't care	Serial Interface selected

3.1 MPU Parallel 68-Series and 80-Series Interface

The parallel interface consists of 8 bi-directional data pins (D0-D7), R/W($\overline{WR}$), A0, E($\overline{RD}$), $\overline{CS}$ In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read.

A31W33128 Pin Name	A0	E	R/W	$\overline{CS}$	D0 - D7
68-Series MPU Signal	A0	E	R/W	$\overline{CS}$	D0 - D7
80-Series MPU Signal	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	D0 - D7

3.2 MPU Serial Interface

The serial interface consists of serial clock input SCLK, serial data input SDI and output SDO, chip select $\overline{CS}$, P/S, R/W, A0. When the E pin to be open and the serial interface is selected by setting P/S to “L”, the instruction code is the same as for the parallel interface .By setting $\overline{CS}$ to “L”. the serial interface circuit enters an operating state. And by setting $\overline{CS}$ to “H’, it will reset the serial interface circuit and initialized the counter.
Data is input in the order of D0, D1, D2,....D7. The displayed data and commands are written at the rising edge of the SCLK. But the displayed data and status are read at the falling edge of the SCLK. Data read needs a dummy read. When in reset condition, the SDO pin will be driven to “H”, and the status reading will be invalidated.

D0 (SDI) : Serial Data Input
D1 (SCLK) : Serial Clock Input
D2 (SDO) : Serial Data Output
D3 to D7 : Open
E : Open
C68/80 : Open

A0	R/W	Operation
L	L	Command input
H	H	Display data read
L	H	Status read
H	L	Display data write

4. Command Execution

When the input at D0-D7 is interpreted as a command and it will be decoded and written to the corresponding command register. The user can input the commands continuously without confirming the busy flag of status command register because the command is completely executed within the cycle time (tcyc) according to the timing characteristics of the command input. But that re-inputting the command within the executed cycle time is inhibited.

5. Data Bus Select

When $\overline{CS}$ is held at "H" level, the D0-D7 is in high impedance state.

68/80-Series shared	68-Series	80-Series		Description
A0	R/W	E	R/W	
1	1	0	1	Reads from Display Data RAM
1	0	1	0	Writes to Display Data RAM
0	1	0	1	Reads Status
0	0	1	0	Command Write to internal register

6. Display Data RAM

The Display Data RAM is made of dual port RAM. The size of the RAM is 64 x 128 + 128 = 8320 bits.
Write "L" or data to be displayed in all display data RAM before turning the display ON.

7. Accessing the Display Data RAM From MPU

In order to match the operating frequency of Display Data RAM with that of the MPU, a dummy read is required before the first actual display data read. When the MPU reads the Display Data RAM, the first dummy read cycle stores the first read data in the bus holder, and then at the next read cycle the MPU read the first read data from the bus holder.
It does not need a dummy cycle when MPU writes data to the Display Data RAM. When the MPU write data to Display Data RAM, once the data is stored in the bus holder, then it is written to Display Data RAM before the next data write cycle.

8. Set Column Address (higher, lower nibble)

This command specifies the column address (higher and lower nibble) of the Display Data RAM. The column address will be incremented by each data access after it is pre-set by the MPU.

9. Set Page Address(0-8)

This command positions the page address to 1 of 9 possible positions in Display Data RAM. Page 0-7 are the graphic display area, and the page 8 are the Icon display area.

10. Set display start line (0-63)

The command is used to change the display page or smooth scroll.

With the display start line value equals to 0, D0 of page 0 is mapped to COM1. The display start line values of 0 to 63 are assigned to page 0 to 7.

11. Status Read

This command shows the status of A31W33128

BUSY : D7 =0 : The A31W33128 is not busy
1 : The A31W33128 is in internal operation or reset state.
ADC : D6 =0 : ADC Reverse : Column addresses 00 to 7FH correspond to segment outputs 128 to 1.
1 : ADC Normal : Column addresses 00 to 7FH correspond to segment outputs 1 to 128.
ON/OFF : D5 =0 : Display ON
1 : Display OFF
RESET : D4 =0 : In normal operation state
1 : Internal reset operation state
PSAVE : D3 =0 : In normal operation state
1 : In Power Save state
ICON : D2 =0 : In normal operation state
1 : In Icon only display state
DREV : D1 =0 : Display Normal
1 : Display Reverse
ALON : D0 =0 : Normal display
1 : Display All-Lit ON

When a serial interface is selected, the status read from the SDO pin is always high level during reset operation.

12. 1/33 ,1/17 Duty Select, Alternate Common Output

Common Output sequence at duty 1/33

Output sequence	Common driving signal output in numerical	Common driving signal Alternate Output
1	COM1	COM1
2	COM2	COM17
3	COM3	COM2
:	:	:
16	COM16	COM9
17	COM17	COM25
:	:	:
31	COM31	COM16
32	COM32	COM32
33	COMICN1,2	COMICN1,2

Common Output sequence at duty 1/17

Output sequence	Common driving signal output in numerical
1	COM1,17
2	COM2,18
3	COM3,19
:	:
15	COM15,31
16	COM16,32
17	COMICN1,2

The common output at duty 1/17 only has in numerical sequence.

13. Read Modify Write , END

Read Modify Write

This command puts the chip in read modify write mode. In this mode the column address is saved before entering the mode, and is incremented by display data write but not by display data read. During the Read Modify Write mode, all commands are usable except the Column address set command.

End

This command relieves the A31W33128 from read modify write mode. The column address that is saved before entering read modify write mode will be restored.

14. Boosting frequency select

Select the boosting frequency:

D1	D0	Boosting Freq.
0	0	Fosc/2
0	1	Fosc/4
1	0	Fosc/8
1	1	Fosc/16

15. RC Oscillator Circuit

The built-in RC oscillator generates the clock for the boosting frequency, and is also used in the display timing. When using the external clock, the external clock is input to OSCI, and OSCO is left floating.

Used built-in RC oscillator , Rf = 1 MΩ		
1/17 duty	Frame freq. 66.17 Hz	at fosc = 18 KHz
1/33 duty	Frame freq.68.18 Hz	at fosc = 18 KHz

16. Reference Voltage Temperature Compensation Coefficient Select

This command is to set one out of 2 different temperature coefficients in order to match various liquid crystal temperature grades.

$$\Delta V_{REF} = \frac{|V_{REF}(T_2)| - |V_{REF}(T_1)|}{T_2 - T_1}$$

$T_2 > T_1$

17. LCD Power Supply Circuit

The LCD power supply circuit generates the LCD voltage needed for display output, which is controlled by pins FNC1 ,FNC2 and LCD power supply circuit ON/OFF command. It consists of:

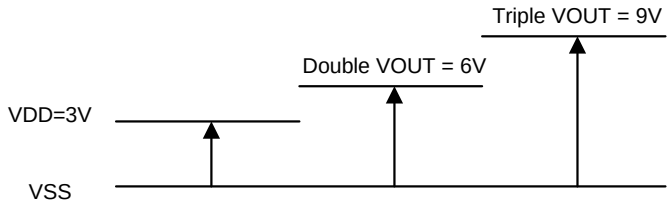
1. Doubler/tripler DC-DC voltage converter.
2. Voltage regulator and LCD voltage command fine adjustment circuit.
3. LCD bias resistor and voltage follower

FNC2	FNC1	Doubler/Tripler Circuit	Voltage Regulator Circuit	LCD Bias Resistor/ Voltage Follower Circuit
L	L	ON	ON	ON
H	L	OFF	OFF	OFF
L	H	OFF	ON	ON
H	H	OFF	OFF	ON

- FNC1 and FNC2 must connect to VDD or VSS.
- Don't connect the external power supply with the built-in LCD power supply circuit ON, it may lead to a breakdown.

17.1 Doubler/Tripler

It is the 2X, 3X DC-DC voltage converter. Please refer to application notes.



Example of Booster Output

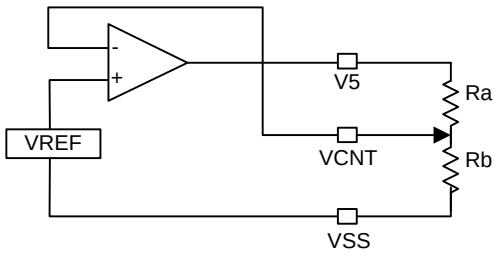
17.2 LCD Voltage Adjustment

There are two methods of adjusting the LCD voltage as follows:

17.2.1 Voltage Regulator

Voltage regulator output V5 is adjusted by externally attached Ra and Rb.

$$V5 = \frac{Ra + Rb}{Ra} \times VREF\ (V)$$



17.2.2 LCD Voltage Command Fine Adjustment control

Software control of 16 voltage levels adjustment of V5 voltage by set 4 bits of the data bus. It can adjust the LCD contrast.

17.3 LCD Bias voltage

When use built-in LCD bias resistor, Software can control the 1/6.7, 1/5,1/4 bias ratio to match the characteristic of LCD panel.

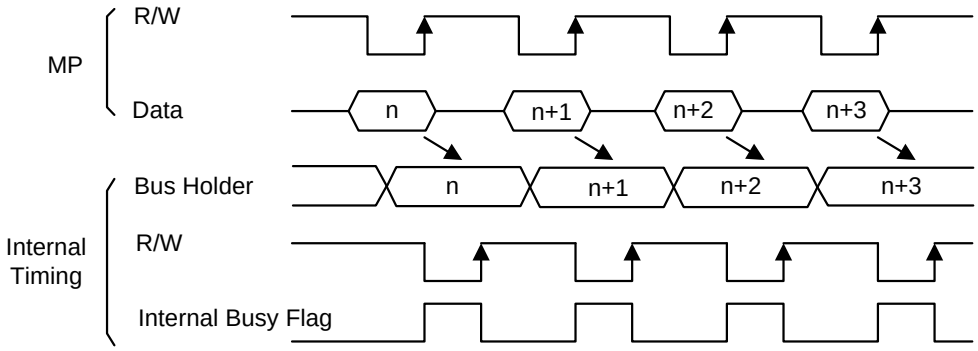
17.4 Voltage Follower

The voltage follower buffers the LCD bias voltage created by the built-in bias resistor, and supplies it to the LCD drive circuit.

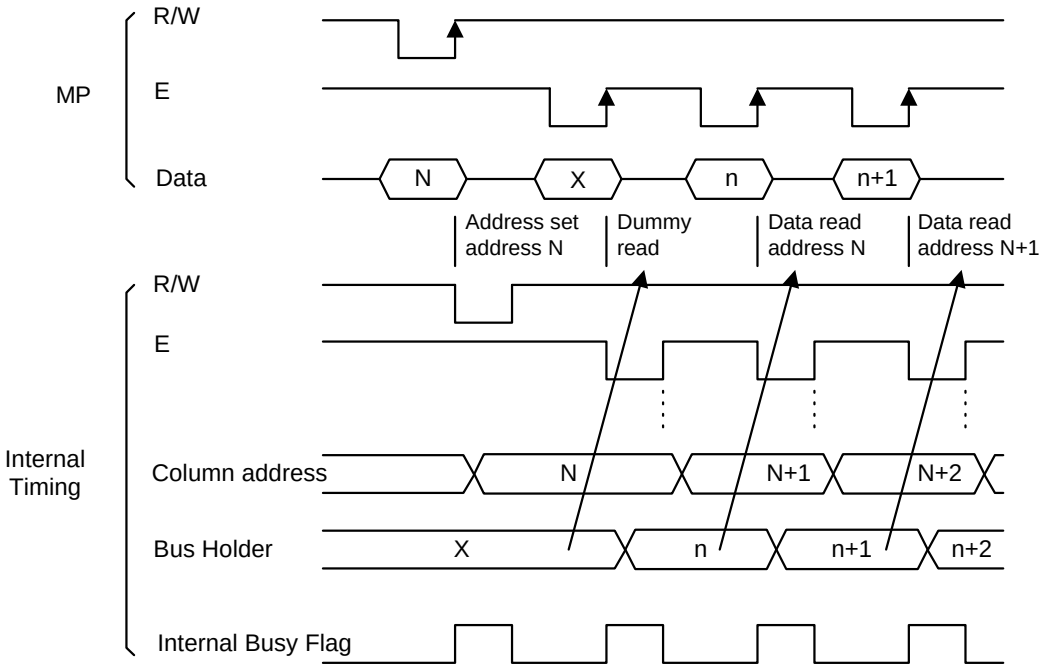
Interface

1. Parallel Interface

1.1 Display Data Write (the 80-Series interface)

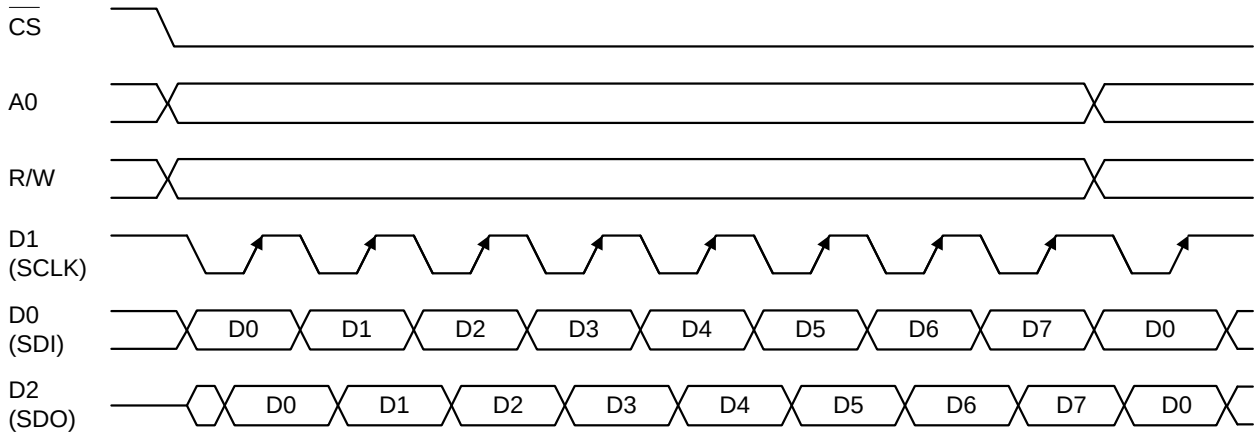


1.2 Display Data Read (the 80-Series interface)



2 Serial Interface

Serial Interface Display Data Write/Read Timing



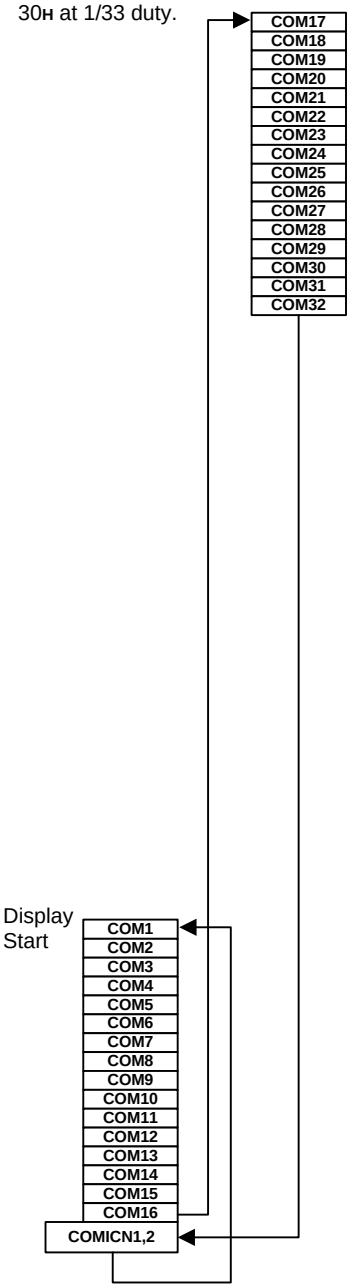
A0	R/W	D0 (SDI)	D2 (SDO)
0	0	Command Write	Invalid
0	1	Invalid	Status Read
1	0	Data Write	Invalid
1	1	Invalid	Data Read (Note)

Note: Data Read needs a dummy read

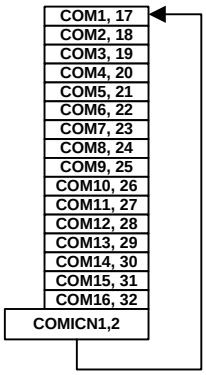
Display Data RAM vs Address

Page Address			Line Address
0, 0, 0, 0	D0	Page0	00H
	D1		01H
	D2		02H
	D3		03H
	D4		04H
	D5		05H
	D6		06H
	D7		07H
0, 0, 0, 1	D0	Page1	08H
	D1		09H
	D2		0AH
	D3		0BH
	D4		0CH
	D5		0DH
	D6		0EH
	D7		0FH
0, 0, 1, 0	D0	Page2	10H
	D1		11H
	D2		12H
	D3		13H
	D4		14H
	D5		15H
	D6		16H
	D7		17H
0, 0, 1, 1	D0	Page3	18H
	D1		19H
	D2		1AH
	D3		1BH
	D4		1CH
	D5		1DH
	D6		1EH
	D7		1FH
0, 1, 0, 0	D0	Page4	20H
	D1		21H
	D2		22H
	D3		23H
	D4		24H
	D5		25H
	D6		26H
	D7		27H
0, 1, 0, 1	D0	Page5	28H
	D1		29H
	D2		2AH
	D3		2BH
	D4		2CH
	D5		2DH
	D6		2EH
	D7		2FH
0, 1, 1, 0	D0	Page6	30H
	D1		31H
	D2		32H
	D3		33H
	D4		34H
	D5		35H
	D6		36H
	D7		37H
0, 1, 1, 1	D0	Page7	38H
	D1		39H
	D2		3AH
	D3		3BH
	D4		3CH
	D5		3DH
	D6		3EH
	D7		3FH
1, 0, 0, 0	D0	Page8	40H
Column Address	00, 01, 02, 03, 04, 05, 06, 07 ..... 3F, 40 ..... 7E, 7F		ADC D0= "0"
	7F, 7E, 7D, 7C, 7B, 7A, 79, 78 ..... 01, 00		ADC D0= "1"
SEG Pin	1, 2, 3, 4, 5, 6, 7, 8 ..... 127, 128		

An example of common output executing display start from line address 30H at 1/33 duty.

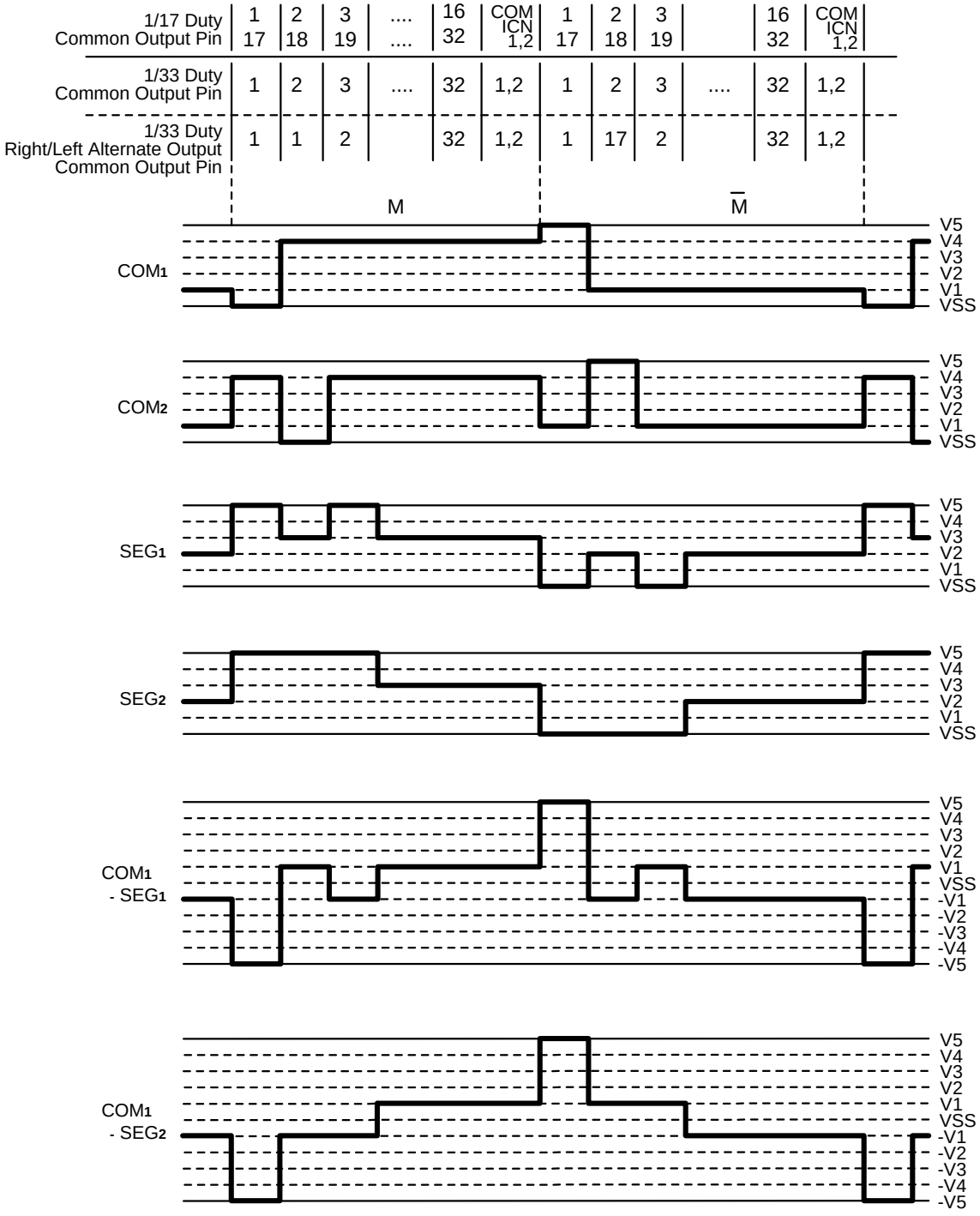


An example of common output executing display start from line address 30H at 1/17 duty.



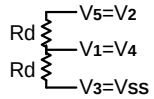
LCD Drive Output Waveform (Waveform B)

The following is an example of how the common and segment drivers may be connected to a LCD panel.

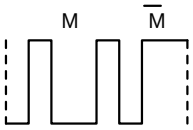


Examples of External Bias Resistor Connection vs LCD Drive Waveform

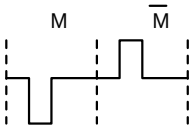
1. 1/2 Bias



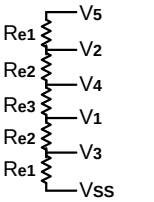
SEG Waveform



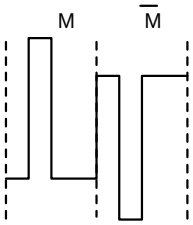
COM Waveform



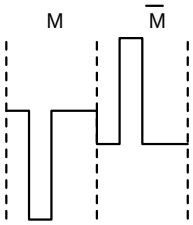
2. 1/2 to 1/3 Bias



SEG Waveform



COM Waveform



$Re_3 = \gamma(Re_1 + Re_2)$

$Re_1 = Re_3$

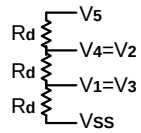
$0 \le \gamma \le 1$

Bias

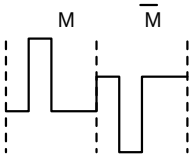
$$= \frac{Re_1 + Re_2}{Re_1 + Re_2 + Re_3 + Re_2 + Re_1}$$

$$= \frac{1}{2 + \gamma}$$

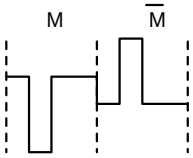
3. 1/3 Bias



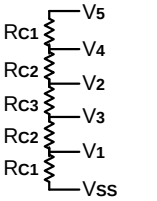
SEG Waveform



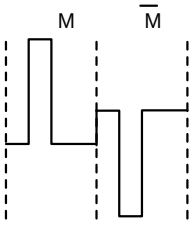
COM Waveform



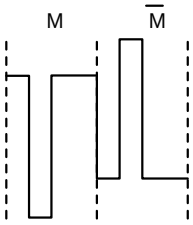
4. 1/3 to 1/4 Bias



SEG Waveform



COM Waveform



$Rc_2 + Rc_3 = Rc_1$

$Rc_2 = \beta Rc_1$

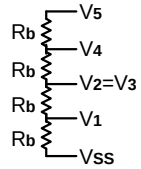
$0 \le \beta \le 1$

Bias

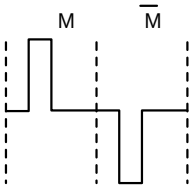
$$= \frac{Rc_1}{Rc_1 + Rc_2 + Rc_3 + Rc_2 + Rc_1}$$

$$= \frac{1}{3 + \beta}$$

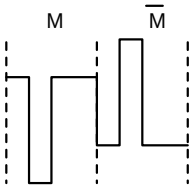
5. 1/4 Bias



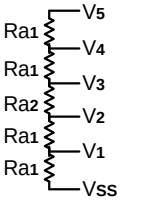
SEG Waveform



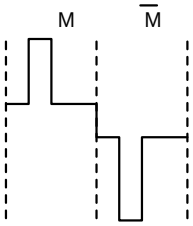
COM Waveform



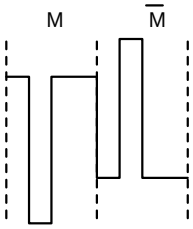
6. 1/4 Bias or more



SEG Waveform



COM Waveform



$Ra_2 = \alpha\ Ra_1$

$0 \le \alpha$

Bias

$$= \frac{Ra_1}{Ra_1 + Ra_1 + Ra_2 + Ra_1 + Ra_1}$$

$$= \frac{1}{4 + \alpha}$$

Absolute Maximum Ratings

VSS = 0.0V

Parameter		Symbol	Ratings	Unit
Supply voltage		VDD	-0.4 to +6.0	V
LCD drive voltage 1		V5	-0.4 to +12	V
LCD drive voltage 2		V1, V2, V3, V4	-0.4 to V5	V
Input voltage		V_{IN}	-0.4 to VDD+0.4	V
Output voltage		V_{OUT}	-0.4 to VDD+0.4	V
Operating temperature range		Topr	-30 to +85	°C
Storage temperature range	Chip	Tstg	-55 to +125	°C
	TAB		-55 to +100	

Note 1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note 2 Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 3 When connecting a bias resistor externally, set the LCD power supply voltage so that the state is changed to V5 ≥VDD.

DC Characteristics

1. Electrical Characteristics

(Unless otherwise specified: VDD = +5.0 ± 0.5V, VSS =0V, Ta = -30 to 85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Operating Voltage	VDD		+2.4	-	+5.5	V	1
LCD Drive Voltage	V5	When using an external LCD Power supply	+2.7	-	+11	V	2
	V1, V2		VSS	-	V5	V	
	V3, V4						
High-level Input Voltage	V_{IH}	VDD=+2.4 to +4.5V	0.8xVDD	-	VDD	V	3
		VDD=+5.0 ± 0.5V	0.8xVDD	-	VDD		
Low-level Input Voltage	V_{IL}	VDD=+2.4 to +4.5V	VSS	-	0.2xVDD	V	3
		VDD=+5.0 ± 0.5V	VSS	-	0.3xVDD		
High-level Output Voltage	V_{OH1}	I_{OH}=-0.5mA, VDD=+2.4 to+4.5V	0.8xVDD	-	-	V	4
		I_{OH}=-I.0 mA	0.8xVDD	-	-		
	V_{OH2}	I_{OH}=-50µA, VDD=+2.4 to+4.5V	0.8xVDD	-	-	V	OSCO 5
		I_{OH}=-120µA	0.8xVDD	-	-		
Low-level Output Voltage	V_{OL1}	I_{OL}=0.5mA, VDD=+2.4 to +4.5V	-	-	0.2xVDD	V	4
		I_{OL}=1.0mA	-	-	0.2xVDD		
	V_{OL2}	I_{OL}=50µA VDD=+2.4 to +4.5V	-	-	0.2xVDD	V	OSCO
		I_{OL}=120µA	-	-	0.2xVDD		
Input Leakage Current	I_{ILEAK}	VDD=+2.4 to +5.5V	-1.0	-	1.0	µA	5
Output Leakage Current	I_{OLEAK}	VDD=+2.4 to +5.5V	-3.0	-	3.0	µA	6
LCD Driver ON Resistor	R_{ON}	Ta=25°C, V5=+8.0V 1/5 Bias	-	3.0	5.0	KΩ	7
Standby Current	Is		-	0.05	5.0	µA	8
Operating Current	I_{SS1}	External LCD power supply is used: During LC display V5=+8.0 V Rf= 1 MΩ	-	20.0	30.0	µA	9
	I_{SS2}	During access: tcyc=200 KHz VDD=+3.0 ± 0.3 V	-	150	450	µA	10
		During access: tcyc=200 KHz	-	300			
Oscillating Frequency	fosc	Rf=1.0MΩ VDD=+3.0V	11	16	21	KHz	11
		Rf=1.0MΩ VDD=+5.0V	15	18	22		
Wait Time	t_R		10	-	-	µs	12

2. LCD Power Supply Circuit Electrical Characteristics

(Unless otherwise specified: VDD = +2.4V to +5.5V, VSS = 0V, Ta = -30 to 85°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Note
Operating Voltage	VDD			+2.4	-	+5.5	V	13
Boosting Output Voltage	V_{OUT}	Triple boosting: Up to VDD=3.6V Double boosting: Up to VDD=5.5V		-	-	+11.0	V	
LCD Supply Circuit Operating Voltage	V5	1/4 Bias		+4.0	-	+11.0	V	14
		1/5 Bias		+4.5	-	+11.0		
		1/6.7 Bias		+5.5	-	+11.0		
LCD Driver Operating Voltage	V_{LCD}			+2.7	-	+11.0	V	15
Built-in LCD Circuit Current Consumption	I_{SSL}	V_{OUT}=+10.0 V Double Boosting VDD=+5.0 V V5=8.0V 1/5 Bias Osc. Frequency : 18 KHz		-	+90	+200	µA	16
External LCD Power Supply Used: LCD Drive Current Consumption	I_{V5}	V5=8.0V 1/5 Bias		-	+30	+75	µA	17
Reference Voltage	V_{REF}	Ta=25°C	ΔVREF=+0.01%/°C	+2.0	+2.2	+2.4	V	18
			ΔVREF=-0.13%/°C	+1.3	+1.5	+1.7		
Reference Current	I_{REF}	Fine adjustment data (1111) Ta=25°C		1.5	2.5	4.0	µA	19
LCD Drive bias voltage (1/4 bias)	V1	V5=+4.0V to +11.0V		1/4*V5-0.1	1/4*V5	1/4*V5+0.1	V	20
	V2			2/4*V5-0.1	2/4*V5	2/4*V 5+0.1		
	V3			2/4*V5-0.1	2/4*V5	2/4*V 5+0.1		
	V4			3/4*V5-0.1	3/4*V5	3/4*V 5+0.1		
LCD Drive bias voltage (1/5 bias)	V1	V5=+4.5V to +11.0V		1/5*V5-0.1	1/5*V5	1/5*V 5+0.1		
	V2			2/5*V5-0.1	2/5*V5	2/5*V 5+0.1		
	V3			3/5*V5-0.1	3/5*V5	3/5*V 5+0.1		
	V4			4/5*V5-0.1	4/5*V5	4/5*V 5+0.1		
LCD Drive bias voltage (1/6.75 bias)	V1	V5=+5.5V to +11.0V		1/6.75*V5-0.1	1/6.75*V5	1/6.75*V 5+0.1		
	V2			2/6.75*V5-0.1	2/6.75*V5	2/6.75*V 5+0.1		
	V3			4.75/6.5* V5-0.1	4.75/6.75* V5	4.75/6.75* V5+0.1		
	V4			5.75/6.75* V5-0.1	5.75/6.75* V5	5.75/6.75* V+0.1		

3. References

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Input Pin Capacity	C_{IN}	Ta=25°C	-	5	8	pF	3

Notes:

1. Sharp variation in the supply voltage or input signal voltage due to strange noises may lead to a malfunction of the IC. Supply stable supply voltage and input signal voltage.
   If you change the level of the supply voltage intentionally, a malfunction may occur. Never change the level of the supply voltage.
2. When the external bias voltage is input, V5≥V4, V3, V2, V1≥VSS, V5≥VDD. There is no limitation for determining the voltage level of V1, V2, V3, and V4.
3. Pins A0, $\overline{CS}$, E, R/W, C68/80, P/S, OSCI, FNC1 and FNC2.
   Pins D0 to D7 during display data write and command input.
   Fully swing the levels V_{IH} and V_{IL} of the input signal within the range of power supply voltage so that the state is V_{IH} =VDD, V_{IL}=VSS. When the level of V_{IH} and V_{IL} is the middle level of the supply voltage, the through current flowing through the input pin and the current consumption may be increased.
4. Pins D0 to D7 during read.
5. Pins A0 $\overline{CS}$, E, R/W, C68/80, P/S, OSCI, FNC1 and FNC2.
6. Pins D0 to D7 during write and high-impedance.
7. ON resistance between LCD drive output pins (SEG1 to SEG128, COM1 to 32, COMICN1, and 2) and LCD drive bias voltage pins (VI, V2, V3, V4). Using the external LCD power supply, measure the resistance at a 0.1-V difference from the LCD drive output pin after applying 1/2 voltage of V5 to the LCD drive bias voltage pin.
8. Power save state. When turning the input pin to "Floating," the through current flows and will eventually the power save effect may be reduced.
9. Shows the current consumption during display including CR oscillation.
   It does not include the current consumed by the booster, LCD supply voltage adjustment circuit, voltage regulator, LCD bias resistor when using the external LCD power supply. The LCD drive output pin is no load. The current consumed by the LCD panel and wiring capacitor is not included. Measure it without access from the MPU. The current consumed by the external LCD power supply and external bias resistor and other is not included.
10. The current consumption while the checkered pattern display data are being written from the MPU. The CR oscillation is measured while the CR oscillating circuit stops. The voltage level of the input signal is the V_{IH}=VDD and V_{IL}=VSS. When the input signal voltage is in the middle level, the current consumption may be increased. When the display data is written from the MPU during display, the state is changed to I_{SS1}+I_{SS2}.
11. Shows the standard value at oscillating resistor 1MΩ. Determine appropriate oscillating frequency so as not to be in synchronization with the frame frequency and other frequency such as the fluorescent lamps.
12. Shows the wait time from when the power voltage rises to 80 of the specified voltage to when the command input becomes available.
13. The operating voltage range of the booster.
14. Shows the operating voltage range of the LC voltage adjustment circuit, voltage follower, and LCD bias resistor. The operating voltage range differs depending upon each bias setting value. To adjust V5 with the LCD voltage adjustment circuit, it is necessary to set the voltage within the bias voltage. IV5I - IV_{OUT} I ≥ 0.2V.
15. The operating voltage range of the LCD driver after the voltage follower functions. Also, it shows the voltage range of V1 to V5 supplied from the external LCD power supply circuit.
16. Shows the value of the current consumed by the booster, LCD voltage adjustment circuit, voltage follower, LCD bias resistor, and LCD driver. It does not include the value IRREG=V5/(R1+R2+R3) of the current flowing through external resistors R1, R2, and R3. Set the command fine adjustment data to 1000. Outputs the checkered patterns from the LCD drive output pin. The pin is measured at "Open." Current consumption of the IC during display is I_{SSL}+I_{SS1}.
17. The built-in LCD power supply circuit stops when FNC1 and 2 are "H." Current consumption only for the LCD driver. Outputs the checkered patterns from the LCD drive output pin. The pin is measured at "Open." Current consumption of the IC during display is IV5+ I_{SS1}.
    When using the external power supply, stop the built-in power supply circuit which does not need to be operated with pins FNC1 and 2 to prevent the IC from being broken due to a shorting of the internal power supply.
18. The reference voltage differs depending upon the temperature coefficient selected with the corresponding command.
19. Constant current which flows into the LCD Voltage Command Fine Adjustment Circuit of the IC, for the Fine adjustment data (1111).
    Increasing the Fine adjustment data by 1 bit, V5 increases by Rb x I_{REF}/15.
20. For the Chips deliveries, chips are delivered after they satisfy their LCD drive bias voltages are 0.08V in the delivery testing at 25°C.

Timing Characteristics

1. Parallel Interface

1.1 68-Series MPU Read/Write Timing Interface Characteristics

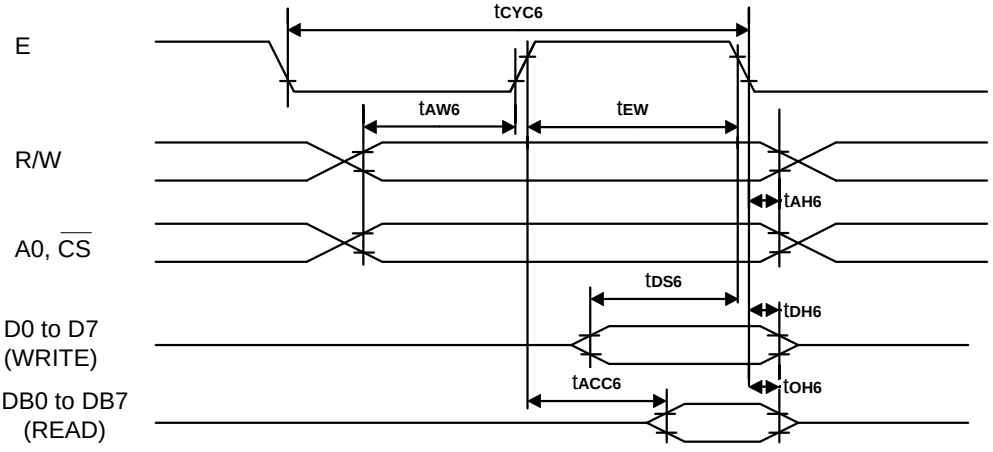
68-Series MPU Read/Write Timing Characteristics (Ta=-30 to 85°C, VDD=+5V±10%)

Signal	Symbol	Designation	Conditions	Min.	Max.	Unit	Note
A0	t_{CYC6}	System Cycle Time		500	-	ns	
$\overline{CS}$, R/W	t_{AH6}	Address Hold Time		20			
	t_{AW6}	Address Setup Time		20			
D0 to D7	t_{DS6}	Data Setup Time		80	-		
	t_{DH6}	Data Hold Time		20	-		
	t_{ACC6}	Access Time	CL=15 pF		90		
	t_{OH6}	Output Disable Time	CL=15 pF	10	60		
E	t_{EW}	Enable Pulse Width	READ	100	-		
			WRITE	80	-		

68-Series MPU Read/Write Timing Characteristics (Ta=-30 to 85°C, VDD=+3V±10%)

Signal	Symbol	Designation	Conditions	Min.	Max.	Unit	Note
A0	t_{CYC6}	System Cycle Time		1000	-	ns	
$\overline{CS}$, R/W	t_{AH6}	Address Hold Time		40	-		
	t_{AW6}	Address Setup Time		40	-		
D0 to D7	t_{DS6}	Data Setup Time		160	-		
	t_{DH6}	Data Hold Time		40	-		
	t_{ACC6}	Access Time	CL=15 pF		180		
	t_{OH6}	Output Disable Time	CL=15 pF	10	120		
E	t_{EW}	Enable Pulse Width	READ	200	-		
			WRITE	160	-		

Note : • Rise/fall time of the input signal is 15 nsec or less.
• Timing is specified at 20% or 80% of the signal waveform.



1.2 80-Series MPU Read/Write Timing Characteristics

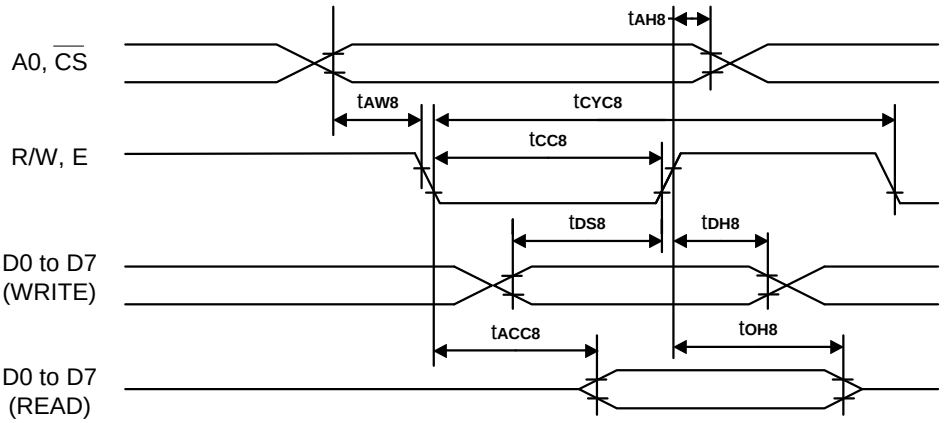
80-Series MPU Read/Write Timing Characteristics (Ta=-30 to 85°C, VDD=+5V±10%)

Signal	Symbol	Designation	Conditions	Min.	Max.	Unit	Note
A0	t_{AH8}	Address Hold Time		20	-	ns	
$\overline{CS}$	t_{AW8}	Address Setup Time		20	-		
R/W, E	t_{CYC8}	System Cycle Time		500	-		
	t_{CC8}	Control Pulse Width		100	-		
D0 to D7	t_{DS8}	Data Setup Time		80			
	t_{DH8}	Data Hold Time		20	-		
	t_{ACC8}	E Access Time	CL=15 pF		90		
	t_{OH8}	Output Disable Time	CL=15 pF	10	60		

80-Series MPU Read/Write Timing Characteristics When VDD=+3V (Ta=-30 to 85°C, VDD=+3V±10%)

Signal	Symbol	Designation	Conditions	Min.	Max.	Unit	Note
A0	t_{AH8}	Address Hold Time		40	-	ns	
$\overline{CS}$	t_{AW8}	Address Setup Time		40	-		
R/W, E	t_{CYC8}	System Cycle Time		1000	-		
	t_{CC8}	Control Pulse Width		200	-		
D0 to D7	t_{DS8}	Data Setup Time		160	-		
	t_{DH8}	Data Hold Time		40	-		
	t_{ACC8}	E Access Time	CL=15 pF		180		
	t_{OH8}	Output Disable Time	CL=15 pF	10	120		

Note : • Rise/fall time of the input signal is 15 nsec or less.
• Timing is specified at 20% or 80% of the signal waveform.



2. Serial Interface

Serial Interface Timing Characteristics (Ta=-30 to 85°C, VDD=+5V±10%)

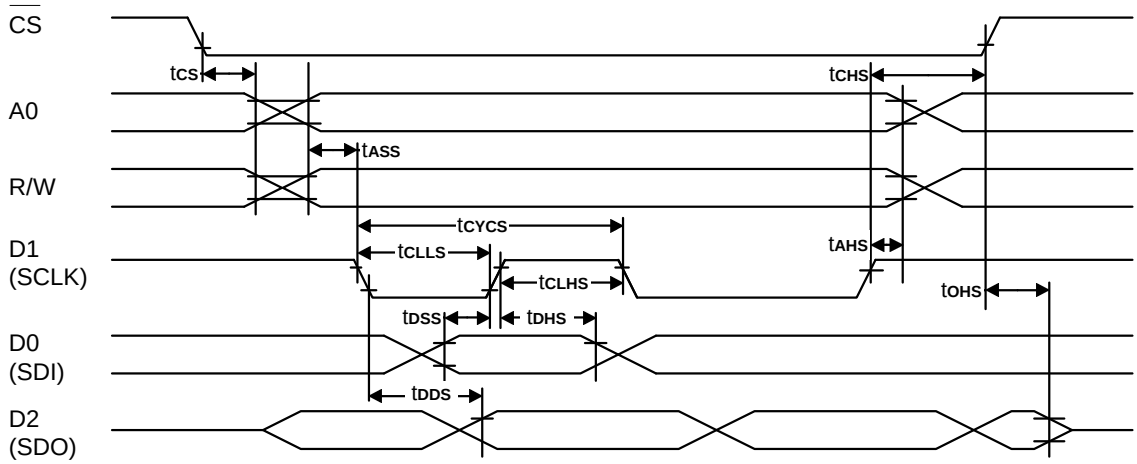
Signal	Symbol	Designation	Conditions	Min.	Max.	Unit	Note
$\overline{CS}$	t_{CSS}	Chip Select Setup Time		50		ns	
	t_{CHS}	Chip Select Hold Time		400			
A0, R/W	t_{ASS}	Address Setup Time		120			
	t_{AHS}	Address Hold Time		200			
D0 (SDI)	t_{DSS}	Data Setup Time		120			
	t_{DHS}	Data Hold Time		50			
D1 (SCLK)	t_{CYCS}	Clock Cycle Time		500			
	t_{CLLS}	Clock L Time		200			
	t_{CLHS}	Clock H Time		200			
D2 (SDO)	t_{DDS}	Data Delay Time	CL=15 pF		90		
	t_{OHS}	Data Disable Time	CL=15 pF	10	60		1

Serial Interface Timing Characteristics (Ta=-30 to 85°C, VDD=+3V±10%)

Signal	Symbol	Designation	Conditions	Min.	Max.	Unit	Note
$\overline{CS}$	t_{CSS}	Chip Select Setup Time		100		ns	
	t_{CHS}	Chip Select Hold Time		800			
A0, R/W	t_{ASS}	Address Setup Time		240			
	t_{AHS}	Address Hold Time		400			
D0 (SDI)	t_{DSS}	Data Setup Time		240			
	t_{DHS}	Data Hold Time		100			
D1 (SCLK)	t_{CYCS}	Clock Cycle Time		1000			
	t_{CLLS}	Clock L Time		400			
	t_{CLHS}	Clock H Time		400			
D2 (SDO)	t_{DDS}	Data Delay Time	CL=15 pF		180		
	t_{OHS}	Data Disable Time	CL=15 pF	10	120		1

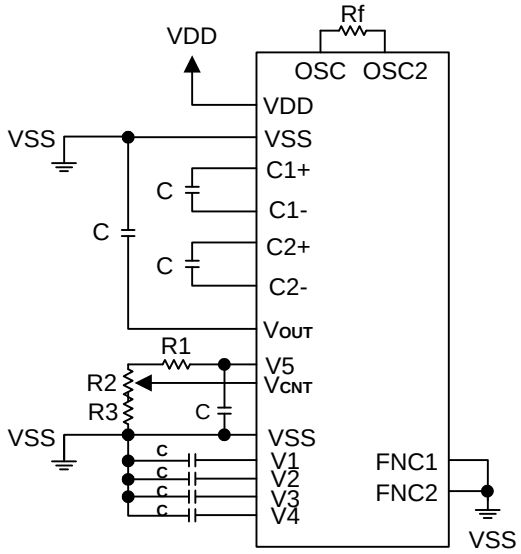
Note : 1. D2(DSO) is high-impedance at the rising edge of the $\overline{CS}$.
2. Rise/fall time of the signal is 15 nsec. or less
3. Timing is specified at 20% or 80% of the signal waveform.

Serial Interface Read/Write Timing Characteristics

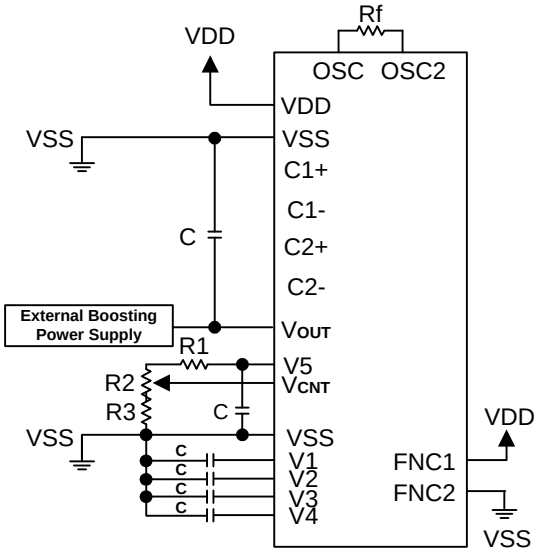


Examples of Applications of LCD Power Supply

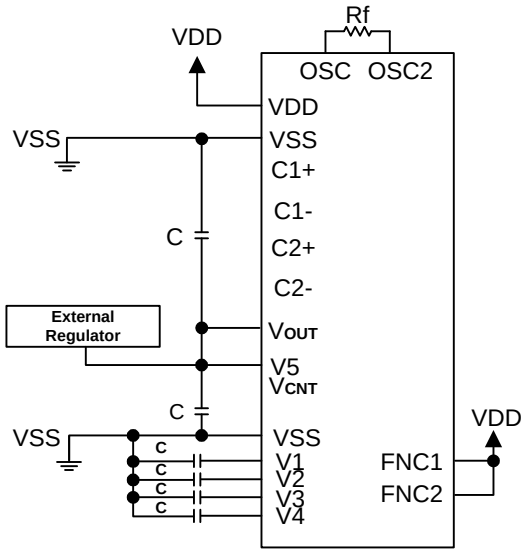
. When Using a Built-in LCD Power Supply Circuit (Triple Boosting)



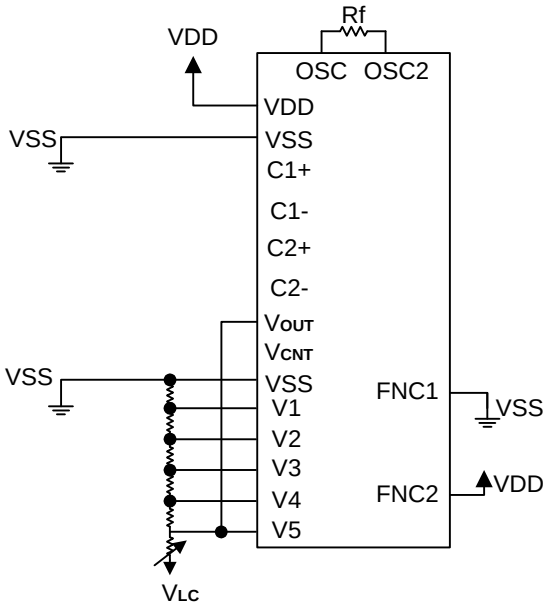
. When Using an External Boosting Power Supply



. When Using an External Regulator



. When Using an External LCD Power Supply



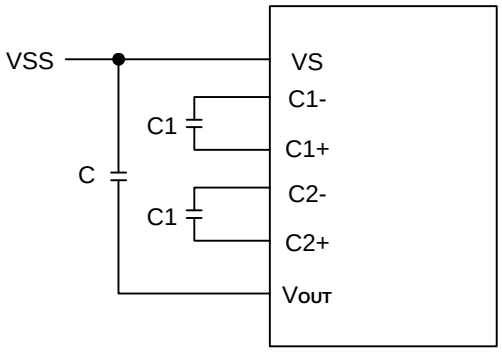
Reference

C : 1.0µF
C1 : 0.47µF
C2 : 0.1µF
C3 : 0.01µF

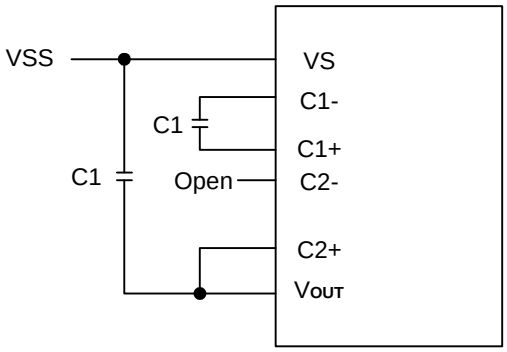
Capacitor C3 connected to V3 pin is recommended 0.01µF

- Booster Capacitor Connection

Tripler



Doubler



Reference

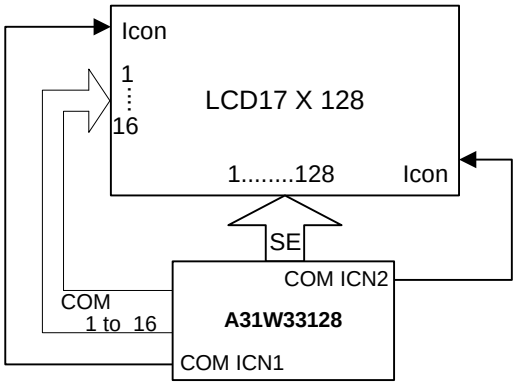
C : 1.0μF

C1 : 0.47μF

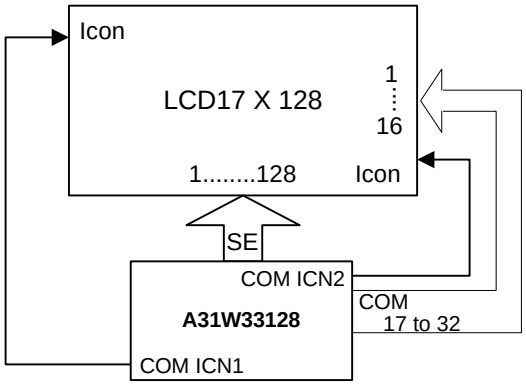
Examples of Connection to LCD Panels

1. 1/17 Duty 17 X 128 Panel

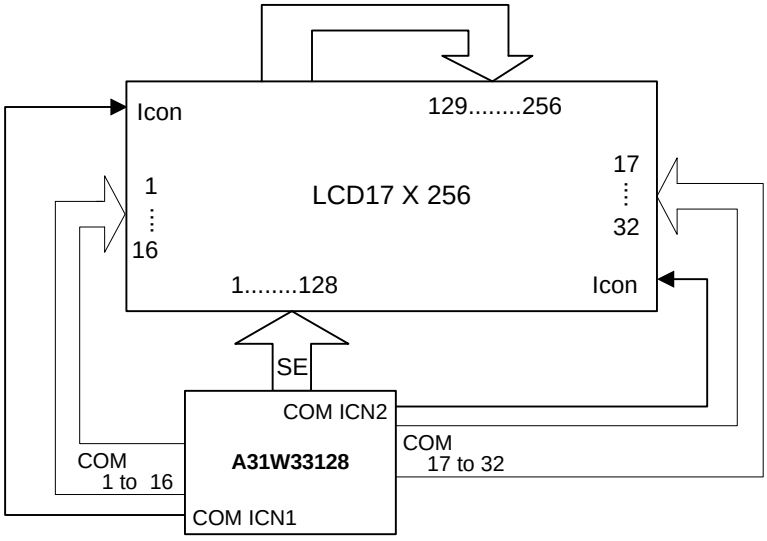
. COM1 to 16 are used:



. COM17 to 32 are used:



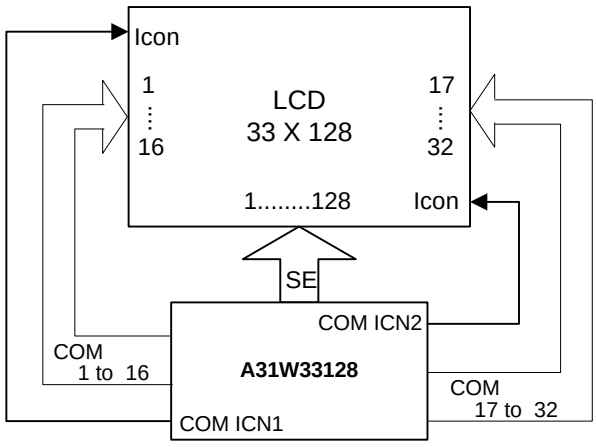
2. 1/33 Duty 17 X 256 Panel



Examples of Connection to LCD Panels (continued)

3. 1/33 Duty 33 X 128 Panel

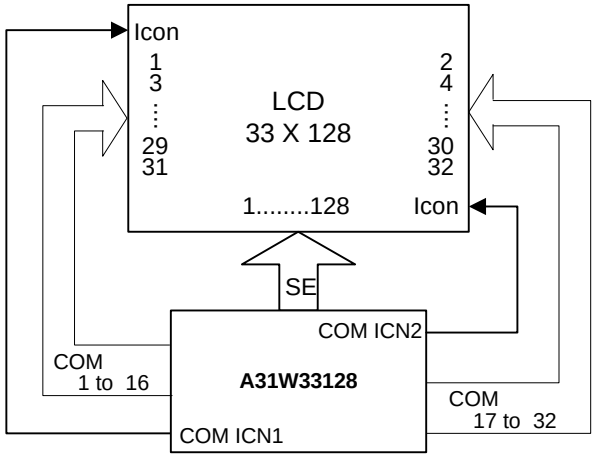
3.1 Normal Common Output



Output in a numerical order of common pin Nos.

3.2 Common Right/Left Alternate Output

Uneven-Numbered Common Line



Even-Numbered Common Line

Ordering Information

Part No.	Package
A31W33128C	COG
A31W33128T	TCP