NEC Electronics Inc.

μPD4216100, 4217100
16,777,216 x 1-Bit Dynamic CMOS RAM

T-46-23-15

Description

The μPD4216100 and the μPD4217100 are fast-page dynamic RAMs organized as 16,777,216 words by 1 bit and designed to operate from a single +5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles.

Two versions of the 16,777,216 x 1-bit DRAM are available. The μPD4216100 version uses 4096 address combinations of A_0 - A_{11} to refresh the memory during a 64-ms refresh period. The μPD4217100 version uses 2048 address combinations of A_0 - A_{10} to refresh the memory during a 32-ms period.

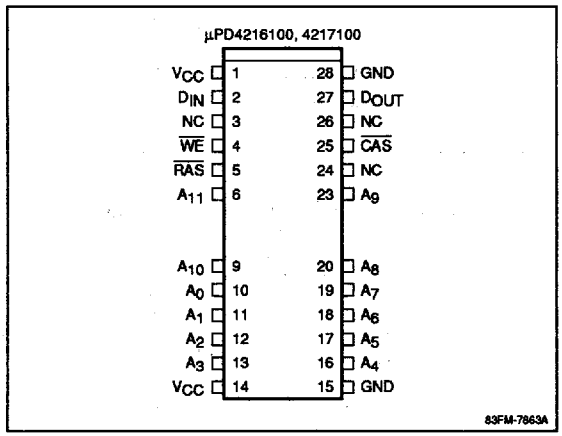
Both versions use row and column address combinations of A_0 - A_{11} for accessing the memory during read, write, and read-modify-write cycles.

Features

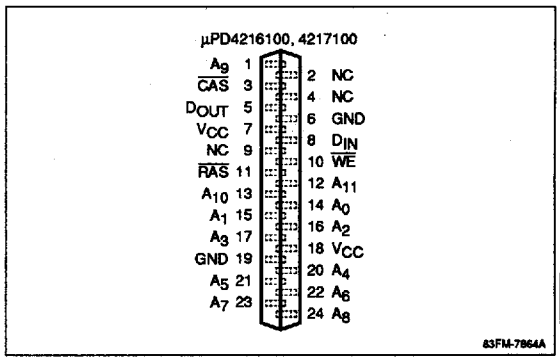
- 16,777,216 by 1-bit organization
- Single +5-volt power supply
- Fast-page option
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 4K refresh cycles every 64 ms (4216100); 2K refresh cycles every 32 ms (4217100)
- 28/24-pin plastic SOJ (400 mil), 24-pin plastic ZIP (475 mil), and 28/24-pin plastic TSOP packaging

Pin Configurations

28/24-Pin Plastic SOJ



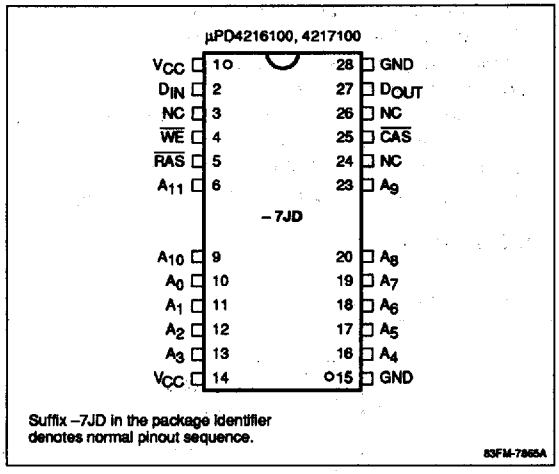
24-Pin Plastic ZIP



8a

Pin Configurations

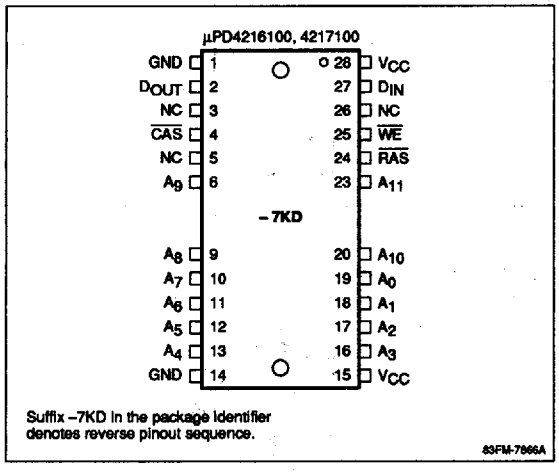
28/24-Pin Plastic TSOP (Normal Pinouts)



Suffix –7JD in the package identifier denotes normal pinout sequence.

83FM-7865A

28/24-Pin Plastic TSOP (Reverse Pinouts)



Suffix –7KD in the package identifier denotes reverse pinout sequence.

83FM-7866A

Pin Identification

Name	Function
A_0 - A_{11}	Address inputs
$\overline{CAS}$	Column address strobe
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	–1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	–55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	–1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Sym	*Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5 (7)	pF	Address, D_{IN}
	C_{I2}	7 (9)	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_O	7 (9)	pF	D_{OUT}

*Values in parentheses are for the ZIP package.

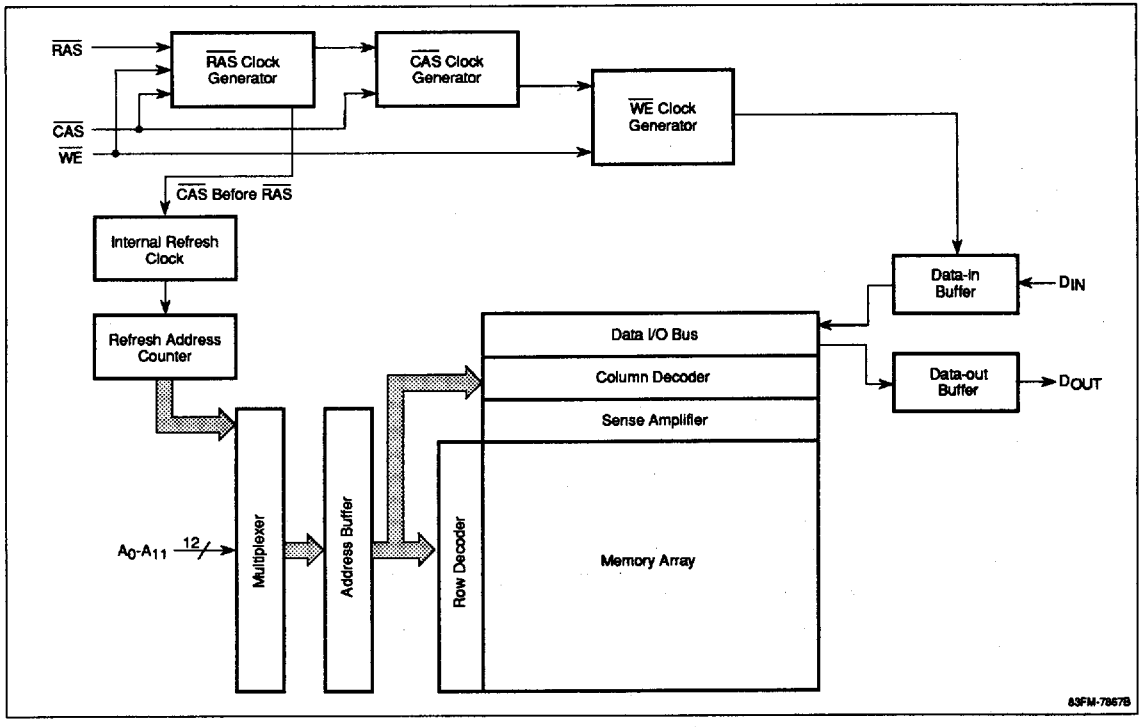
Ordering Information, μPD4216100 (4K Refresh Cycles)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD4216100LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	45 ns	
LE-80	80 ns	150 ns	50 ns	
LE-10	100 ns	180 ns	60 ns	
μPD4216100V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
V-70	70 ns	130 ns	45 ns	
V-80	80 ns	150 ns	50 ns	
V-10	100 ns	180 ns	60 ns	
μPD4216100G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	45 ns	
G5-80	80 ns	150 ns	50 ns	
μPD4216100G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	45 ns	
G5M-80	80 ns	150 ns	50 ns	

Ordering Information, μPD4217100 (2K Refresh Cycles)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD4217100LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	45 ns	
LE-80	80 ns	150 ns	50 ns	
LE-10	100 ns	180 ns	60 ns	
μPD4217100V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
V-70	70 ns	130 ns	45 ns	
V-80	80 ns	150 ns	50 ns	
V-10	100 ns	180 ns	60 ns	
μPD4217100G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	45 ns	
G5-80	80 ns	150 ns	50 ns	
μPD4217100G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	45 ns	
G5M-80	80 ns	150 ns	50 ns	

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
				1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Operating current, average	I_{CC1} (4216100)		90		80		70		60	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; $t_{RC} \geq t_{RC}$ min; I_O = 0 mA (Note 5)
	I_{CC1} (4217100)		110		100		90		80	mA	
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (4216100)		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$; $t_{RC} \geq t_{RC}$ min; I_O = 0 mA (Note 5)
	I_{CC3} (4217100)		110		100		90		80	mA	
Operating current, fast-page cycle, average	I_{CC4} (4216100)		70		60		50		40	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} \geq t_{RC}$ min; I_O = 0 mA (Note 5)
	I_{CC4} (4217100)		70		60		50		40	mA	
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (4216100)		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; $t_{RC} \geq t_{RC}$ min; I_O = 0 mA (Note 5)
	I_{CC5} (4217100)		110		100		90		80	mA	
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		35		40		50		ns	(Note 16)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		15		18		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		15		15		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	18	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	10		10		10		10		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		0		0		ns	(Note 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	5		5		5		5		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	15		18		20		25		ns	(Note 16)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	10		15		15		20		ns	(Note 15)

8a

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Fast-page read-modify-write cycle time	t_{PRWC}	60		65		75		85		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	100	125,000	ns	
Random read or write cycle time	t_{RC}	110		130		150		180		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 10)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		64		64		64		64	ms	(Note 18)
	t_{REF}		32		32		32		32	ms	(Note 19)
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		55		ns	
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		70		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5		5		5		5		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	15		18		20		25		ns	
Read-write cycle time	t_{RWC}	135		155		175		210		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		70		80		100		ns	(Note 16)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	10		10		15		20		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		20		ns	
Write command pulse width	t_{WP}	10		10		15		20		ns	(Note 14)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{WE}$ setup time	t_{WSR}	10		10		10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(11) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

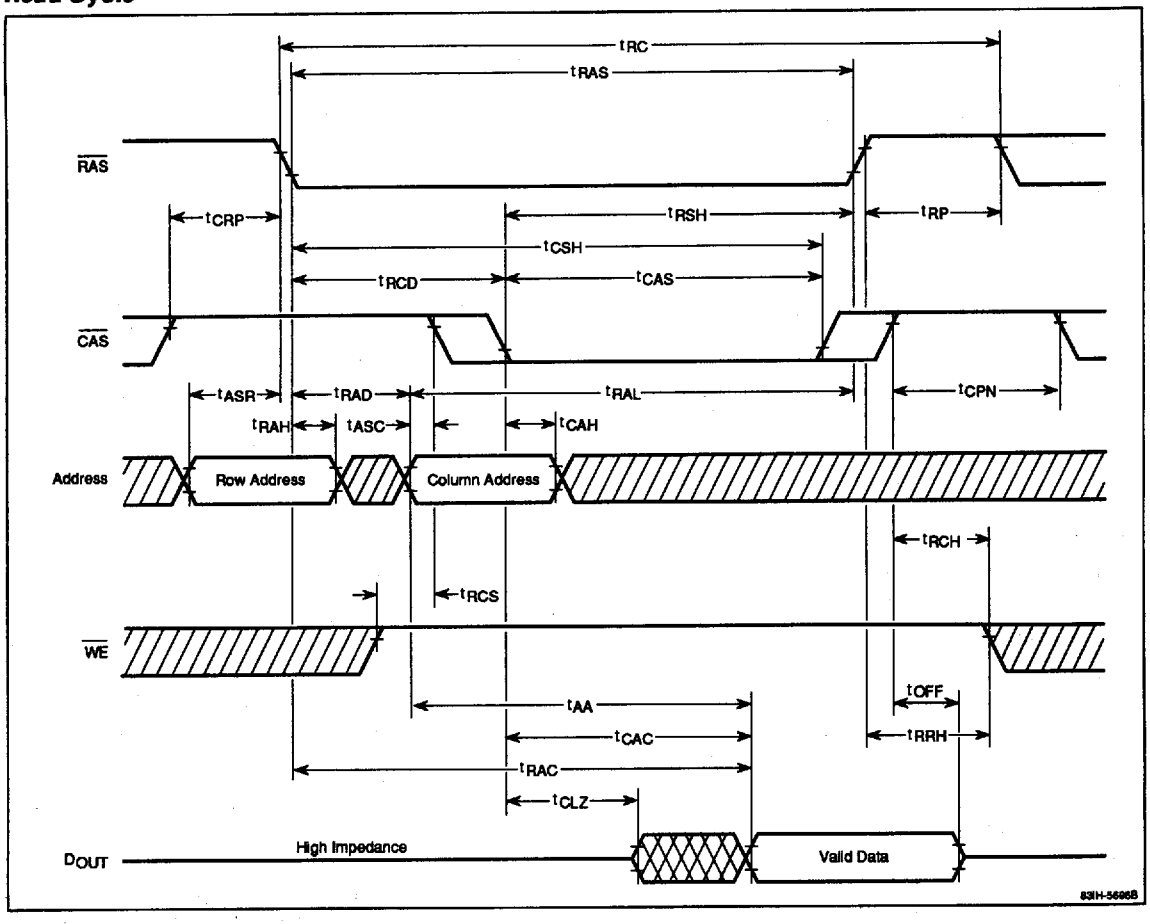
(17) Assumes that the test mode has been set. A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may be inadvertently initiated during power up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power up sequence to ensure normal device operation. Contact your NEC Electronics sales representative for more details.

(18) The μPD4216100 RAS-only refresh (ROR) cycle uses 4096 external row address combinations of A_0 - A_{11} to refresh the memory during a 64-ms refresh period (t_{REF}). Row and column address combinations of A_0 - A_{11} are used to access the memory during read, write, and read-modify-write cycles. CBR ($\overline{CAS}$ before $\overline{RAS}$) and hidden CBR refresh cycles use 4096 internal row address combinations of A_0 - A_{11} to refresh the memory during a 64-ms refresh period (t_{REF}).

(19) The μPD4217100 RAS-only refresh (ROR) cycle uses 2048 external row address combinations of A_0 - A_{10} to refresh the memory during a 32-ms refresh period (t_{REF}). Row and column address combinations of A_0 - A_{10} are used to access the memory during read, write, and read-modify-write cycles. CBR ($\overline{CAS}$ before $\overline{RAS}$) and hidden CBR refresh cycles use 2048 internal row address combinations of A_0 - A_{10} to refresh the memory during a 32-ms refresh period (t_{REF}).

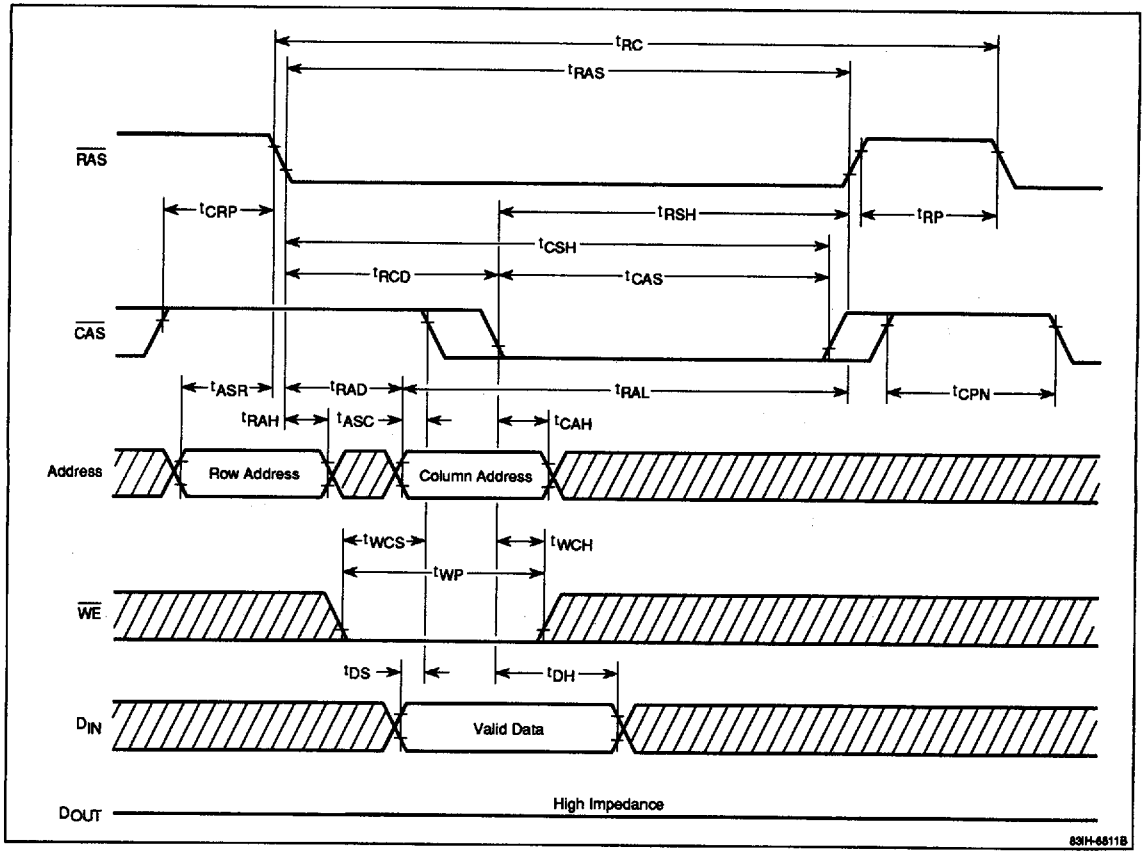
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

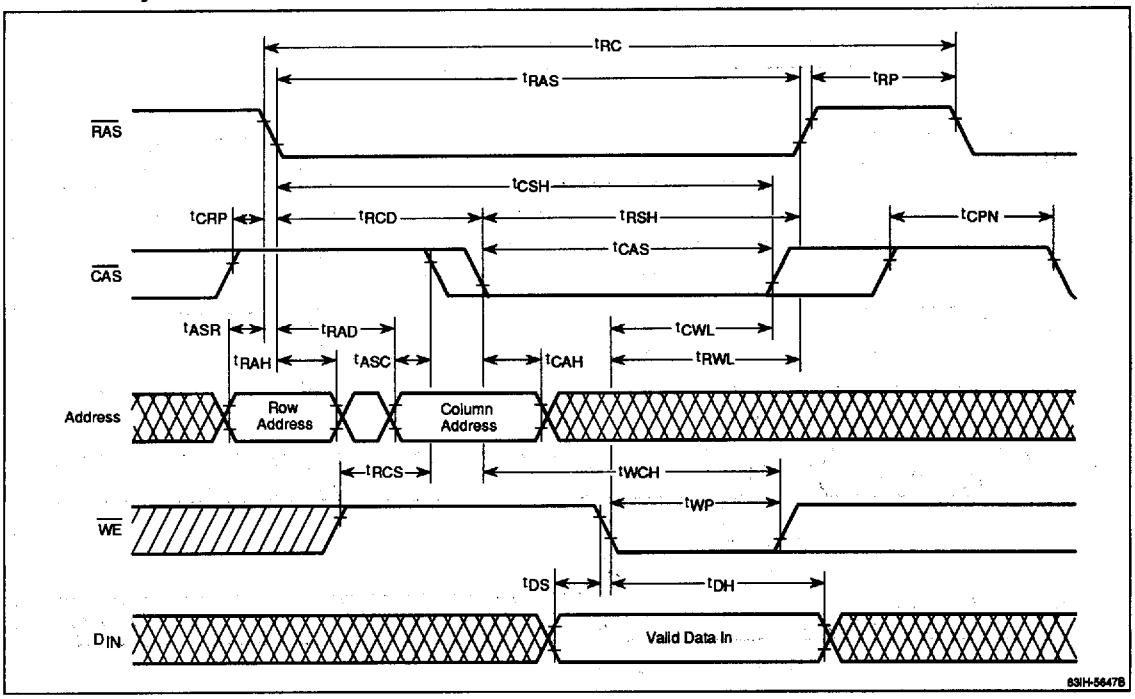
Early Write Cycle



8a

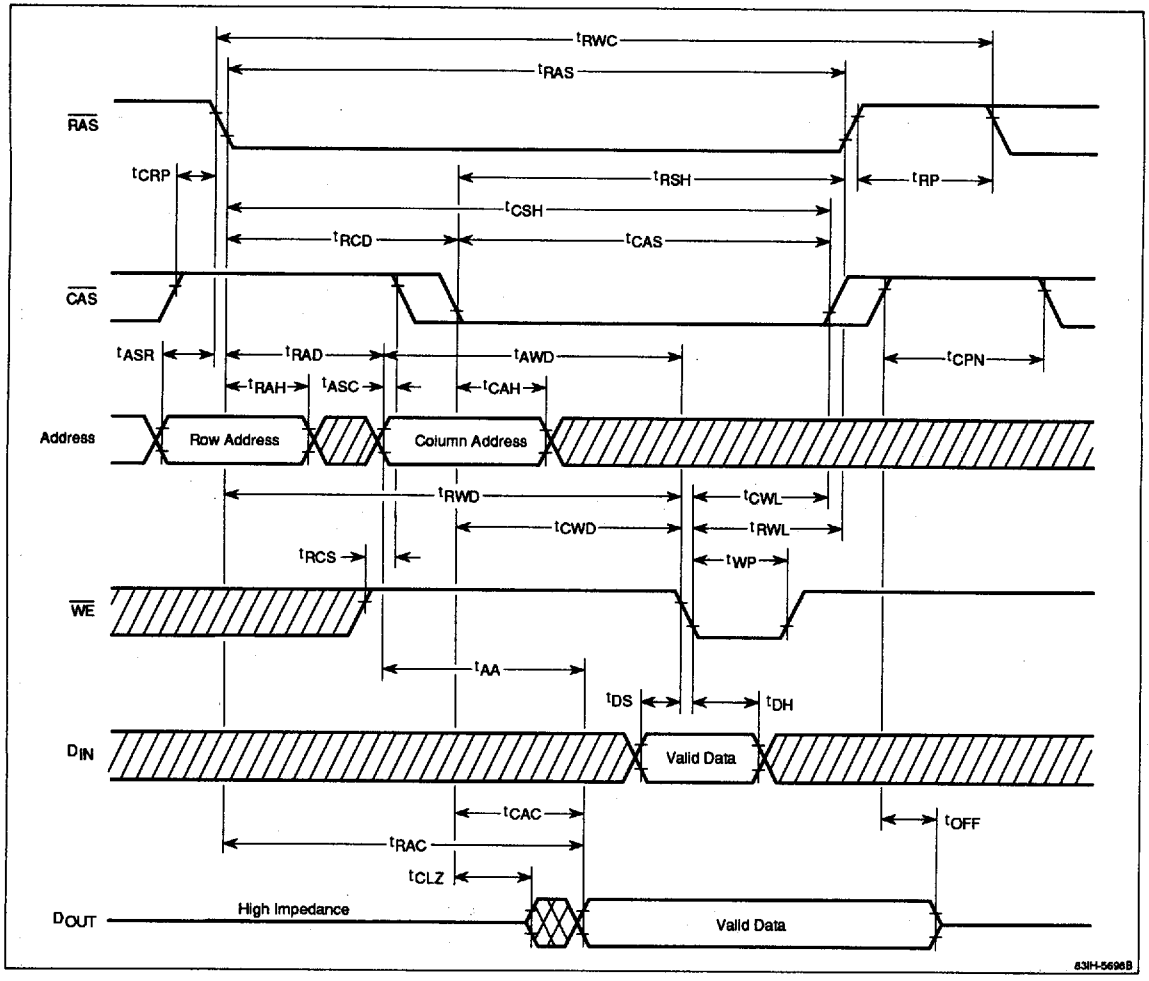
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

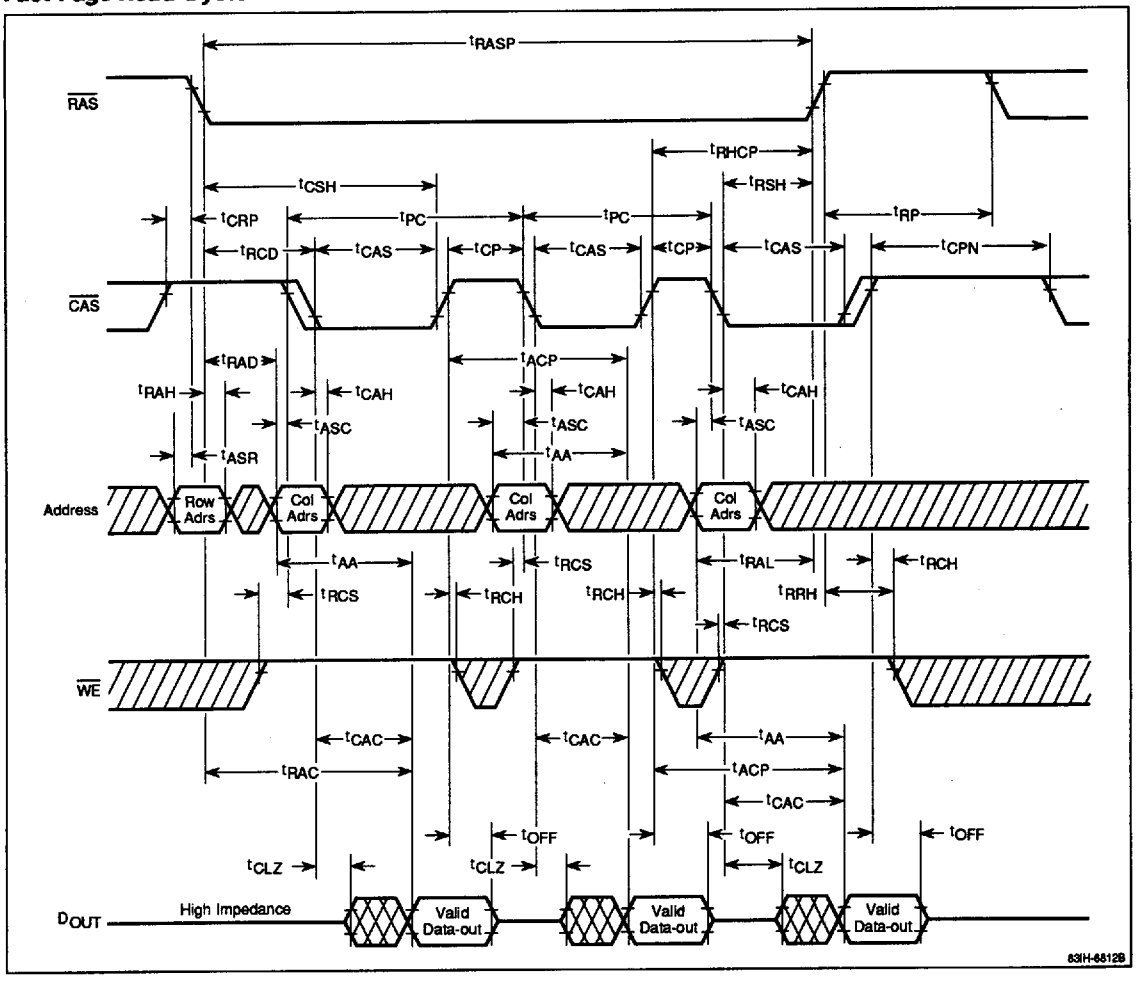
Read-Write/Read-Modify-Write Cycle



8a

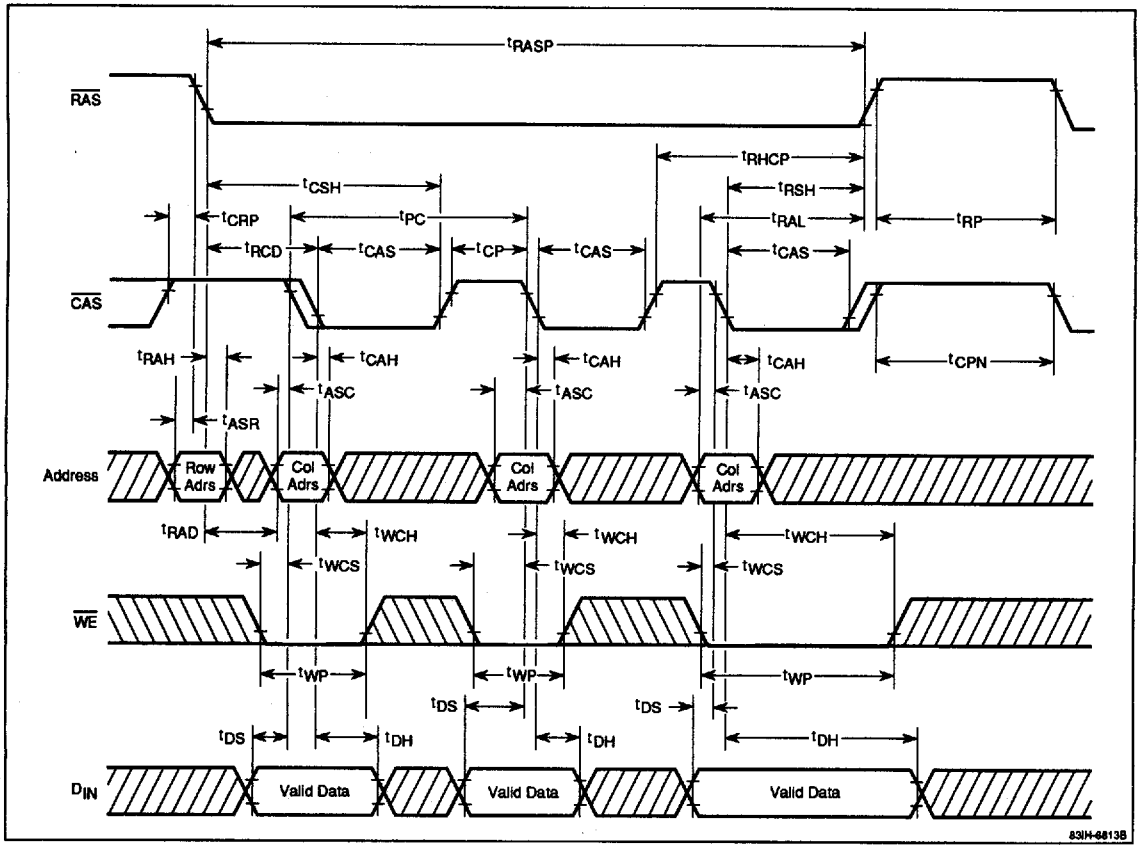
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

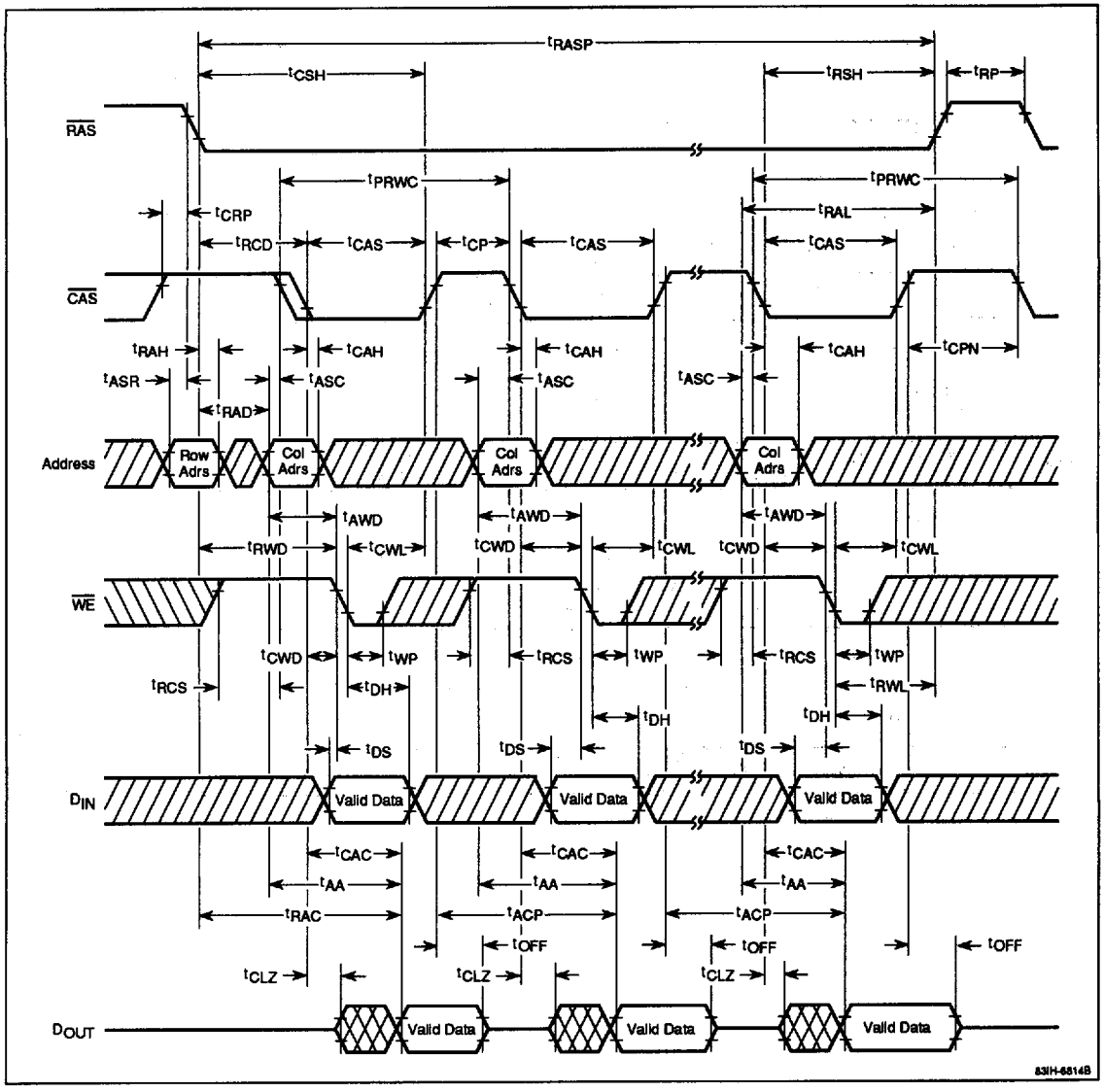
Fast-Page Early Write Cycle



8a

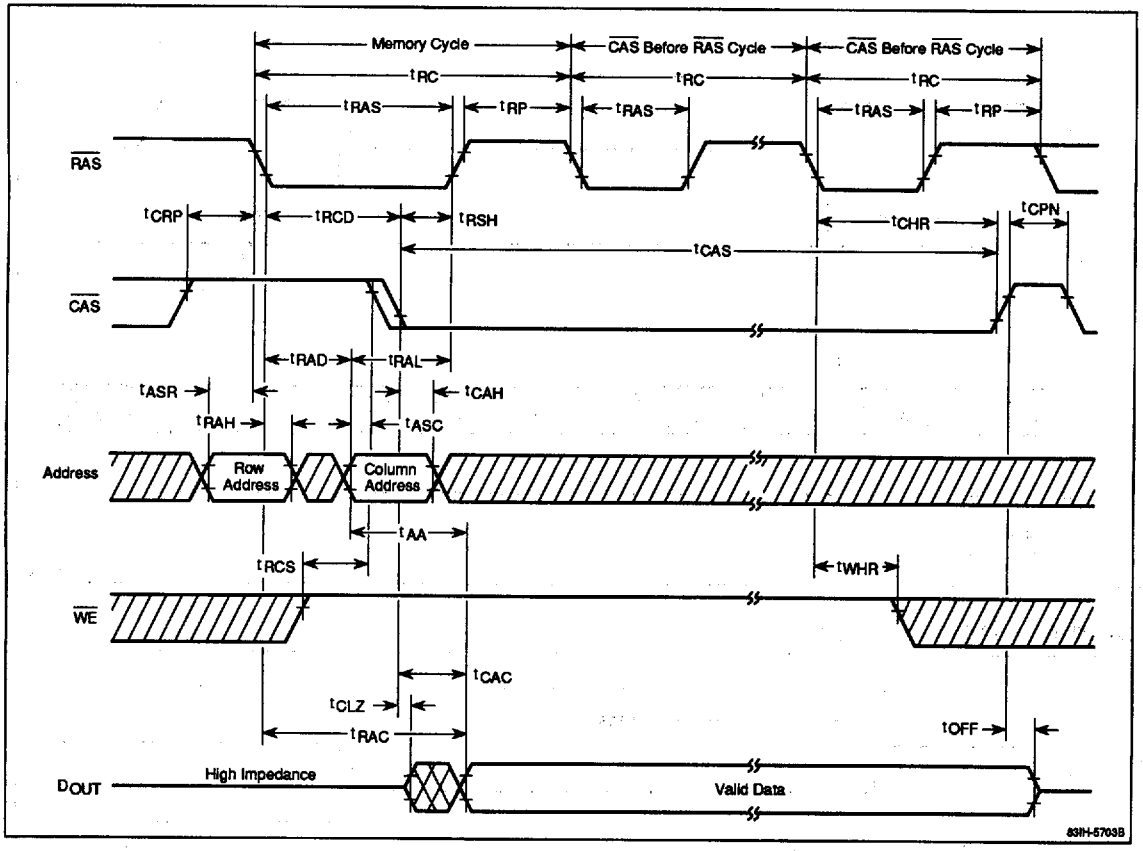
Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



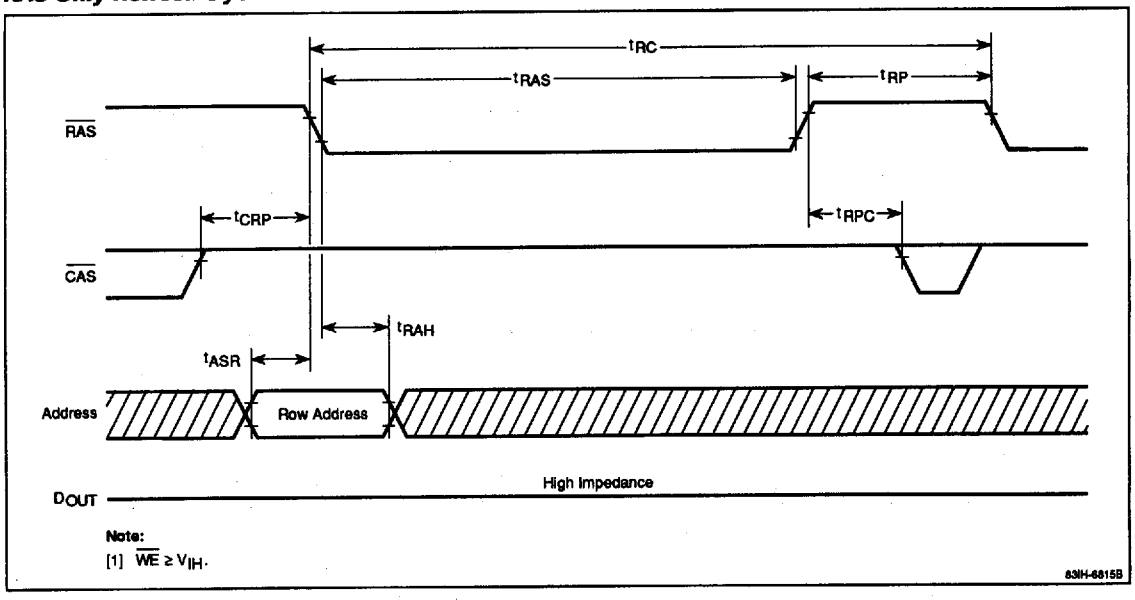
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

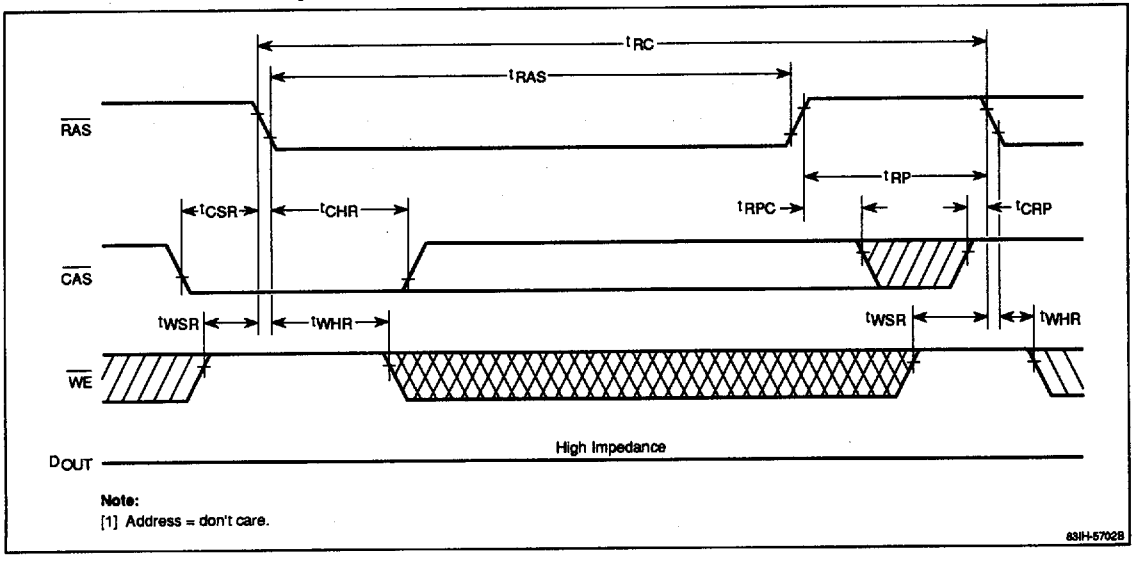
RAS-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6815B

CAS Before RAS Refresh Cycle



Note:
[1] Address = don't care.

83IH-5702B