TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TMP04060F-XXX(JTMP04060-XXXS)

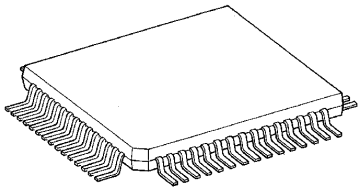
CMOS 4-BIT LL MICROCONTROLLER (LL : LOW POWER CONSUMPTION & VOLTAGE OPERATION MICROCONTROLLER)

◆ OUTLINE

The TMP04060F-XXX is an advanced microcontroller developed for applications in multi-digit calculators and LCD remote controllers.

It is a 4-bit CMOS LL microcontroller with integrated a 4-bit high-performance CPU, memory (static work RAM, data RAM and program ROM). LCD display LL controller driver, and a multi-function timer into single-chip.

The basic features are as follows.



LQFP60-P-1414-0.80

Weight : g (Typ.)

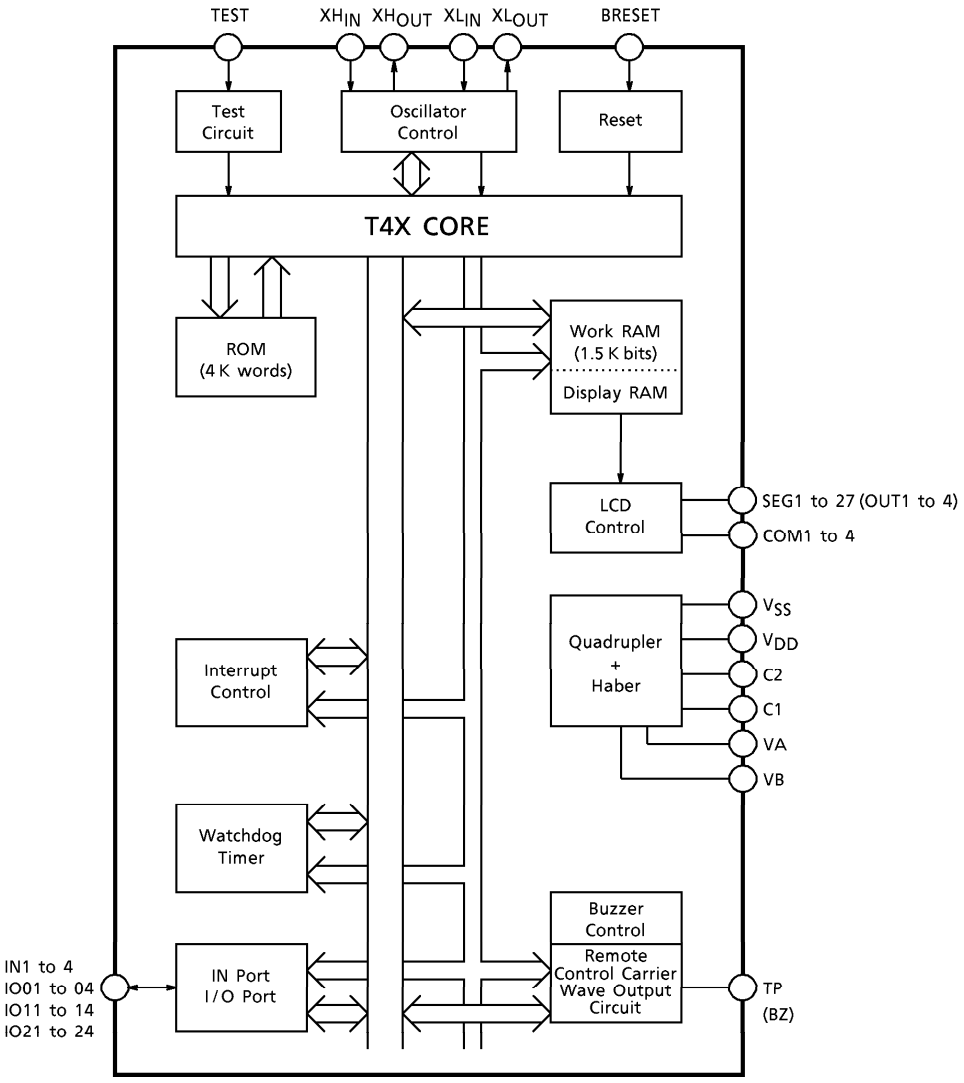
◆ FEATURES

- Number of instructions : 56
- Minimum instruction execution time : 61 μs (at 32.768 kHz)
  1 μs (at 2 MHz / 3.0 V)
- Oscillating circuit :

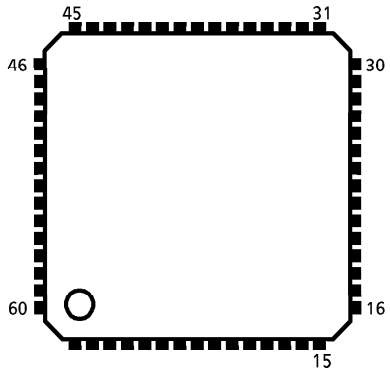
USE	POWER SUPPLY VOLTAGE	HIGH-SPEED OSCILLATOR	LOW-SPEED OSCILLATOR
Calculator	1.5 V	internal CR (78 kHz)	internal C (16 kHz)
	3.0 V	internal CR (1.1 MHz)	internal C (30 kHz)
Remote controller	3.0 V	—	36.864 kHz (X'tal)
	3.0 V	2 MHz (X'tal)	32.768 kHz (X'tal)
	3.0 V	455 kHz (X'tal)	32.768 kHz (X'tal)

- Built-in ROM size : 4 K words (1 word = 16 bits)
- Built-in RAM size :
  Work RAM : 384 × 4 bits
- Input pins : 4 pins (with interrupts)
- I/O pins : 12 pins (Output pins for key strobe)
- Output pins : 1 pin (carrier wave output)
- Interruption : 2 external system (input pins, general-purpose I/O pin)
  1 internal system (timings)
- LCD display driver controller : 27 seg × 4 com
- Built-in LCD driver power circuit
- Watchdog timer

Block Diagram



Pin Assignment



PIN No.	PIN NAME
1	C1
2	C2
3	V_{SS}
4	BRESET
5	XL_{IN}
6	XL_{OUT}
7	V_{DD}
8	XH_{IN}
9	XH_{OUT}
10	TEST
11	TP
12	IN1
13	IN2
14	IN3
15	IN4
16	IO01
17	IO02
18	IO03
19	IO04
20	IO11
21	IO12
22	IO13
23	IO14
24	IO21
25	IO22
26	IO23
27	IO24
28	S27 (OUT4)
29	S26 (OUT3)
30	S25 (OUT2)

PIN No.	PIN NAME
31	S24 (OUT1)
32	S23
33	S22
34	S21
35	S20
36	S19
37	S18
38	S17
39	S16
40	S15
41	S14
42	S13
43	S12
44	S11
45	S10
46	S9
47	S8
48	S7
49	S6
50	S5
51	S4
52	S3
53	S2
54	S1
55	COM4
56	COM3
57	COM2
58	COM1
59	VA
60	VB

Pin Description

PIN NAME	FUNCTION
V_{DD}	Power supply (+)
V_{SS}	Power supply (−)
VA, VB	Boosted voltage output
C1 to C2	Capacitor pin for LCD booster
XH_{IN} to XH_{OUT}	Crystal / resister connection pin for high-speed oscillator
XL_{IN} to XL_{OUT}	Crystal connection pin for low-speed oscillator
IN1 to IN4	Input port (with interruption)
IO01 to IO04	I/O port (with interruption)
IO11 to IO14	I/O port
IO21 to IO24	I/O port
SEG1 to SEG27	LCD segment output (SEG24 to SEG27 are also used as OUT1 to OUT4)
COM1 to COM4	LCD common output
TP	Carrier wave output for remote control (in common with buzzer output)
BRESET	Reset input (low active)
TEST	Test input

◆ MEMORY MAP

1. Program ROM

Program ROM consists of 16 bits per 1 word. Op-code and operand are executed in one word units. Program ROM consists of 4 K words per page.
This program ROM area can be used for constant data ROM. In this case, it can be used in byte units (1 byte = 8 bits).

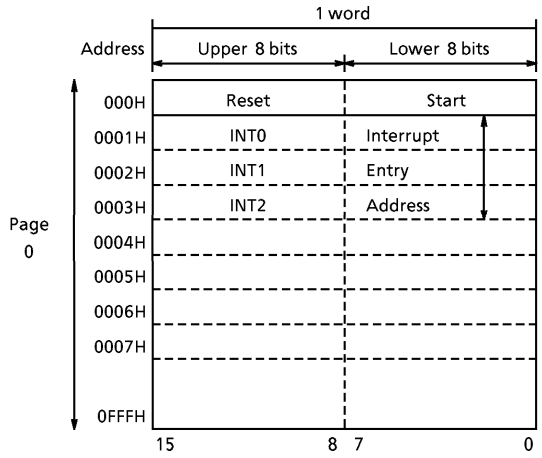


Fig.1 Program memory map

(Note) : Use the CALL instruction to write the interrupt entry address. Write NOP for unused interrupts.

```
Example : CALL A : INT0
          NOP    : INT1
          CALL B : INT2
```

2. Work RAM

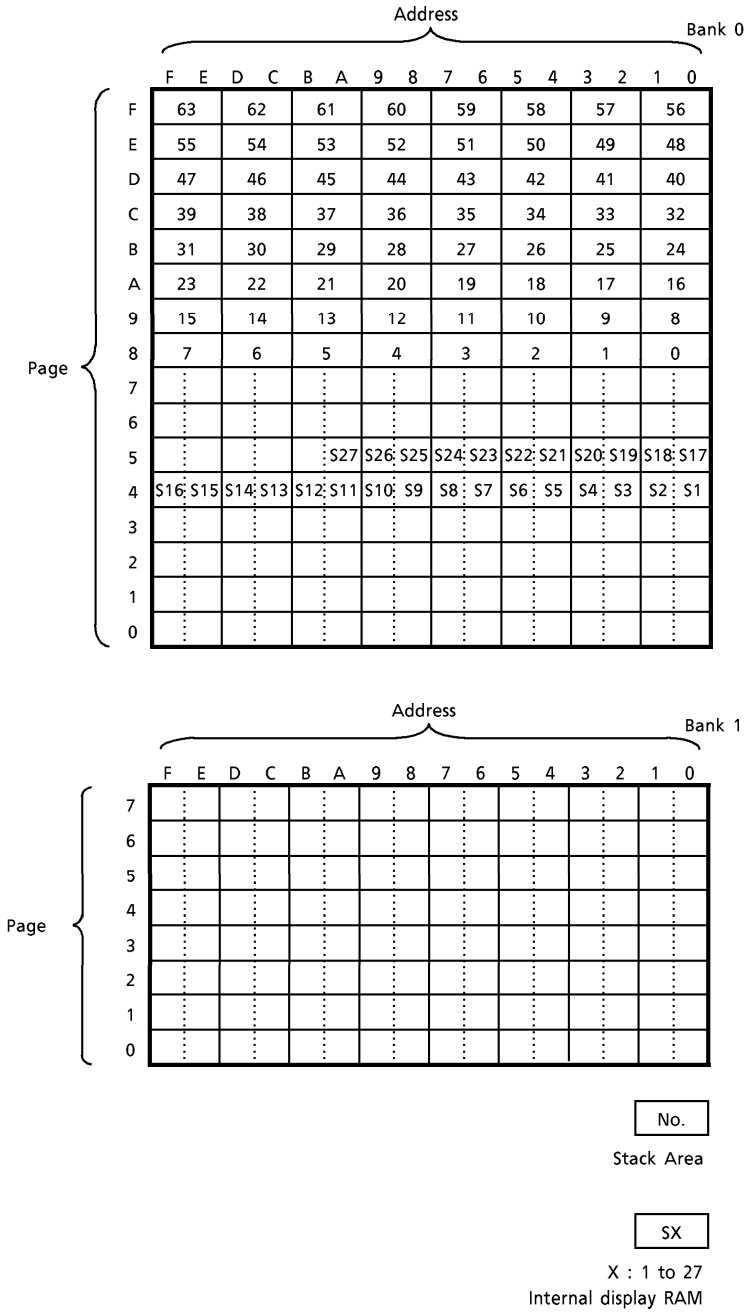


Fig.2 Work RAM

≪not supported : bank 1≫

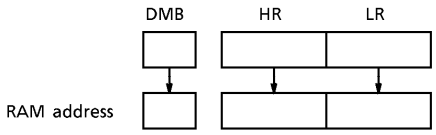
Note that pages 8 to F of the bank do not exist. Don't try to use them.

Bank 0 of Work RAM consists of 256 × 4 bits.
Bank 1 of Work RAM consists of 128 × 4 bits.
R / W is performed at the address specified by bellows.

(1) Indirectly addressing mode (Fig.3 (a))

DMB in F-reg, H, L-reg specify the Work RAM address.
(DMB : bank, H-reg : page, L-reg : address)

LD A, M : A←RAM (HL)

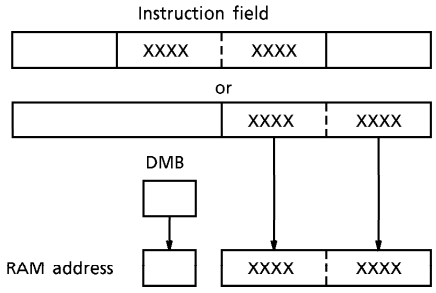


(a) Indirectly addressing

(2) Directly addressing mode (Fig.3 (b))

Immediate data (8 bits) in instruction specify the Work RAM page and address.
Bank is specified by DMB in F-reg.

LD 2CH, 0AH : RAM (2CH)←AH

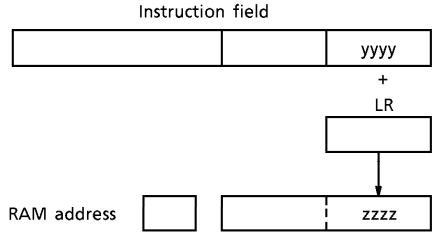


(b) Directly addressing

(3) Index addressing mode (Fig.3 (c))

Address (L-reg) is specified by the immediate data (4 bits) in instruction, and the other immediate data specify Page.

LDRI 4H, 3H : RAM (HL + 4H)
←RAM (3H, L)
L←L + 1, A←A − 1



(c) Index addressing

Fig.3 Addressing mode

2-1. Stack RAM area

BANK 0, PAGE 8 to F area can be used as Stack area.
When using the "CALL / CALLS" instruction or start the interruption routine, the data of program counter and Program memory bank are stored in Stack area.
Then, using "RET" instruction, program return according to those data.
And, using "PUSH" instruction, 8 bits data in a pair register can be stored in Stack area.
Then, using "POP" instruction, those data are returned to the register.
Maximum Stack area is 64 (0 to 63), and each Stack area consist of 8 bits.

2-2. Display RAM area

Banks 0, page 4, and 5 (addresses 0 to A) can also be used as display RAM.

	3	2	1	0
PC6	—	(EXO)	DON	DSTA
R / W	—	R / W	W	W
Initial Value	—	0	0	0

The display RAM area is structured as shown below :

	Address	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	Bank 0	CCCC OOOO MMMM 4321	CCCC OOOO MMMM 4321	←	←	←	←	←	←	←	←	←	←	←	←	←	CCCC OOOO MMMM 4321
Page	5						S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17
	4	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1

DATA write for display RAM only 4-bit transfer instructions available.

REGISTER FILE

Register files consist of 1. general-purpose registers and 3. peripheral I/O registers.

1. General register

1.1 Flag Register : F-Register (PAGE / AD = 0 / 0)

	3	2	1	0
R00	DMB0	DMB1	ZF	CF
R / W	R / W	R / W	R / W	R / W
Initial Value	—	—	—	—

CF : Carry Flag
ZF : Zero Flag
DMB0 : Work RAM Bank
DMB : Always set to "0".

1-2. Accumulater register : A-register (PAGE / AD = 0 / 1)

1-3. H.L register (PAGE / AD = 0 / 3 to 2)
H.L Register are used for Work RAM address setting with DMB.

H Register

	3	2	1	0
R03	HR3	HR2	HR1	HR0
R / W	R / W	R / W	R / W	R / W
Initial Value	—	—	—	—

Work RAM page

L Register

	3	2	1	0
R02	LR3	LR2	LR1	LR0
R / W	R / W	R / W	R / W	R / W
Initial Value	—	—	—	—

Work RAM address

1-4. Bank register (PAGE / AD = 0 / 7) : B-register
B-Register is used for ROM Page.

* TMP04060F has only page 0 (0000. Do not use the upper page.

	3	2	1	0
R07	BR3	BR2	BR1	BR0
R / W	R / W	R / W	R / W	R / W
Initial Value	—	—	—	—

1-5. D-register, E-register, P-register
General-purpose register. (PAGE / AD = 0 / 5, 0 / 4, 0 / 6)
When using ROM as Data Table Function, B, P, D and E-Register are used for ROM address setting.
(Data table function : user can use ROM area for store the constant, and can access those constant by LDBL or LDBH instruction.)

ADDRESS			0		1		2		3		4		5		6		7	
PAGE (RFB)	8 BIT ADDRESS		0				2				4				6			
			LOWER 4 BIT		UPPER 4 BIT		L 4 BIT		H 4 BIT		L 4 BIT		H 4 BIT		L 4 BIT		H 4 BIT	
	R / W		READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE
0	MSB	BIT3	F REGISTER		A REGISTER		L REGISTER		H REGISTER		E REGISTER		D REGISTER		P REGISTER		B REGISTER	
		BIT2																
		BIT1																
	LSB	BIT0																
1	MSB	BIT3	STACK POINTER (SP)		0		INT2				IOD14	IOO14	IOD24	IOO24				
		BIT2					INT1				IOD13	IOO13	IOD23	IOO23				
		BIT1					INT0				IOD12	IOO12	IOD22	IOO22				
	LSB	BIT0	0				0				IOD11	IOO11	IOD21	IOO21				
2 (PAx)	MSB	BIT3	IND04		IOD04	IOO04												RST
		BIT2	IND03		IOD03	IOO03									LOWCP			
		BIT1	IND02		IOD02	IOO02					WDT2				CPMODE2			
	LSB	BIT0	IND01		IOD01	IOO01					WDT1				CPMODE1			
3 (PBx)	MSB	BIT3																
		BIT2																
		BIT1																
	LSB	BIT0																
4 (PCx)	MSB	BIT3			IIN4		IIE4											
		BIT2	ESELT		IIN3		IIE3						BZSEL		EXO			
		BIT1	ESELIO		IIN2		IIE2						BZ1			DON		
	LSB	BIT0	ESELI		IIN1		IIE1		IOIE0				BZ0			DSTA		
5 (PDx)	MSB	BIT3	TI4						TIE4		OO34				CARRY3		CARRY7	
		BIT2	TI3						TIE3		OO33		INR		CARRY2		CARRY6	
		BIT1	TI2						TIE2		OO32		TPCNT		CARRY1		CARRY5	
	LSB	BIT0	TI1						TIE1		OO31		IB		CARRY0		CARRY4	

Fig.6 Register file

(Note) : Blank columns are indeterminate.

◆ **PERIPHERAL CIRCUIT**

Each peripheral circuits can be accessed (Read / Write / Circuit setting) by Register files.

1. Oscillator block

1-1. Dual-clock specifications (system where both high-speed and low-speed oscillators are used)

	3	2	1	0
PA6	—	LOWCP	CPMODE2	CPMODE1
R / W	—	R / W	R / W	R / W
Initial Value	—	0	1	1

The CPU clock is generated by the asynchronous oscillator switching circuit which has low-speed and high-speed clock oscillator circuit.
This block also provides the clock for the timer circuit, LCD driver, Quadrupler.
Oscillation mode is controlled by Register file CPMODE1 and CPMODE2 (PAGE / AD = 2 / 6), as follows.

CPMODE 1	CPMODE 2	LOW-SPEED OSC	HIGH-SPEED OSC	SYSTEM CP	MODE NAME
0	0	OFF	OFF	OFF	(CPM0)
1	0	ON	OFF	Low speed	(CPM1)
0	1	OFF	ON	High speed	(CPM2)
1	1	ON	ON	High speed	(CPM3)

CPMODE 1 and 2 are initially 1 (CPM3)

LOWCP is the display clock control bit. When LOWCP is set to 1, Low-speed OSC clock is supplied to LCD circuit. LOWCP is initially "0". Even if LOWCP is set to 1, clock cannot be occupied to display circuit during Low-speed OSC stopped, and display cannot be shown.
Low-speed OSC circuit can select X'tal or internal CR oscillation by Mask option.
High-speed OSC circuit can select X'tal or external CR oscillation by Mask option.

Oscillator types depending on use

USE	POWER SUPPLY VOLTAGE	HIGH-SPEED OSC	LOW-SPEED OSC
Calculator	1.5 V	Internal CR (78 kHz)	Internal C (16 kHz) <External R>
	3.0 V	Internal CR (1.1 MHz)	Internal C (30 kHz) <External R>
Remote controller	3.0 V	X'tal (2 MHz)	X'tal (32.768 kHz)
	3.0 V	X'tal (455 kHz)	X'tal (32.768 kHz)

Setting a register to CPM1 and executing a HALT instruction sets the mode to Halt (system CP off, high-speed oscillator off, low-speed oscillator on). Setting a register to CPM0 and executing a HALT instruction sets the mode to Stop (system CP off, high-speed oscillator and low-speed oscillators off). Even if, mode is changed to MODE 0 from MODE 1 / 2 / 3, there are no changing until use HALT instruction.

The High / Low-speed OSC circuit has WARM UP function.

The low-speed oscillation does not have enough warm-up time, therefore, when the oscillation is started, software need to make warming up time enoughly.

When the System CP is changed between Low and High (CPM1→CPM2 / 3 or CPM2→CPM1), changing System CP waits to finish the warming up time.

Also that until the system CP is changed, instructions are executed with the previous system CP.

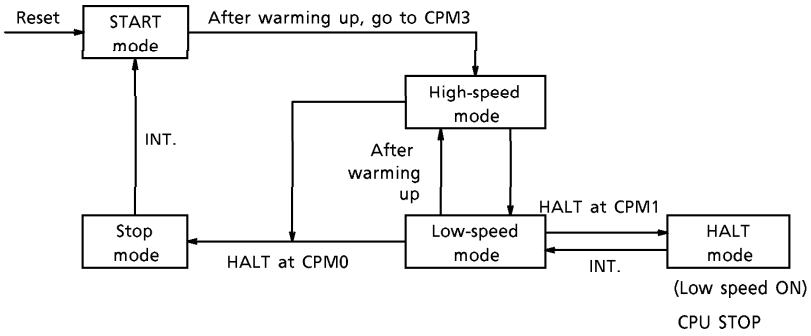


Fig.5 Mode status

The reset for this Divider circuit is done by Register file RST1 (PA7W).

	3	2	1	0
PA7W	RST	—	—	—
R / W	W	—	—	—
Initial Value	0	—	—	—

RST : Binary counter reset

(Note 1) : Do not set System CP to low-speed when the Low-speed OSC is not in operation or before stable.
(Note 2) : Do not set System CP to high-speed when the High-speed OSC is not in operation or before stable.
(Note 3) : When using a crystal oscillator for low-speed oscillation, do not change to STOP mode.

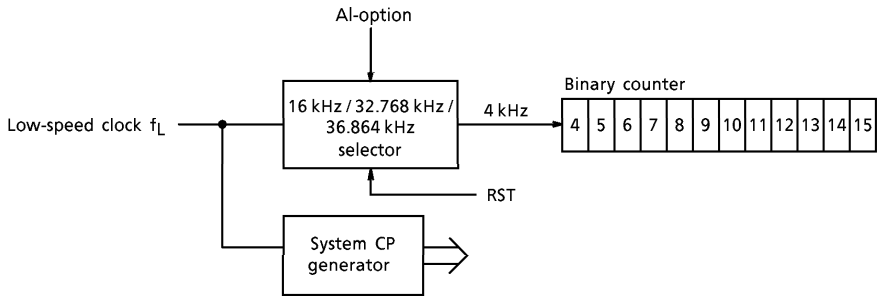


Fig.6 Divider circuit

Example 1

START mode (After warming up, program start at address 0000.)
↓
CPM3 (High / Low speed ON, SYSCP = High, LOWCP OFF)
↓ LD 26O, 7H
CPM3 (High / Low speed ON, SYSCP = High, LOWCP ON)
↓ LD 26O, 4H
CPM0 (High / Low speed ON, SYSCP = High, LOWCP ON)
(There are no change after shift to CPM0)
↓ HALT
STOP mode (High / Low-speed OSC, STOP, SYSCP OFF, LOWCP OFF)

When an interruption occurs, the mode is changed to START mode and program start at the address which is decided by each interruption (refer to Fig.1).

Example 2

START mode (After warming up, program start at address 0000.)
↓
CPM3 (High / Low speed ON, SYSCP = High, LOWCP OFF)
↓ LD 26O, 5H
CPM1 (Low speed ON, SYSCP = Low, LOWCP ON)
↓ HALT
HALT mode (High-speed OSC OFF, Low-speed OSC ON, SYSCP OFF, LOWCP ON)

When an interruption occurs, the mode is changed to slow mode (CPM1) and program start at the address which is decided by each interruption.

Example 3

START mode (After warming up, program start at address 0000.)

↓

CPM3 (High / Low speed ON, SYSCP = High, LOWCP OFF)

↓ LD 26O, 7H

CPM3 (High / Low speed ON, SYSCP = High, LOWCP ON)

↓ LD 26O, 4H

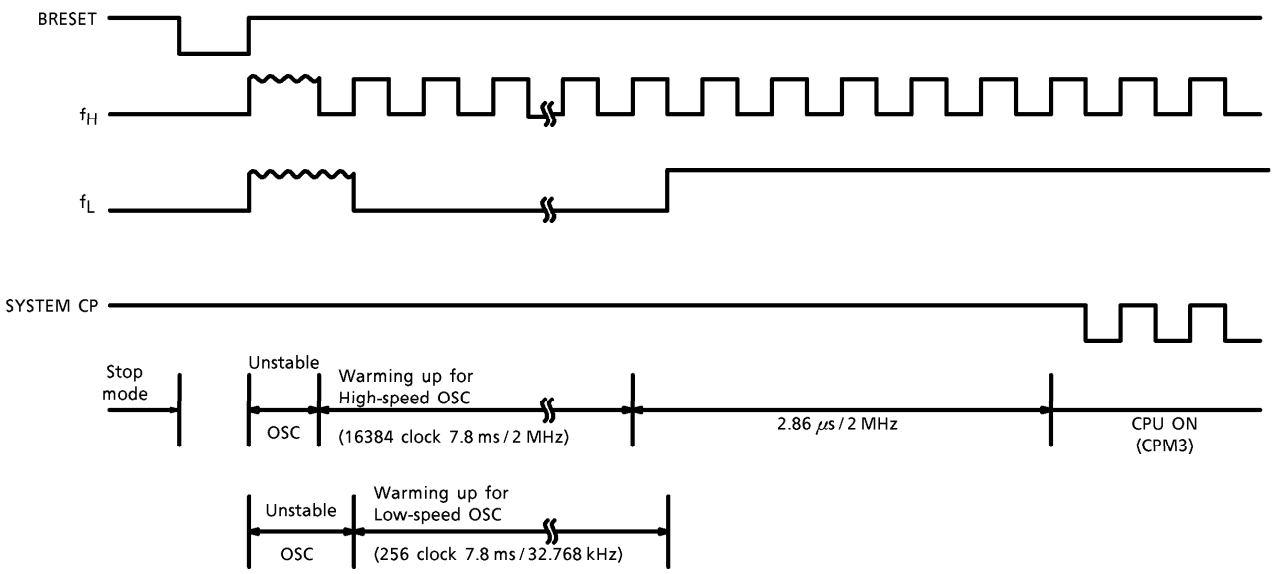
CPM0 (High / Low speed ON, SYSCP = High, LOWCP ON)

(Just changing to CPM0 does not change the oscillator mode.)

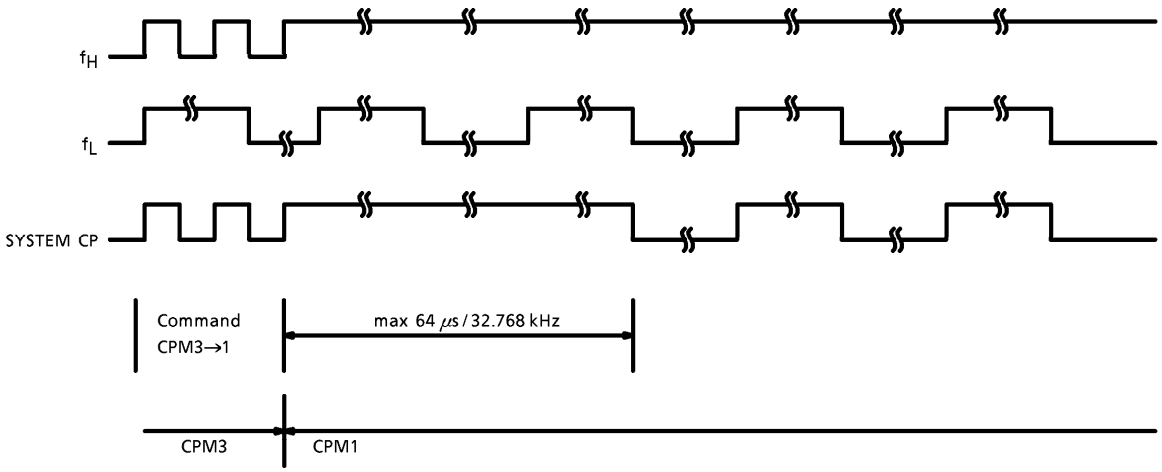
↓ LD 26O, 7H

CPM3 (High / Low speed ON, SYSCP = High, LOWCP ON)

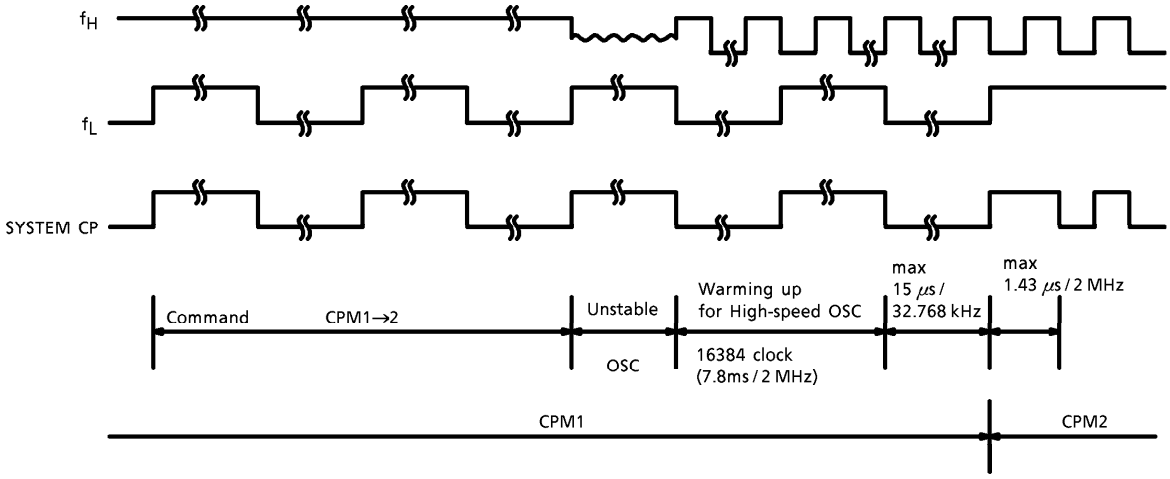
Example 4 (After reset)



Example 5 (CPM3→1)



Example 6 (CPM1→2)



(Note) : No warm-up is provided for high-speed and low-speed RC oscillations by mask options.

1-2. Single-clock specifications (system where low-speed oscillator is only used)

Oscillator types depending on use

USE	SUPPLY VOLTAGE	HIGH-SPEED	LOW-SPEED
Remote controller	3.0 V	—	X'tal (36.864 kHz)

	3	2	1	0
PA6	—	LOWCP	CPMODE2	CPMODE1
R / W	—	R / W	R / W	R / W
Initial Value	—	0	0	1

The CPU clock is generated by the asynchronous oscillator switching circuit which has low-speed clock oscillator circuit.
This block also provides the clock for the timer circuit, LCD driver, Quadrupler.
Oscillation mode is controlled by register file CPMODE1 and CPMODE2 (PAGE / AD = 2 / 6), as follows. Once CPMODE1 and CPMODE2 are set, low-speed oscillator will start and it can not be turned off.

CPMODE 1	CPMODE 2	LOW-SPEED OSC	HIGH-SPEED OSC	SYSTEM CP	MODE NAME
1	0	ON	OFF	Low speed	(CPM1)

LOWCP is the display clock control bit. When LOWCP is set to 1, Low-speed OSC clock is supplied to LCD circuit. LOWCP is initially "0". Even if LOWCP is set to 1, clock cannot be occupied to display circuit during Low-speed OSC stopped, and display cannot be shown. When using "HALT" instruction at CPM1, mode is changed to HALT mode (System CP OFF, Low-speed OSC ON).

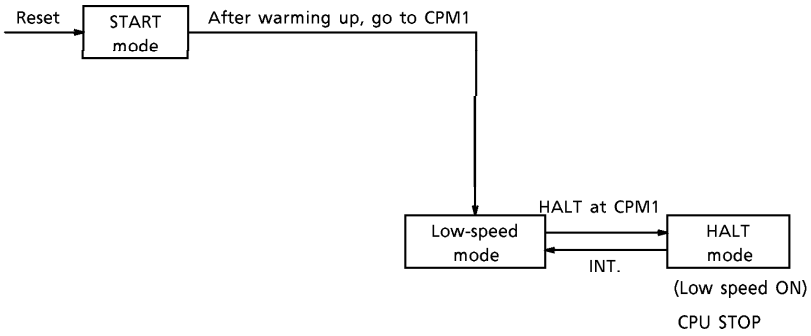


Fig.7 Mode status

TMP04060 has 15 bits Divider.
The reset for this Divider circuit is done by Register file RST (PA7W).

	3	2	1	0
PA7W	RST	—	—	—
R / W	W	—	—	—
Initial Value	0	—	—	—

RST : Binary counter reset

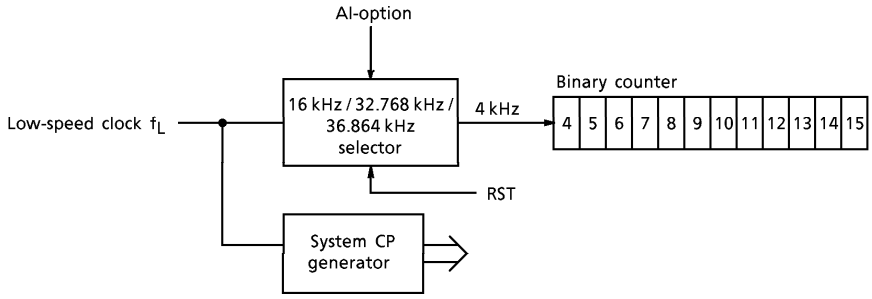


Fig.8 Divider circuit

Example 1

START mode (After warming up, program start at address 0000.)

↓

CPM1 (Low speed ON, SYSCP = Low, LOWCP ON)

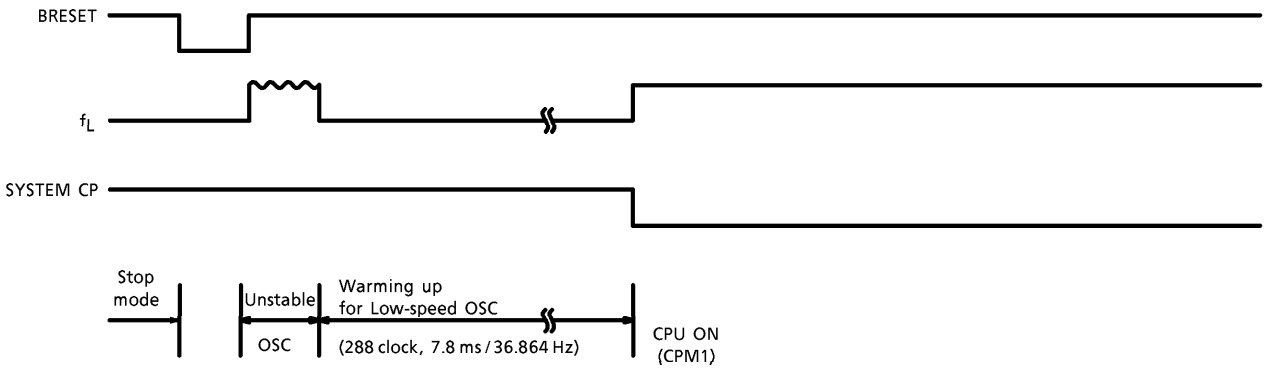
(There are no change after shift to CPM0)

↓ HALT

HALT mode (High-speed OSC, OFF, Low-speed OSC, ON, SYSCP OFF, LOWCP ON)

When an interruption occurs, the mode is changed to low-speed mode and program start at the address which is decided by each interruption .

Example 2 (After reset)



2. Interruption block

Interruption is supplied by IN1 to 4, I/O01 to 04, Timer/Counter, Timing.

(Interruption Priority)

The priority of the interrupts is fixed as shown in the table below.

INT0	INT1	INT2
TIN	IIN	IOIN

(Higher) ← Priority → (Lower)

IIN : IN1 to 4, IOIN : IO01 to 04, TIN : Timing

(Interruption enable/disable)

Each interruption (IIN, IOIN, TIN) is decided disable/enable as follows.

IIN : IIE1 to 4 (PC2-BIT0 to 3)

IOIN : IOIE0 (PC3-BIT0)

TIN : TIE1 to 4 (PD3-BIT0 to 3)

Each interruption is decided disable/enable by INT0 to 2.
Disable the unnecessary interrupts in your application by initial settings of IIE1-4, IOIE, TIE1-4, and TCI1E/2E.

INT0 to 2 are initially 0 (disable).

	3	2	1	0
R12	INT2	INT1	INT0	(0)
R/W	R/W	R/W	R/W	—
Initial Value	0	0	0	0

INT0 to 2 = 0 INT0 to 2 disable
= 1 INT0 to 2 enable

(Interrupt reset)

When an interrupt is detected, reset the interrupt as follows;
First reset the interrupt latch by disabling the interrupt (input interrupts IN1 to IN4, IO01 to IO04, timing interrupts TI1 to TI4 using the corresponding register file (IN1 to IN4 : PC2 (IIE1 to IIE4), IO01 to IO04 : PC3 (IOIE0), TI1 to TI4 : PD3 (TIE1 to TIE4). Next, reset the interrupt latch circuit for the core by disabling / enabling the interrupt using register file R12 or R13. (Enable the interrupt again by a transfer instruction to R12 or R13 if necessary.)

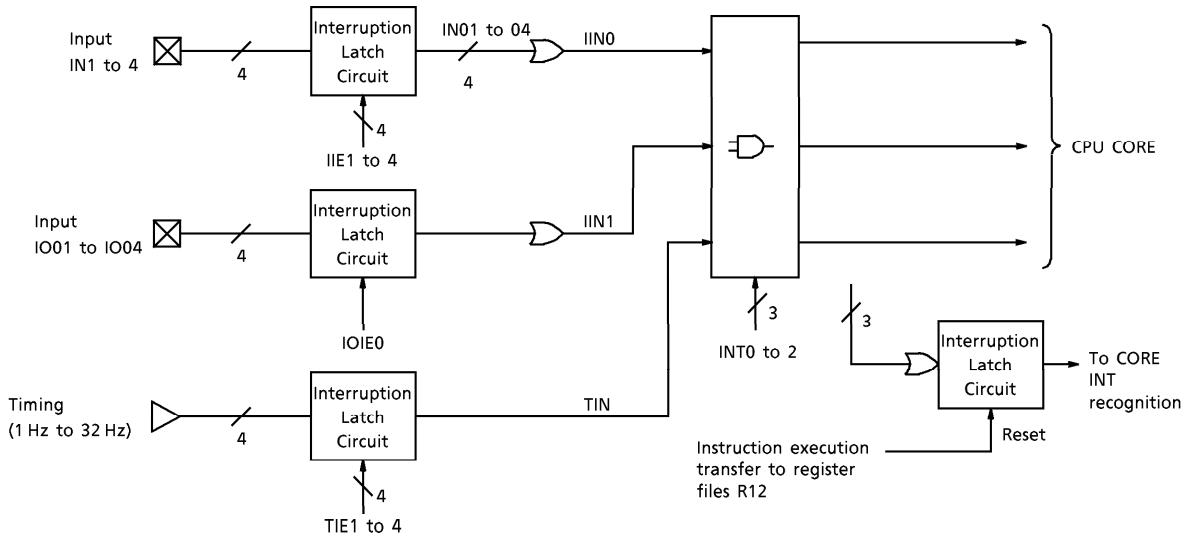


Fig.9 Interruption circuit block

2-1. Input / Inoutput Interruption

(Interruption enable / disable)

	3	2	1	0
PC2	IIE4	IIE3	IIE2	IIE1
R / W	R / W	R / W	R / W	R / W
Initial Value	0	0	0	0

IIE1 = 0 IN1 Interruption disable
1 IN1 Interruption enable
IIE2 = 0 IN2 Interruption disable
1 IN2 Interruption enable
IIE3 = 0 IN3 Interruption disable
1 IN3 Interruption enable
IIE4 = 0 IN4 Interruption disable
1 IN4 Interruption enable

IIE1 to 4 are initially 0 (IN1 to 4 Interruption disable)

	3	2	1	0
PC3	—	—	—	IOIE0
R / W	—	—	—	R / W
Initial Value	—	—	—	0

IOIE0 = 0 IO01 to 4 Interruption disable
= 1 IO01 to 4 Interruption enable

IOIE0 is initially 0 (disable)

Interruption enable / disable bit can use as interruption reset.
When the interruption occurs and after recognizing the interruption, it can be resetted INT latch by setting IIE1 to 4 or IOIE0.

(Interruption Data Read)

Interruption Data of IN1 to 4 can be read by Register file IIN1 to 4.

	3	2	1	0
PC1R	IIN4	IIN3	IIN2	IIN1
R / W	R	R	R	R
Initial Value	0	0	0	0

Example

```
LD 42O, 0FH    (set enable to IN1 to 4 interruption)
    ↓          IN1 interruption occurs.
               Program goes to the address which is decided by each interruption.
LD M, 4IO      (read IN1 to 4 interruption)
    ↓          Recognize which interruption is occurred.
               (Recognize IN1 interruption is occurred.)
LD 42O, 0EH    (reset IN1 interruption)
    ↓
LD 12O, 0FH    (set enable to INT0 to 2)
```

2-2. Timing interruption

(Timing Interruption enable / disable)

Selected Timing Interruption can be controlled enable / disable by Register file TIE1 to 4 (PD3).
TIE1 to 4 are initially 0 (disable).

<High-speed oscillator : 2 MHz, low-speed oscillator : 32.768 kHz>

	3	2	1	0
PD03	TIE4	TIE3	TIE2	TIE1
R / W	R / W	R / W	R / W	R / W
Initial Value	0	0	0	0

TIE1 = 0 1 Hz INT. disable
1 1 Hz INT. enable
TIE2 = 0 2 Hz INT. disable
1 2 Hz INT. enable
TIE3 = 0 8 Hz INT. disable
1 8 Hz INT. enable
TIE4 = 0 32 Hz INT. disable
1 32 Hz INT. enable

(Timing interruption read)

Selected Timing Interruption can be read by Register file TI1 to 4 (PD0R).
<High-speed oscillator : 2 MHz, low-speed oscillator : 32.768 kHz>

	3	2	1	0
PD0R	TI4	TI3	TI2	TI1
R / W	R	R	R	R
Initial Value	0	0	0	0

TI1 : Interruption data of 1 Hz
TI2 : Interruption data of 2 Hz
TI3 : Interruption data of 8 Hz
TI4 : Interruption data of 32 Hz

(Interruption edge selection)

TIN Interruption can be selected the reading point (↑ or ↓) by Register file ESELT. ESTLT is initially 0 (rising EDGE).

	3	2	1	0
PC0	—	ESELT	(ESLI0)	(ESSELI)
R / W	—	R / W	R / W	R / W
Initial Value	—	0	0	0

ESELT = 0 : Interruption at rising Edge of Timing INT.
1 : Interruption at rising Edge of Timing INT.

3. Watchdog timer

JTMP04060-XXXS incorporates a one-channel independent dedicated watchdog timer. Watchdog time can be selected from 32.768 kHz, 0.5, 1.0, or 2.0 seconds. Writing to PA4 of the register file clears the watchdog timer.

	3	2	1	0
PA4			WDT2	WDT1
R / W			R / W	R / W
Initial Value			0	0

WDT2	WDT1	32.768 kHz
0	0	Stop
0	1	0.5 s
1	0	1.0 s
1	1	2.0 s

* To run the watchdog timer, the binary counter circuit must be run.
* The binary counter dose not run while CPU is in CPM2 mode.

4. I/O PORT (Refer to Fig.10)

TMP04060F-XXXX has 4 inputs and 12 I/O ports.
4 inputs and 4 I/O ports have Interruption.For details, refer to page 128.

4-1. INPUT (IN1 to 4)

Each input data can be read by Register file IND1 to 4.

	3	2	1	0
PA0R	IND4	IND3	IND2	IND1
R/W	R	R	R	R
Initial Value	0	0	0	0

Each input Interruption function can be set enable/disable by Register file IIE1 to 4.

	3	2	1	0
PC2	IIE4	IIE3	IIE2	IIE1
R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0

IIE1 to 4 = 0 : IN1 to IN4 each Interruption disable
= 1 : IN1 to IN4 each Interruption enable

(Note) : IIE1 to IIE4 interrupt disable/enables are register files that are effective when rising-edge interrupts are selected.
When level interrupts are selected, interrupts are disabled/enabled by the data input from ports. In this case, therefore, interrupts cannot be disabled/enabled by the register files.

4 inputs (IN1 to 4) Interruption data can be read by Register file IIN1 to 4.

	3	2	1	0
PC1R	IIN4	IIN3	IIN2	IIN1
R/W	R	R	R	R
Initial Value	0	0	0	0

(Note) : Interrupt data IN11 to IN14 cannot be read out. Only the data input from ports can be read out. (refer to Fig.9.)

Interrupt timings (rising edge / level) can be selected using register file ESELI.

	3	2	1	0
PC0	—	(ESELT)	(ESELIO)	ESELI
R / W	—	R / W	R / W	R / W
Initial Value	—	0	0	0

ESELI = 0 IN1 to 4 : Interruption at rising edge of input INT.
= 1 IN1 to 4 : High level of input INT.

Input level-triggered interrupts are possible when ESELIO = 1. In this case, if interrupts have been enabled by register files INT0-2, the interrupt remain asserted while the input level is high.

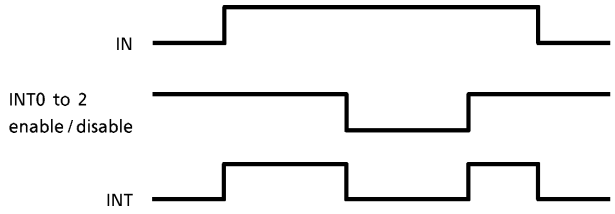


Fig.10 Interruption by high level-read

SELECTING INPUT PULL-DOWN RESISTOR

Using bit 2 of register file PD5, a pull-down resistor can be connected / disconnected to IN1 to IN4.

	3	2	1	0
PD5	—	INR	(TPCNT)	(IB)
R / W	—	R / W	R / W	R / W
Initial Value	—	0	0	0

The INR initial value is 0 (pull-down resistor off).

4-2. I/O ports (IO01 to IO04)

Each input data can be read by IOD01 to IOD04 of Register file, when using input port.

	3	2	1	0
PA1R	IOD04	IOD03	IOD02	IOD01
R/W	R	R	R	R
Initial Value	—	—	—	—

IO01 to IO04 have Interruption, each interruption function can be set disable/enable by Register file PA1R.
(Four interrupt sources are collectively disabled/enabled by IOIE0.)

	3	2	1	0
PC3	—	—	—	IOIE0
R/W	—	—	—	R/W
Initial Value	—	—	—	0

IOIE0 = 0 : IO01 to IO04 Interruption disable
= 1 : IO01 to IO04 Interruption enable

(Note) : The IO01-IO04 interrupt disable/enables are the register files that are effective when rising-edge interrupts are selected.
When level interrupts are selected, interrupts are disabled/enabled by the data input from ports. In this case, therefore, interrupts cannot be disabled/enabled by the register files.
The interrupt data IO01 to IO04 cannot be read out. Only the data input from ports can be read out.

	3	2	1	0
PC0	—	(ESELT)	ESELIO	(ESELI)
R/W	—	R/W	R/W	R/W
Initial Value	—	0	0	0

ISELIO = 0 IN1 to 4 : Interruption at rising edge of input INT.
= 1 IN1 to 4 : High level of input INT.

Input level-triggered interrupts are possible when ESELIO = 1. In this case, if interrupts have been enabled by register files INT0-2, the interrupt remain asserted while the input level is high.

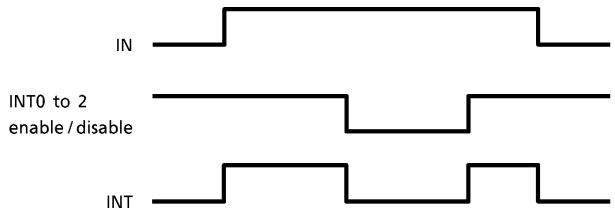


Fig.11 Interruption by high level-read

Output data can be read by following Register file, when using each I/O ports as output.

	3	2	1	0
PA1W	IOO04	IOO03	IOO02	IOO01
R/W	W	W	W	W
Initial Value	0	0	0	0

4-3. I/O ports (IO11 to IO14, IO21 to IO24)

Each input data can be read by following Register file, when using input port.

	3	2	1	0
R14R	IOD14	IOD13	IOD12	IOD11
R/W	R	R	R	R
Initial Value	—	—	—	—

	3	2	1	0
R15R	IOD24	IOD23	IOD22	IOD21
R/W	R	R	R	R
Initial Value	0	0	0	0

When using each input/output port for output, the output data can be set using the register file shown below.

	3	2	1	0
R14W	IOO14	IOO13	IOO12	IOO11
R/W	W	W	W	W
Initial Value	0	0	0	0

	3	2	1	0
R15W	IOO24	IOO23	IOO22	IOO21
R/W	W	W	W	W
Initial Value	0	0	0	0

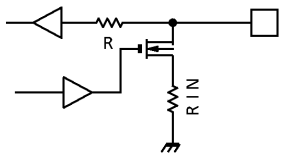
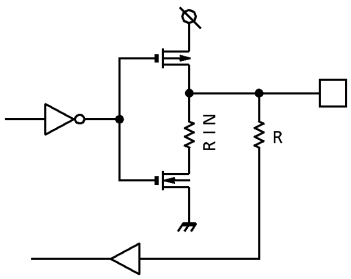
	INPUT / OUTPUT CIRCUITS
IN1 to IN4	
IO01 to IO04 IO11 to IO14 IO21 to IO24 * Low (Pull down) after reset	

Fig.12 Structure of input / output port

RIN : Internal pull-down resistor, 400 kΩ (Typ.)
R : Input protective resistor, 150 Ω (Typ.)

4-4. Expanted output ports (O31 to O34)

Setting when using SEGMENT Driver as an output port.

	3	2	1	0
PC6	—	EXO	(DON)	(DSTA)
R / W	—	R / W	W	W
Initial Value	—	0	0	0

EXO	SEG PIN
	SEG24 TO 27
0	SEG Dr
1	Output ports

The initial value of EXO is 0.

Each data for output port can be set by following Register file.

	3	2	1	0
PD4W	OO34	OO33	OO32	OO31
R / W	R / W	R / W	R / W	R / W
Initial Value	0	0	0	0

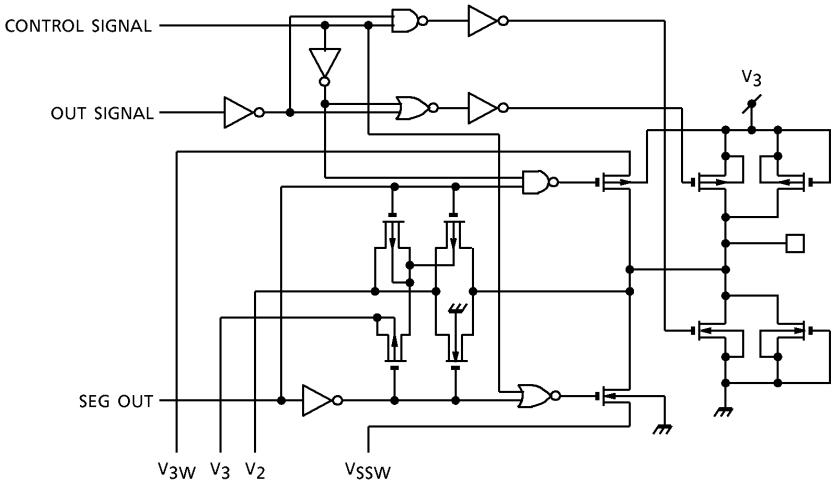
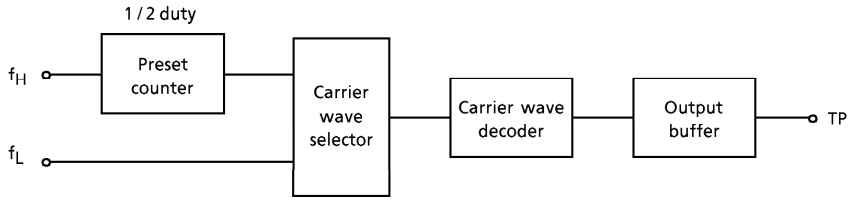
	OUTPUT CIRCUIT
O31 to O34 * SEGMENT is output port after reset	

Fig.13 Structure of output port

5. Remote control transmitter circuit (Carrier wave output)

This port is an output-only port for carrier wave output. The circuit consists of a carrier wave decoder and an output buffer. Fig.14 shows an example of the structure of output code from the port.
Carrier wave can be selected using the register shown below.



When a 36.864-kHz oscillator is used, the carrier waveform has the same cycle as that of source oscillation (f_{OSC}). This output waveform can be programmed in units of one instruction in two cycles. When using a 2-MHz oscillator, with 1 / 106 frequency (1 / 2 duty), the waveform can be programmed in units of 106 instructions in two cycles.
Fig.14 shows an example of code structure where custom code and data code are generated in 8 bits.
The output code is generated by software. Various types of codes such as 1 code in 16 bits, data 2 code, and data 3 code can be output. This port can be programmed to output a non-carrier waveform.

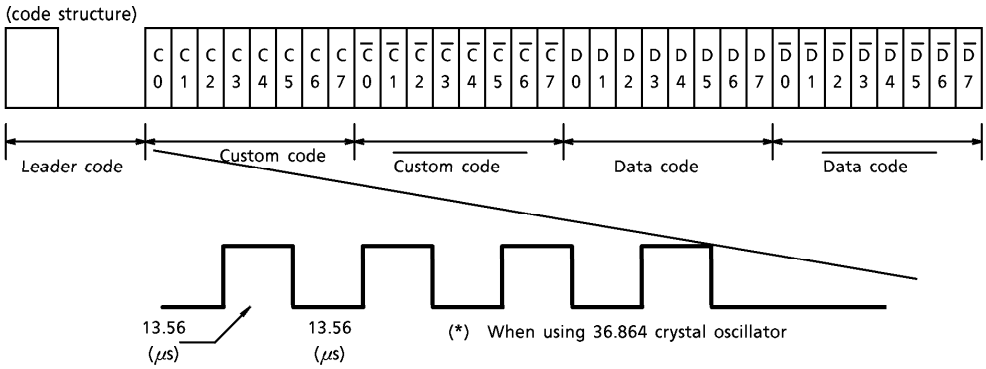


Fig.14 Output code structure (Example)

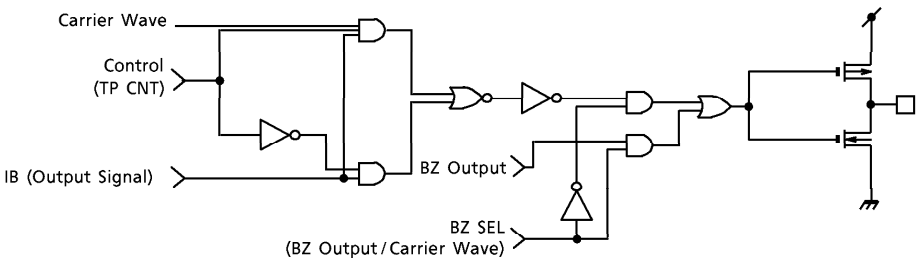
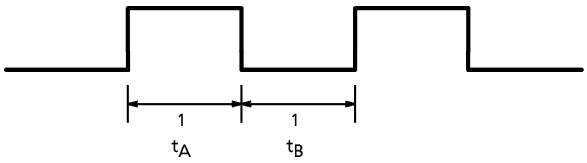


Fig.15 Diagram of output port circuit

5-1. Selecting carrier wave obtained from high-speed oscillator

Carrier wave duty 1 / 2



Using registers PD6 and PD7, the following frequencies obtained by dividing f_H can be selected for $t_A + t_B$.

	3	2	1	0
PD6	CARRY3	CARRY2	CARRY1	CARRY0
R / W	R / W	R / W	R / W	R / W
Initial Value	0	0	0	0

	3	2	1	0
PD7	CARRY7	CARRY6	CARRY5	CARRY4
R / W	R / W	R / W	R / W	R / W
Initial Value	0	0	0	0

1. High-speed OSC frequency 2 MHz

CARRY 7	CARRY 6	CARRY 5	CARRY 4	CARRY 3	CARRY 2	CARRY 1	CARRY 0	TPCONT	IB	DIVID	CARRIER WAVE FREQUENCY OUTPUT (kHz)
0	0	0	0	0	0	0	0	0	0		
0	0	0	0	0	1	1	0	1	1	1 / 12	166.67
0	0	0	0	0	1	1	1	1	1	1 / 14	142.86
0	0	0	0	1	0	0	0	1	1	1 / 16	125.00
0	0	0	0	1	0	0	1	1	1	1 / 18	111.11
0	0	0	0	1	0	1	0	1	1	1 / 20	100.00
0	0	0	0	1	0	1	1	1	1	1 / 22	90.91
0	0	0	0	1	1	0	0	1	1	1 / 24	83.33
0	0	0	0	1	1	0	1	1	1	1 / 26	76.92
0	0	0	0	1	1	1	0	1	1	1 / 28	71.43
0	0	0	0	1	1	1	1	1	1	1 / 30	66.67
0	0	0	1	0	0	0	0	1	1	1 / 32	62.50
0	0	0	1	0	0	0	1	1	1	1 / 34	58.82
0	0	0	1	0	0	1	0	1	1	1 / 36	55.56
0	0	0	1	0	0	1	1	1	1	1 / 38	52.63
0	0	0	1	0	1	0	0	1	1	1 / 40	50.00
0	0	0	1	0	1	0	1	1	1	1 / 42	47.62
0	0	0	1	0	1	1	0	1	1	1 / 44	45.45
0	0	0	1	0	1	1	1	1	1	1 / 46	43.48
0	0	0	1	1	0	0	0	1	1	1 / 48	41.67
0	0	0	1	1	0	0	1	1	1	1 / 50	40.00
0	0	0	1	1	0	1	0	1	1	1 / 52	38.46
0	0	0	1	1	0	1	1	1	1	1 / 54	37.04
0	0	0	1	1	1	0	0	1	1	1 / 56	35.71
0	0	0	1	1	1	0	1	1	1	1 / 58	34.48
0	0	0	1	1	1	1	0	1	1	1 / 60	33.33
0	0	0	1	1	1	1	1	1	1	1 / 62	32.26
0	0	1	0	0	0	0	0	1	1	1 / 64	31.25
0	0	1	0	0	0	0	1	1	1	1 / 66	30.30
0	0	1	0	0	0	1	0	1	1	1 / 68	29.41
0	0	1	0	0	0	1	1	1	1	1 / 70	28.57
0	0	1	0	0	1	0	0	1	1	1 / 72	27.78
0	0	1	0	0	1	0	1	1	1	1 / 74	27.03
0	0	1	0	0	1	1	0	1	1	1 / 76	26.32
0	0	1	0	0	1	1	1	1	1	1 / 78	25.64
0	0	1	0	1	0	0	0	1	1	1 / 80	25.00
0	0	1	0	1	0	0	1	1	1	1 / 82	24.39
0	0	1	0	1	0	1	0	1	1	1 / 84	23.81
0	0	1	0	1	0	1	1	1	1	1 / 86	23.26
0	0	1	0	1	1	0	0	1	1	1 / 88	22.73
0	0	1	0	1	1	0	1	1	1	1 / 90	22.22
0	0	1	0	1	1	1	0	1	1	1 / 92	21.74
0	0	1	0	1	1	1	1	1	1	1 / 94	21.28
0	0	1	1	0	0	0	0	1	1	1 / 96	20.83
0	0	1	1	0	0	0	1	1	1	1 / 98	20.41
0	0	1	1	0	0	1	0	1	1	1 / 100	20.00
0	0	1	1	0	0	1	1	1	1	1 / 102	19.61
0	0	1	1	0	1	0	0	1	1	1 / 104	19.23
0	0	1	1	0	1	0	1	1	1	1 / 106	18.87

2. High-speed OSC frequency 455 kHz

CARRY 7	CARRY 6	CARRY 5	CARRY 4	CARRY 3	CARRY 2	CARRY 1	CARRY 0	TPCONT	IB	DIVID	CARRIER WAVE FREQUENCY OUTPUT (kHz)
0	0	0	0	0	0	0	0	0	0		
0	0	0	0	0	1	1	0	1	1	1 / 12	37.91
0	0	0	0	0	1	1	1	1	1	1 / 14	32.5
0	0	0	0	1	0	0	0	1	1	1 / 16	28.43
0	0	0	0	1	0	0	1	1	1	1 / 18	25.27
0	0	0	0	1	0	1	0	1	1	1 / 20	22.75
0	0	0	0	1	0	1	1	1	1	1 / 22	20.68
0	0	0	0	1	1	0	0	1	1	1 / 24	18.95
0	0	0	0	1	1	0	1	1	1	1 / 26	17.5
0	0	0	0	1	1	1	0	1	1	1 / 28	16.25
0	0	0	0	1	1	1	1	1	1	1 / 30	15.16
0	0	0	1	0	0	0	0	1	1	1 / 32	14.21
0	0	0	1	0	0	0	1	1	1	1 / 34	13.38
0	0	0	1	0	0	1	0	1	1	1 / 36	12.63
0	0	0	1	0	0	1	1	1	1	1 / 38	11.97
0	0	0	1	0	1	0	0	1	1	1 / 40	11.37
0	0	0	1	0	1	0	1	1	1	1 / 42	10.83
0	0	0	1	0	1	1	0	1	1	1 / 44	10.34
0	0	0	1	0	1	1	1	1	1	1 / 46	9.89
0	0	0	1	1	0	0	0	1	1	1 / 48	9.47
0	0	0	1	1	0	0	1	1	1	1 / 50	9.1

TP control and IB (output signal) of the output port circuit in Fig.2 can be controlled by register PD5.

	3	2	1	0
PD5	—	INR	TPCNT	IB
R / W	—	R / W	R / W	R / W
Initial Value	—	0	0	0

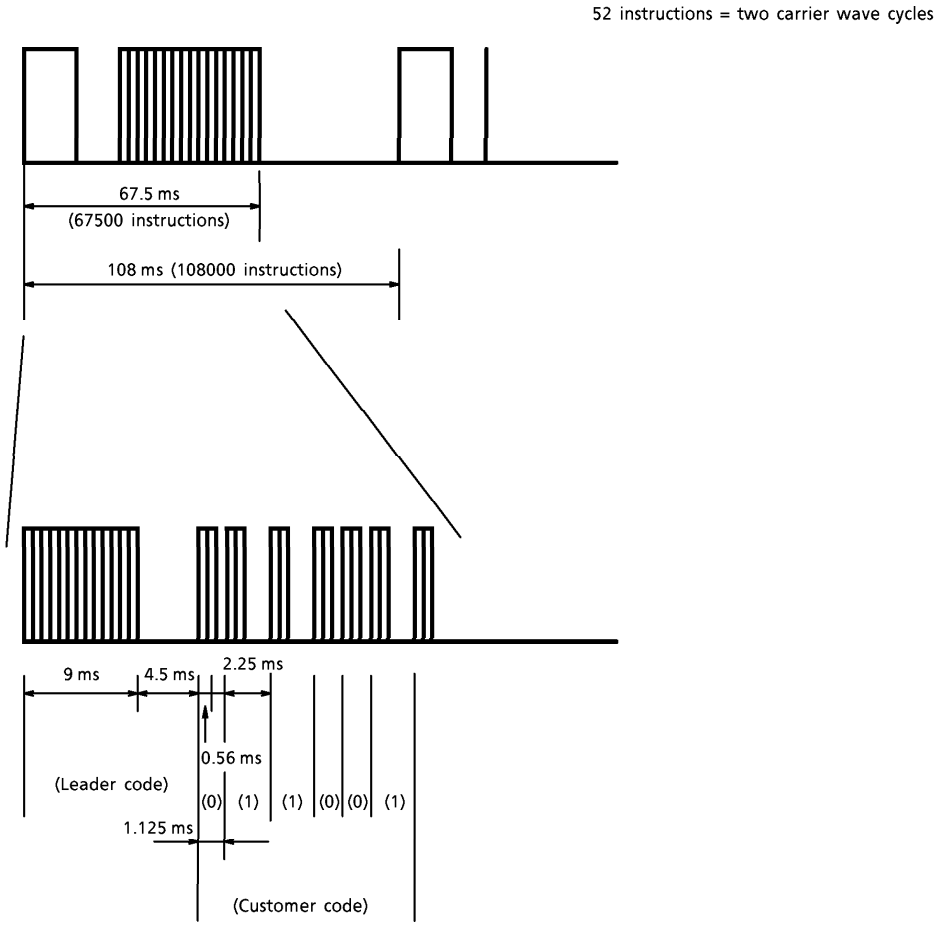
How to generate carrier wave obtained from the high-speed oscillator can be summarized as follows :

TP	IB	TPCNT
Off (H)	0	*
Carrier wave of any frequency	0 or 1 by program	1
Non-carrier wave output	0 or 1 by program (Note)	0

* : arbitrary
(Note) : The control time varies depending on the selected system clock.

① Remote output waveform (Example)

For 1 / 52 frequency (carrier wave : 38.46 kHz) using 2-MHz high-speed oscillator



② Remote output flow chart (Example)

For 1 / 52 frequency (carrier wave : 38.46 kHz) using 2-MHz high-speed oscillator

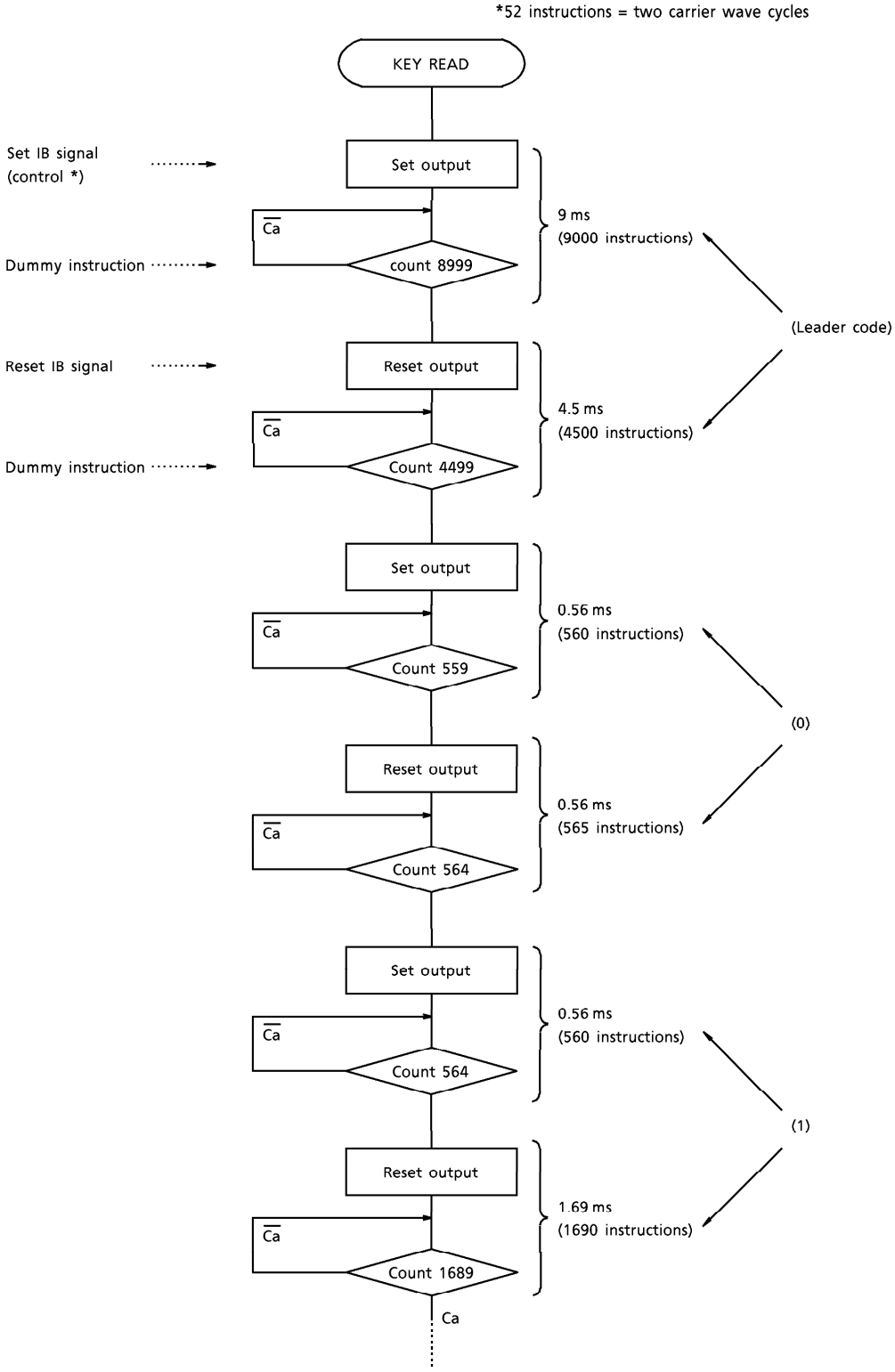


Fig.15 Remote output waveform (Example)

For 36.864-kHz crystal oscillator

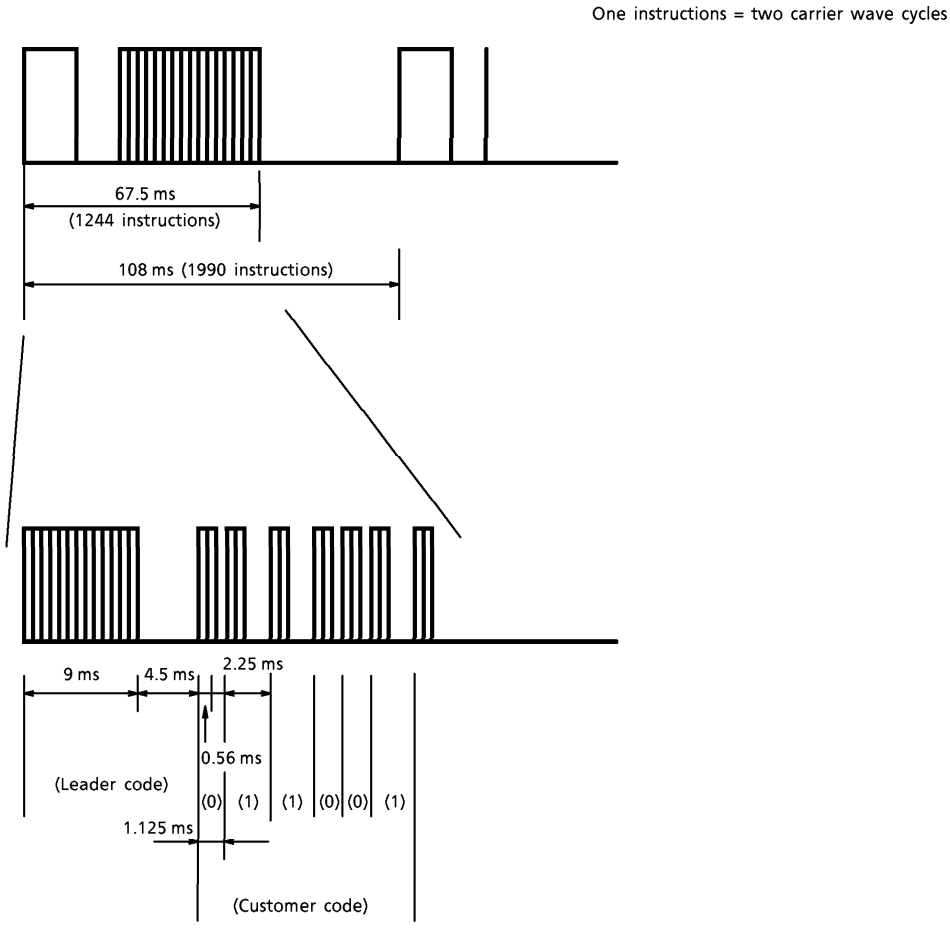
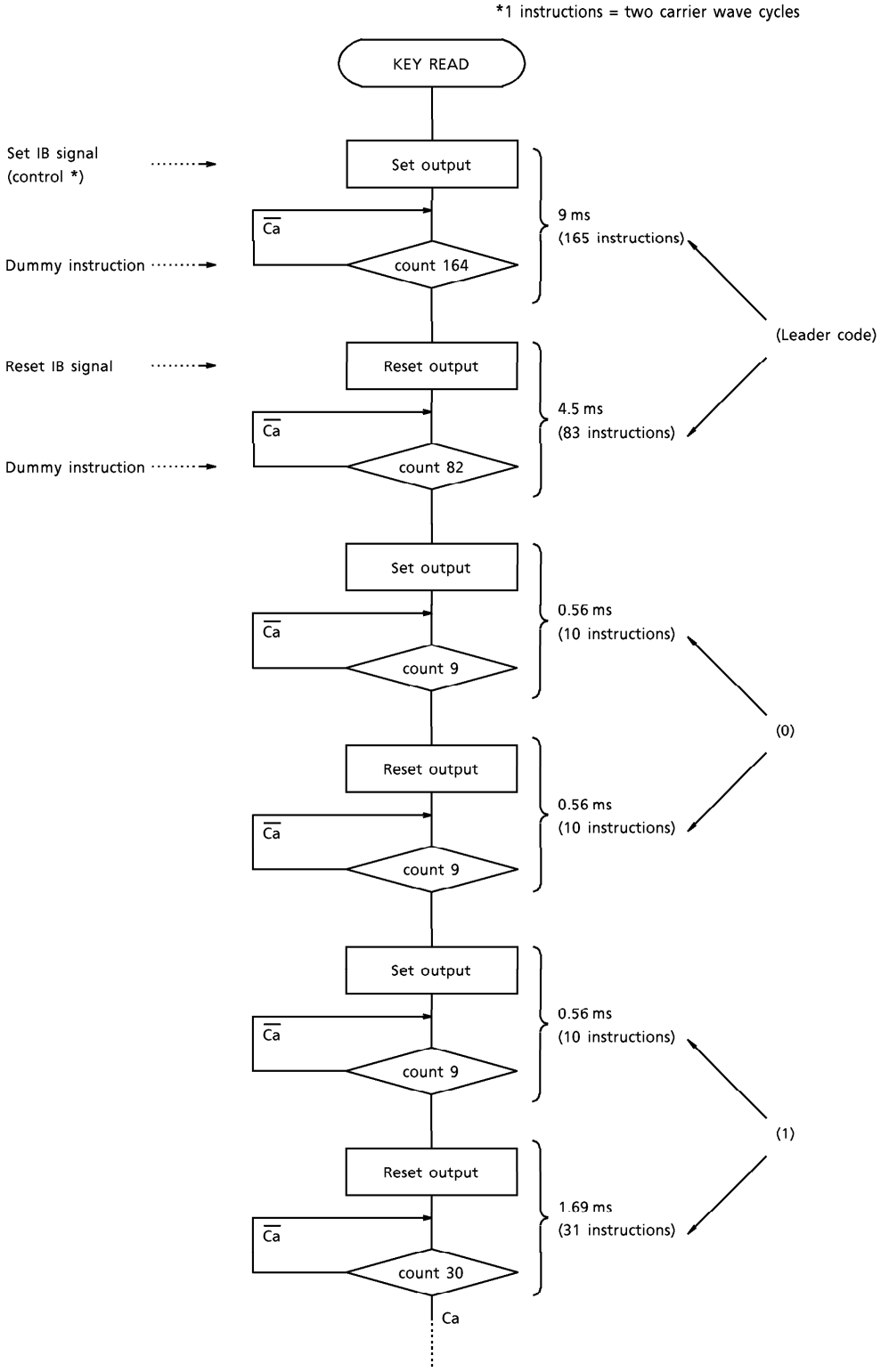


Fig.16 Remote output flow chart (example)

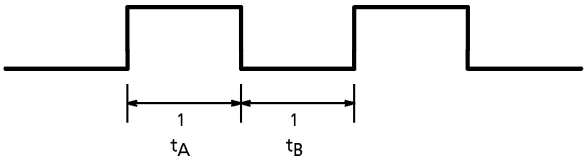
For using 36.864-kHz crystal oscillator



5-2. Selecting carrier wave obtained from low-speed oscillator

In case the single clock mode is selected by mask option, the carrier wave is generated by low speed clock.

The carrier wave duty is 1 / 2.



6. LCD circuit

The LCD driver circuit has common signals and segment signals to drive 4.5 V, 1 / 4 duty, 1 / 3 bias LCD.

DUTY	FRAME FREQUENCY	COMMON	SEGMENT
1 / 4	97.5 Hz	COM1 to COM4	S1 to S27

The LCD driver circuit is controlled by Register file both DSTA and DON.

	3	2	1	0
PC6W	—	(EXO)	DON	DSTA
R / W	—	R / W	W	W
Initial Value	—	0	0	0

DSTA = 0 com / seg = V_{SS}
= 1 enable normal Display
DON = 0 Quadrupler OFF
= 1 Quadrupler ON

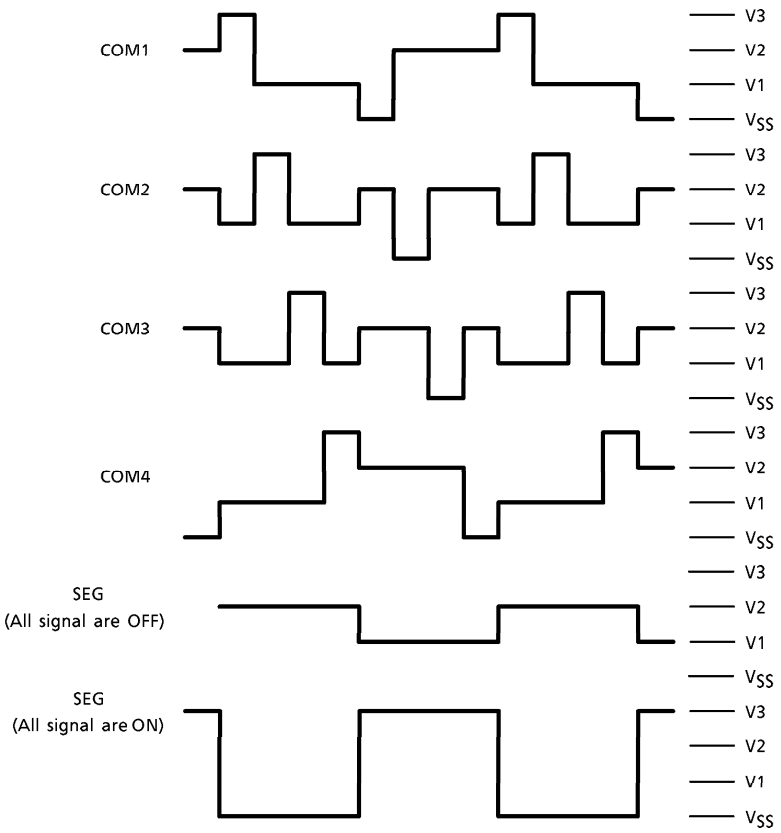


Fig.17 1/4 duty display wave form

(Note 1) : Display signals from segment and common are mode by the clock which come from low-speed oscillation. Even though the high-speed oscillator may be operating no display is output unless the low-speed oscillator is operating.

(Note 2) : Register file DON and DSTA are read to Display Driver circuit by the clock which is made by LOWCP.
When the LOWCP is needed OFF it is needs max. 103 ms after changing the data of DON and DSTA.

5. Buzzer circuit

Buzzer sound can be selected by Register file BZSEL, BZ1, BZ0.
(Note that BZ is also used as the remote control output pin.)

	3	2	1	0
PC7	—	BZSEL	BZ1	BZ0
R / W	—	R / W	R / W	R / W
Initial Value	—	0	0	0

The buzzer drive frequency is 4 kHz.
The initial values are all 0 s.

When BZSEL = 0, TP output (remote control carrier wave output).
When BZSEL = 1, buzzer drive output (CMOS).

BZ1	BZ0	Buzzer Output
0	0	"L"
0	1	8 Hz, 1 Hz
1	0	
1	1	"H"

Setting the above register once continuously outputs the above timing as cycle (1 Hz).

Note : Since low-frequency oscillation is used to generate clock for the buzzer circuit, buzzer sound cannot be output in CPM0 Mode and CPM2 Mode, in which low-frequency oscillation is stopped.

8. Mask option

TMP04060FXXX has following Mask option.

USE	BATTERY	HIGH-SPEED OSC	LOW-SPEED OSC
Calculater	1.5 V	CR (78 k)	Internal C (16 k)
	3.0 V	CR (1.1 M)	Internal C (30 k)
Remote Controller	3.0 V	—	X'tal (36.864 k)
	3.0 V	X'tal (2 M)	X'tal (32.768 k)
	3.0 V	X'tal (455 k)	X'tal (32.768 k)

9. ELECTRICAL CHARACTERISTICS

Absolute maximum ratings (V_{SS} = 0 V)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	− 0.3 to 6.0	V
Input Voltage	V_{IN}	− 0.3 to V_{DD} + 0.3	V
Power Dissipation	P_D	350	mW
Solder Temperature	T_{sol}	260 (10 s)	°C
Storage Temperature	T_{stg}	− 55 to 125	°C
Operating Temperature	T_{opr}	− 10 to 50	°C

1.5 V version (Unless otherwise specified, V_{SS} = 0 V, Ta = 25°C)
(Recommended operating condition)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Power Supply Voltage		V_{DD}	f_{XTH} = 78 kHz	1.2	1.5	1.8	V
Oscillation Frequency		f_L	V_{DD} = 1.5 V, R_f = 470kΩ (*1)	—	16	—	kHz
		f_H	V_{DD} = 1.5 V (*2)	27	78	109	
Input Voltage	"H" Level	V_{IH}	V_{DD} = 1.3 V	V_{DD} × 0.8	—	V_{DD}	V
			V_{DD} = 1.7 V	V_{DD} × 0.7	—	V_{DD}	
	"L" Level	V_{IL}	V_{DD} = 1.3 V	0	—	V_{DD} × 0.2	
			V_{DD} = 1.7 V	0	—	V_{DD} × 0.3	
Quadrupler Capacitance		C_1, C_2		—	0.1	—	μF
Smoothing Capacitance		V_1		—	0.1	—	μF
		V_2		—	0.1	—	

(*1) : Internal crystal oscillation circuit is used for low-speed oscillator (with external R).
(*2) : Internal CR oscillator is used for high-speed oscillator.

(DC CHARACTERISTICS)

CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN	TYP.	MAX	UNIT
Input Current (1) (IN1 to 4, IO01 to 04 IO11 to 14, IO21 to 24)	I_{IL1}	V_{DD} = 1.8 V, V_{IN} = 0 V		– 500	—	500	nA
	I_{IH1}	V_{DD} = 1.8 V, V_{IN} = 1.8 V		3.21	4.5	7.5	μA
Input Current (2) (BRESET)	I_{IL2L}	V_{DD} = 1.8 V, V_{IN} = 1.3 V, Low Register side		– 16.6	– 10	– 7.14	μA
	I_{IL2H}	V_{DD} = 1.8 V, V_{IN} = 0 V, High Register side		– 6	– 3.6	– 2.57	
Input Current (3) (TEST)	I_{IH3}	V_{DD} = 1.8 V, V_{IN} = 1.8 V		129	180	300	μA
Output Current (1) (IO01 to 04, IO11 to 14, IO21 to IO24)	I_{OH1}	V_{DD} = 1.2 V, V_{OH} = 0.7 V		—	—	– 150	μA
Output Current (2) (TP)	I_{OH4}	V_{DD} = 1.2 V, V_{OH} = 0.7 V		—	—	– 50	μA
	I_{OL4}	V_{DD} = 1.2V, V_{OL} = 0.5 V		100	—	—	
Output Current (3) (SEGMENT)	I_{OH2}	V_{DD} = 1.5 V, V_A = 3.0 V, V_B = 4.5 V	V_{OH} = V_3 – 0.5 V	—	—	– 100	μA
	I_{OL2}		V_{OL} = 0.5 V	100	—	—	
	I_{OM2A}		V_{OM} = V_1 + 0.5 V	50	—	—	
	I_{OM2B}		V_{OM} = V_2 – 0.5 V			– 50	
Output Current (4) (COMMON)	I_{OH3}	V_{DD} = 1.5 V, V_A = 3.0 V, V_B = 4.5 V	V_{OH} = V_3 – 0.5 V	—	—	– 100	μA
	I_{OL3}		V_{OL} = 0.5 V	100	—	—	
	I_{OM3A}		V_{OM} = V_1 + 0.5 V	—	—	– 50	
	I_{OM3B}		V_{OM} = V_2 + 0.5 V	50	—	—	
Quadrupler Output	V_A	V_{DD} = 1.5 V, Ta = 25°C		—	2 × V_{DD}	—	V
	V_B			—	3 × V_{DD}	—	
Power Supply Current (Low-Speed Crystal Oscillation Circuit / High-Speed Crystal Oscillation Circuit)	I_{DDOP}	V_{DD} = 1.5 V, f_H = Internal, f_L = Internal, CPM3, external R = 470 kΩ	Display ON	—	50	77	μA
			Display OFF	—	—	73	
	I_{DDSLOW}	V_{DD} = 1.5 V, f_H = Internal, f_L = Internal (external R), CPM1	Display ON	—	12	17	
			Display OFF	—	—	16	
	I_{DDHOLD}	V_{DD} = 1.5 V, f_H = Internal, f_L = Internal (external R), In HALT mode	Display ON	—	2.5	5.0	
			Display OFF	—	—	4.0	
	I_{DDSTOP}	V_{DD} = 1.5 V In STOP mode		—	0.4	1	

3. 3.0 V version (Unless otherwise specified, V_{SS} = 0 V, Ta = 25°C)

3-1. Typical operating conditions

(DC CHARACTERISTIC)

CHARACTERISTIC		SYMBOL	TEST CONDITION		MIN	TYP.	MAX	UNIT
Input Current (1) (IN1 to 4, IO01 to 04 IO11 to 14, IO21 to 24)		I_{IL1}	V_{DD} = 3.6 V, V_{IN} = 0 V		– 500	—	500	nA
		I_{IH1}	V_{DD} = 3.6 V, V_{IN} = 3.6 V		6.43	9.0	15.0	μA
Input Current (2) (BRESET)		I_{IL2L}	V_{DD} = 3.6 V, V_{IN} = 3.1 V, Low Register side		– 16.6	– 10	– 7.14	μA
		I_{IL2H}	V_{DD} = 3.6 V, V_{IN} = 0 V, High Register side		– 12	– 7.2	– 5.14	
Input Current (3) (TEST)		I_{IH3}	V_{DD} = 3.6 V, V_{IN} = 3.6 V		257	360	600	μA
Output Current (1) (IO01 to IO04, IO11 to IO14, IO21 to IO24)		I_{OH1}	V_{DD} = 2.4 V, V_{OH} = 1.9 V		—	—	– 1.5	mA
Output Current (2) (TP)		I_{OL2}	V_{DD} = 2.4 V, V_{OL} = 0.5 V		2.0	—	—	mA
		I_{OH2}	V_{DD} = 2.4 V, V_{OH} = 1.9 V		—	—	– 2.0	
Output Current (3) (SEGMENT)		I_{OH3}	V_{DD} = 3.0 V, V_A = 1.5 V, V_B = 4.5 V	$V_{OH} = V_2 - 0.5$ V	—	—	– 100	μA
		I_{OL3}		V_{OL} = 0.5 V	100	—	—	
		I_{OM3A}		$V_{OM} = V_2 + 0.5$ V	—	—	– 100	
		I_{OM3B}		$V_{OM} = V_1 - 0.5$ V	50	—	—	
Output Current (4) (COMMON)		I_{OH4}	V_{DD} = 3.0 V, V_A = 1.5 V, V_B = 4.5 V	$V_{OH} = V_3 - 0.5$ V	—	—	– 100	μA
		I_{OL4}		V_{OL} = 0.5 V	100	—	—	
		I_{OM4A}		$V_{OM} = V_2 - 0.5$ V	—	—	– 100	
		I_{OM4B}		$V_{OM} = V_1 + 0.5$ V	100	—	—	
Quadrupler Output		V_1	V_{DD} = 3.0 V, Ta = 25°C		—	V_{DD} / 2	—	V
		V_3			—	3 / 2 × V_{DD}	—	
Input Voltage	High level	V_{IH}	V_{DD} = 1.8 V		V_{DD} × 0.8	—	V_{DD}	V
			V_{DD} = 3.6 V		V_{DD} × 0.7	—	V_{DD}	
	Low level	V_{IL}	V_{DD} = 1.8 V		0	—	V_{DD} × 0.2	
			V_{DD} = 3.6 V		0	—	V_{DD} × 0.3	
Quadrupler Capacitor		C_1, C_2			—	0.1	—	μF
Smoothing Capacitor		V_A			—	0.1	—	μF

3-2. Specifications for 3.0-V calculator

H-OSC : 1.1 MHz (with internal CR), L-OSC : 30 kHz (with internal C and external R)

(Recommended operating conditions)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Power Supply Voltage	V_{DD}	f_H = 1.1 MHz (CR), f_L = 30 kHz (CR)	2.4	3.0	3.6	V
Oscillation Frequency	f_L	V_{DD} = 3.0 V, R_f = 470kΩ (* 1)	—	30	—	kHz
	f_H	V_{DD} = 3.0 V (* 2)	0.4	1.1	1.6	MHz

(* 1) : Internal crystal oscillation circuit is used for low-speed oscillator (with external R).
(* 2) : Internal CR oscillator is used for high-speed oscillator.

(Current consumption)

CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN	TYP.	MAX	UNIT
Power Supply Voltage	I_{DD} op	V_{DD} = 3.0 V CPM3 mode	Display ON	—	0.85	1.5	mA
			Display OFF	—	—	1.5	
	I_{DD} SLOW	V_{DD} = 3.0 V CPM1 mode	Display ON	—	23.0	40.0	μA
			Display OFF	—	—	39.0	
	I_{DD} HOLD	V_{DD} = 3.0 V In HALT mode	Display ON	—	9.0	16.0	
			Display OFF	—	—	14.0	
	I_{DD} STOP	V_{DD} = 3.0 V In STOP mode		—	0.8	1.4	

3-3. Specification for 3-V remote controller (Single clock)

L-OSC : 36.864 kHz (X'tal)

(Recommended operating conditions)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Power Supply Voltage	V_{DD}	f_L = 36.864 kHz (X'tal)	1.8	3.0	3.6	V
Oscillation Frequency	f_L	V_{DD} = 3.0 V	—	36.864	—	kHz

(Oscillation characteristics)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Oscillation Start Voltage (low-speed)	V_{sta1}	t_{sta} = 10 s	—	—	1.8	V
Oscillation Hold Voltage (low-speed)	V_{hold1}		1.8	—	—	V

(Current consumption)

CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN	TYP.	MAX	UNIT
Power Supply Voltage	I_{DD} op	V_{DD} = 3.0 V CPM1 mode	Display ON	—	23.0	40.0	μA
			Display OFF	—	—	39.0	
	I_{DD} HOLD	V_{DD} = 3.0 V In HALT mode	Display ON	—	6.5	14.0	
			Display OFF	—	—	12.0	

3-4. Specifications for 3.0-V remote controller (Dual clock)

H-OSC : 2 MHz (with X'tal), L-OSC : 32.768 kHz (with X'tal)

(Recommended operating conditions)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Power Supply Voltage	V_{DD}	f_H = 2 MHz (X'tal), f_L = 32.768 kHz (X'tal)	2.4	3.0	3.6	V
Oscillation Frequency	f_L	V_{DD} = 3.0 V	—	32.768	—	kHz
	f_H	V_{DD} = 3.0 V	—	2.0	—	MHz

(Oscillation characteristics)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Oscillation Start Voltage (low-speed)	V_{sta1}	t_{sta} = 10 s	—	—	2.0	V
Oscillation Hold Voltage (low-speed)	V_{hold1}		2.0	—	—	V
Oscillation Start Voltage (high-speed)	V_{sta2}	t_{sta} = 8 ms	—	—	2.4	V
Oscillation Hold Voltage (high-speed)	V_{hold2}		2.4	—	—	V

(Current consumption)

CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN	TYP.	MAX	UNIT
Power Supply Voltage	I_{DD} op	V_{DD} = 3.0 V CPM3 mode	Display ON	—	0.85	1.2	mA
			Display OFF	—	—	1.2	
	I_{DD} SLOW	V_{DD} = 3.0 V CPM1 mode	Display ON	—	17.0	24.0	μA
			Display OFF	—	—	23.0	
	I_{DD} HOLD	V_{DD} = 3.0 V In HALT mode	Display ON	—	7.0	12.0	
			Display OFF	—	—	11.0	
	I_{DD} STOP	V_{DD} = 3.0 V In STOP mode		—	0.8	1.2	

3-5. Specifications for 3.0-V remote controller (Dual clock)

H-OSC : 455 kHz (with X'tal), L-OSC : 32.768 kHz (with X'tal)

(Recommended operating conditions)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Power Supply Voltage	V_{DD}	f_H = 1 MHz (X'tal), f_L = 32.768 kHz (X'tal)	2.2	3.0	3.6	V
Oscillation Frequency	f_L	V_{DD} = 3.0 V	—	32.768	—	kHz
	f_H	V_{DD} = 3.0 V	—	455	—	kHz

(Oscillation characteristics)

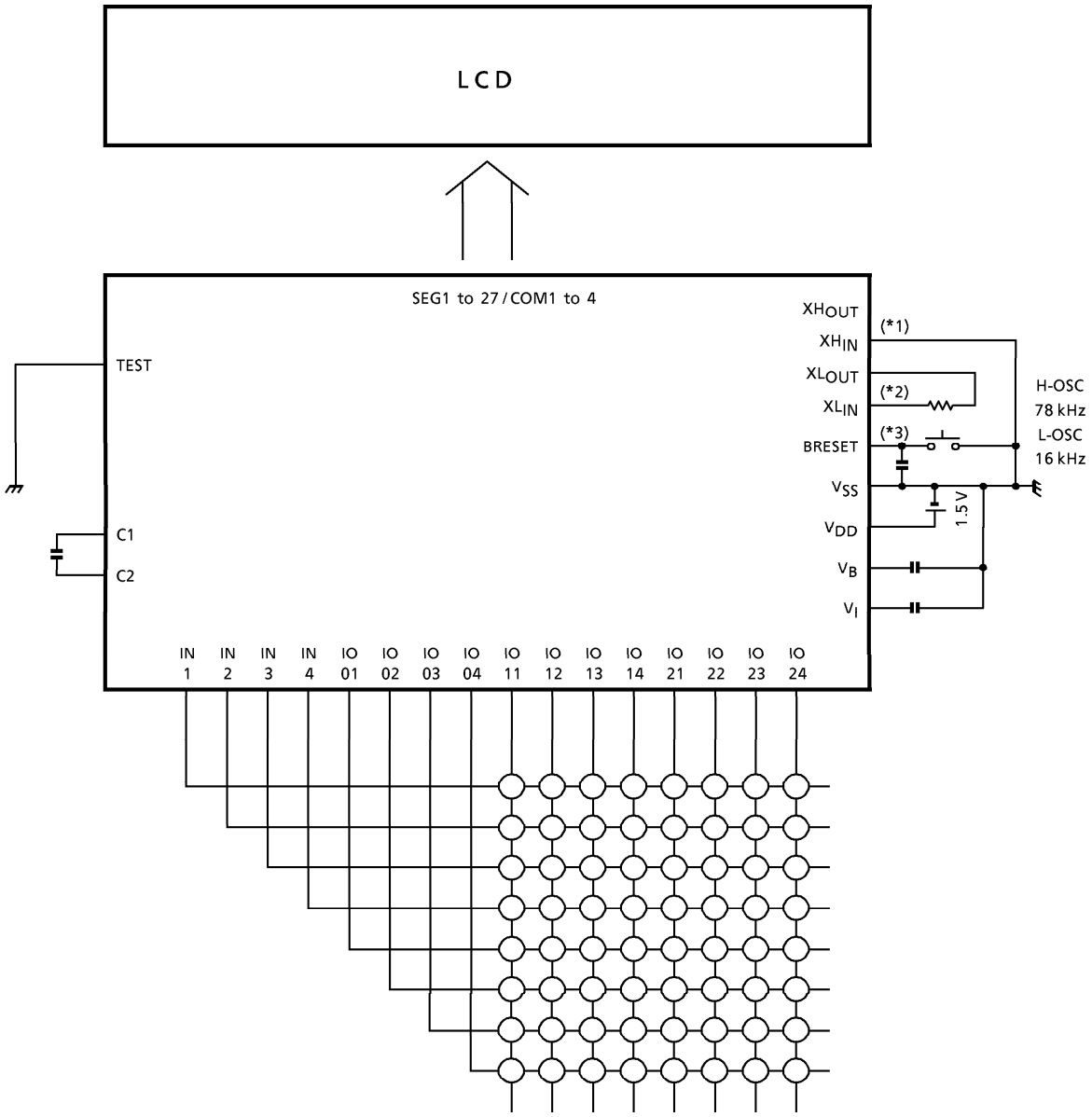
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Oscillation Start Voltage (low-speed)	V_{sta1}	t_{sta} = 10 s	—	—	2.0	V
Oscillation Hold Voltage (low-speed)	V_{hold1}		2.0	—	—	V
Oscillation Start Voltage (high-speed)	V_{sta2}	t_{sta} = 8 ms	—	—	2.2	V
Oscillation Hold Voltage (high-speed)	V_{hold2}		2.2	—	—	V

(Current consumption)

CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN	TYP.	MAX	UNIT
Power Supply Voltage	I_{DD} op	V_{DD} = 3.0 V CPM3 mode	Display ON	—	0.5	1.0	mA
			Display OFF	—	—	1.0	
	I_{DD} SLOW	V_{DD} = 3.0 V CPM1 mode	Display ON	—	17.0	24.0	μA
			Display OFF	—	—	23.0	
	I_{DD} HOLD	V_{DD} = 3.0 V In HALT mode	Display ON	—	7.0	12.0	
			Display OFF	—	—	11.0	
	I_{DD} STOP	V_{DD} = 3.0 V In STOP mode		—	0.8	1.2	

EXAMPLE OF APPLICATION CIRCUIT (1)

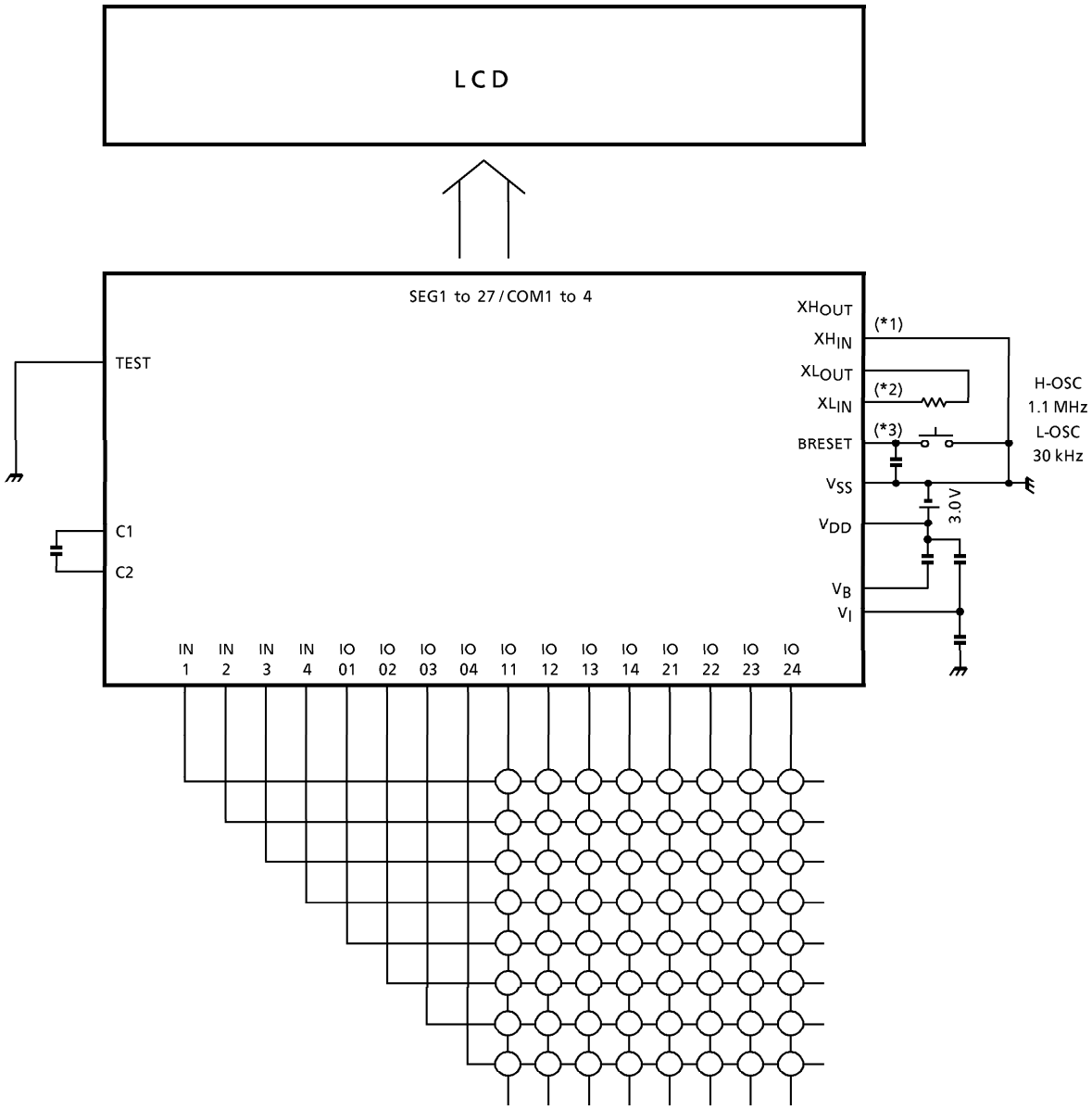
Calculator 1 (1.5 V)



(*1) : When internal CR oscillator is used for high-speed oscillator, XH_{IN} is connected to GND.
(*2) : Insert a resistor (Rf = 470 kΩ) between XL_{IN} and XL_{OUT}.
(*3) : A 0.1-μF capacitor is connected between BRESET and V_{SS}.
(*4) : A 0.1-μF capacitor is used for quadrupler.

EXAMPLE OF APPLICATION CIRCUIT (2)

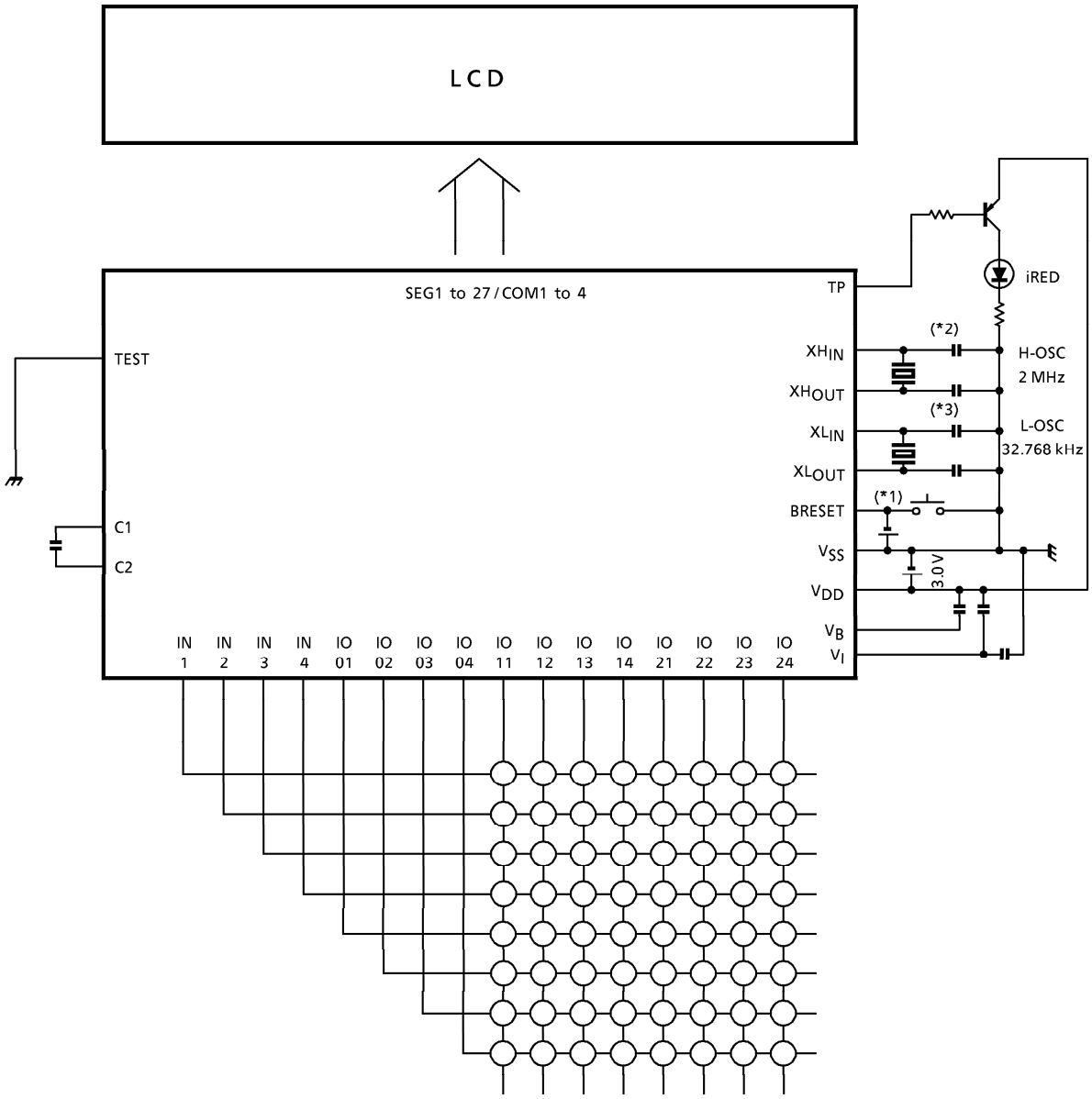
Calculator 2 (3.0 V)



(*1) : When internal CR oscillator is used for high-speed oscillator, XH_{IN} is connected to GND.
(*2) : Insert a resistor (Rf = 470 kΩ) between XL_{IN} and XL_{OUT}.
(*3) : A 0.1-μF capacitor is connected between BRESET and V_{SS}.
(*4) : A 0.1-μF capacitor is used for quadrupler.

EXAMPLE OF APPLICATION CIRCUIT (3)

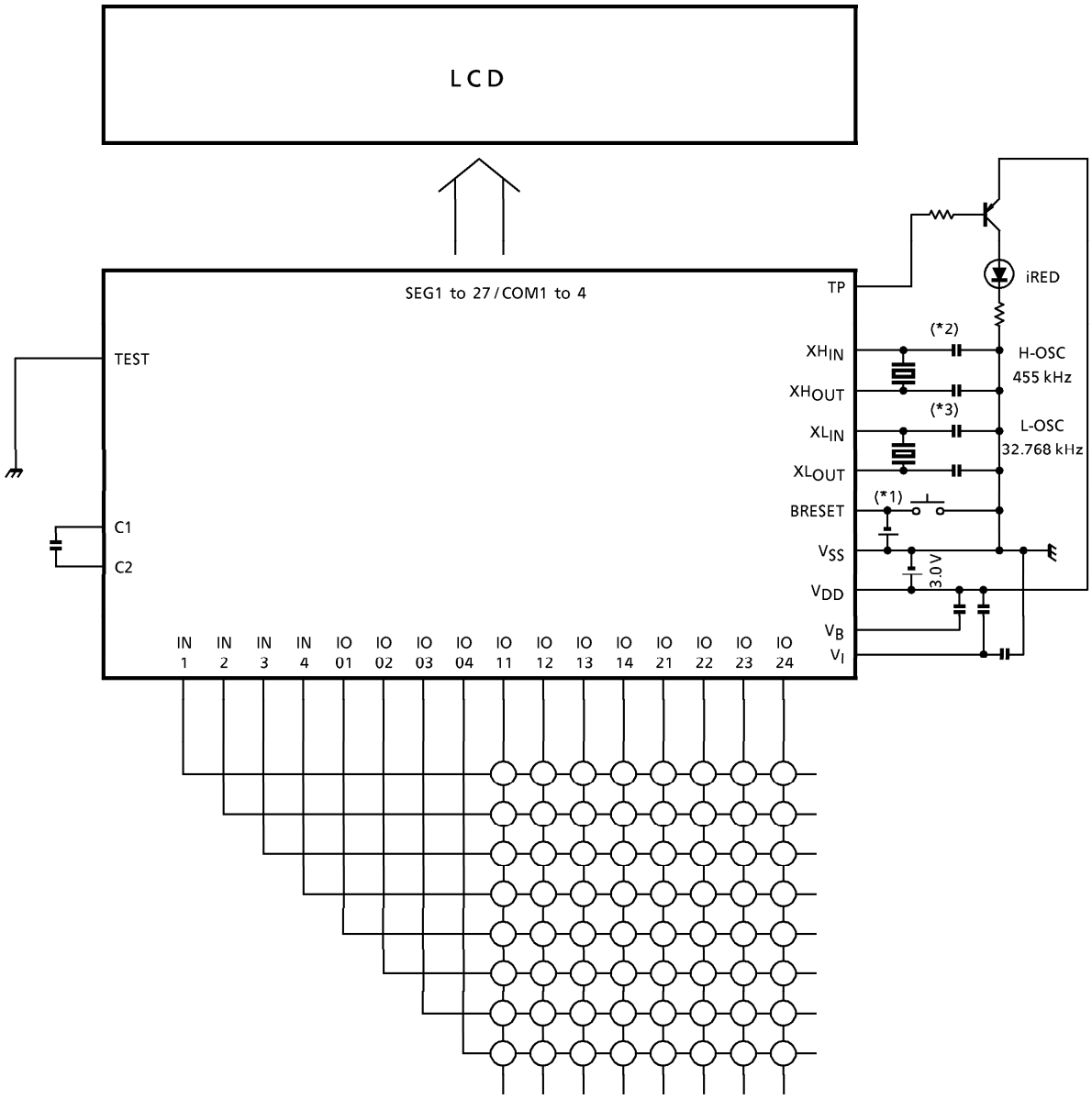
Remote controller 1 (V_{DD} = 3.0 V, f_H = 2 MHz, f_L = 32.768 kHz)



(*1) : A 0.1-μF capacitor is connected between BRESET and V_{SS}.
(*2) : Recommended high-speed oscillator circuit capacitor : 22 pF
(*3) : Recommended low-speed oscillator circuit capacitor : 15 pF
(*4) : A 0.1-μF capacitor is used for quadrupler.

EXAMPLE OF APPLICATION CIRCUIT (4)

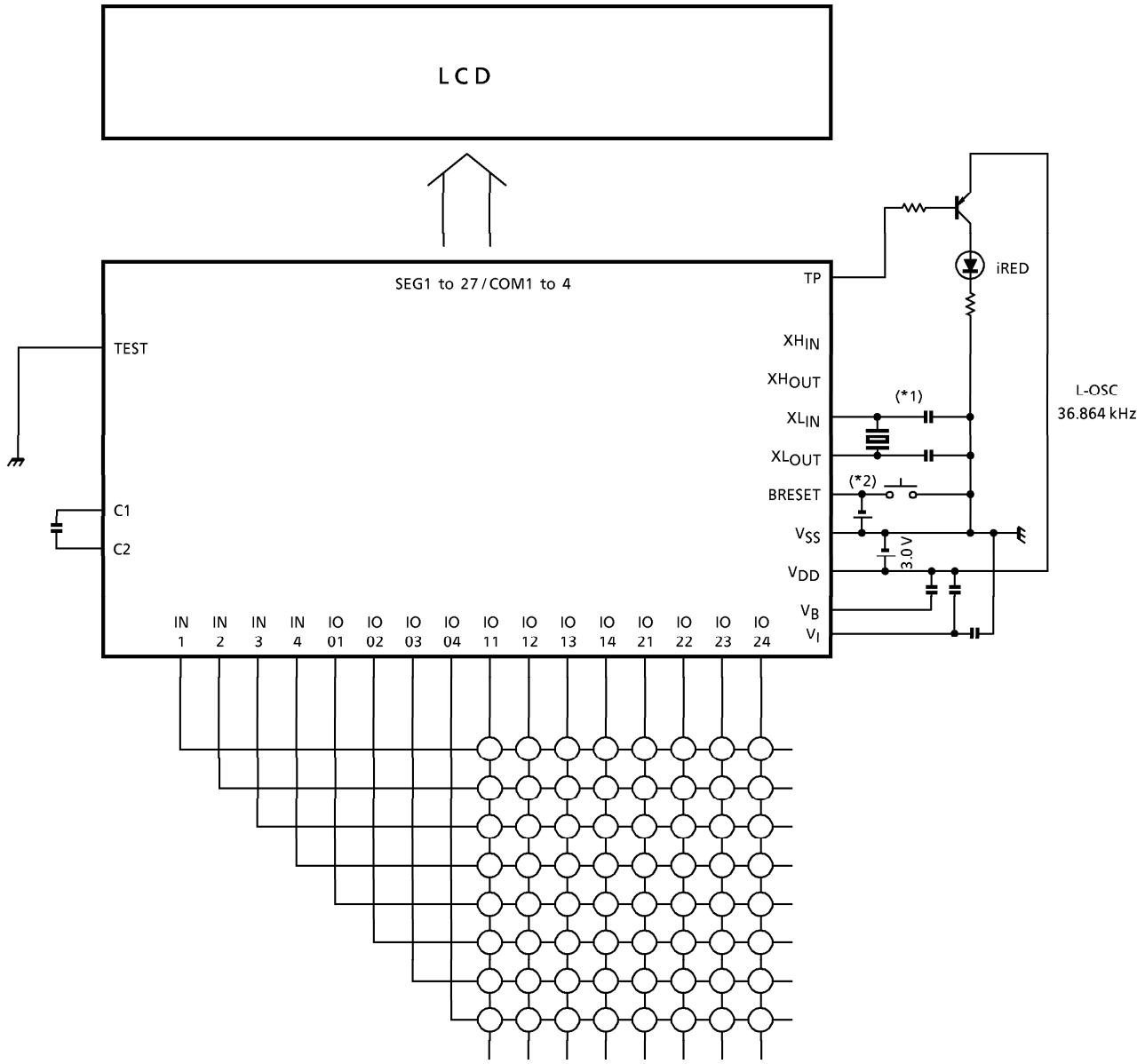
Remote controller 2 (V_{DD} = 3.0 V, f_H = 455 kHz, f_L = 32.768 kHz)



(*1) : A 0.1-μF capacitor is connected between BRESET and V_{SS}.
(*2) : Recommended high-speed oscillator circuit capacitor : 22 pF
(*3) : Recommended low-speed oscillator circuit capacitor : 15 pF
(*4) : A 0.1-μF capacitor is used for quadrupler.

EXAMPLE OF APPLICATION CIRCUIT (5)

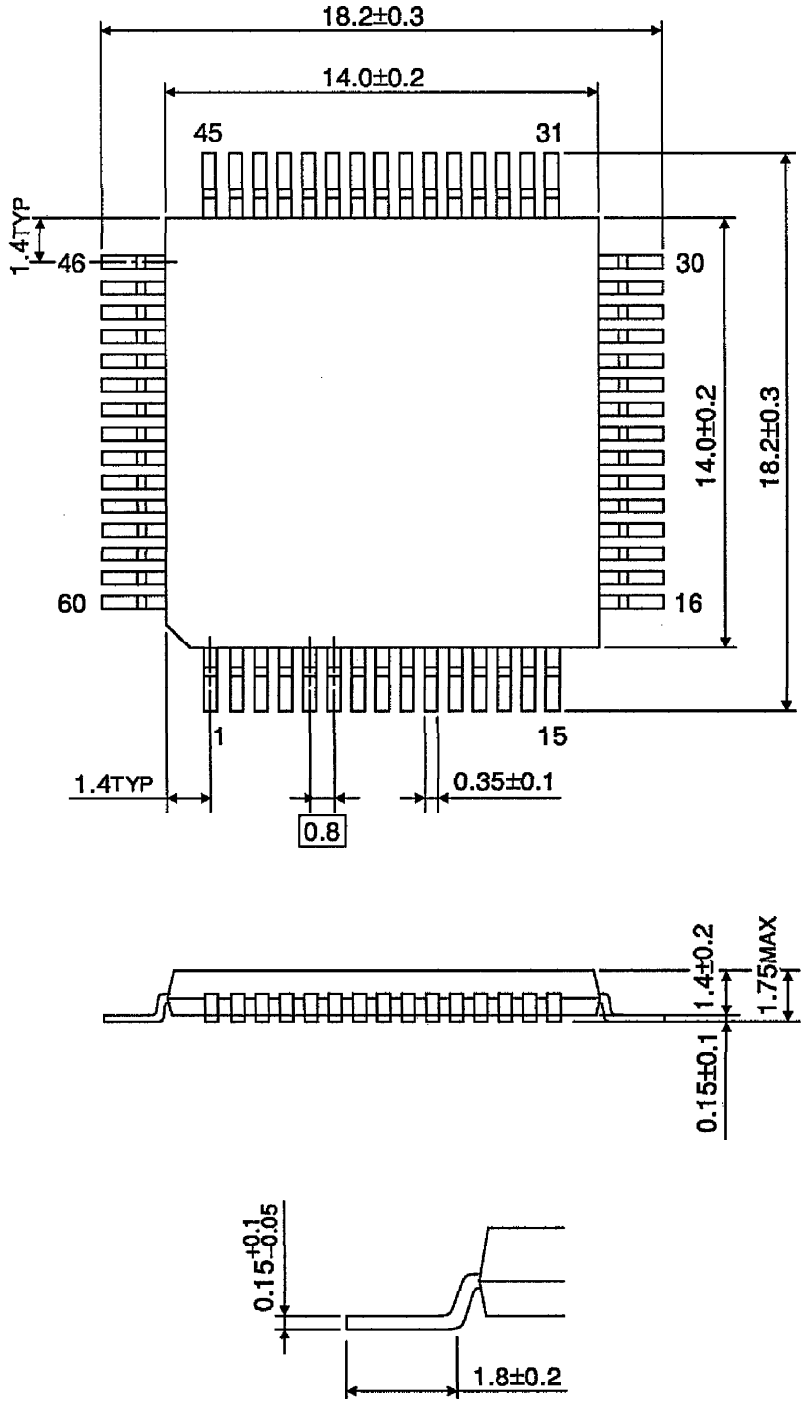
Remote controller 3 (V_{DD} = 3.0 V, f_L = 36.864 kHz)



(*1) : Recommended low-speed oscillator circuit capacitor : 15 pF
(*2) : A 0.1-μF capacitor is connected between BRESET and V_{SS}.
(*3) : A 0.1-μF capacitor is used for quadrupler.

PACKAGE DIMENSIONS

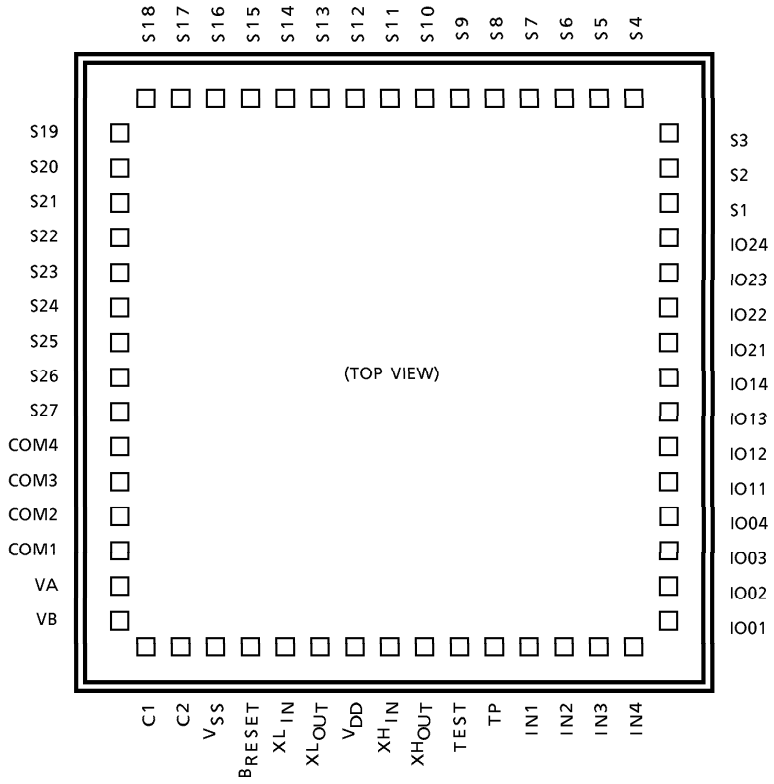
LQFP60-P-1414-0.80 Unit : mm



Weight : g (Typ.)

BARE CHIP

1. Pad assignment



Chip size 3.41 × 3.88 (mm)
Chip thickness 450 ± 30 (μm)

Substrate voltage V_{SS}

2. Pad location table

($\times 10^{-3}$ mm)

No.	PAD NAME	X POINT	Y POINT
1	C1	– 1567	1251
2	C2	– 1567	1006
3	V_{SS}	– 1567	799
4	BRESET	– 1567	600
5	XL_{IN}	– 1567	450
6	XL_{OUT}	– 1567	300
7	V_{DD}	– 1567	150
8	XH_{IN}	– 1567	0
9	XH_{OUT}	– 1567	– 150
10	TEST	– 1567	– 300
11	TP	– 1567	– 480
12	IN1	– 1567	– 658
13	IN2	– 1567	– 808
14	IN3	– 1567	– 1006
15	IN4	– 1567	– 1251
16	IO01	– 1336	– 1805
17	IO02	– 1072	– 1805
18	IO03	– 846	– 1805
19	IO04	– 648	– 1805
20	IO11	– 460	– 1805
21	IO12	– 300	– 1805
22	IO13	– 150	– 1805
23	IO14	0	– 1805
24	IO21	150	– 1805
25	IO22	300	– 1805
26	IO23	460	– 1805
27	IO24	648	– 1805
28	S27 (OUT4)	846	– 1805
29	S26 (OUT3)	1072	– 1805
30	S25 (OUT2)	1336	– 1805

No.	PAD NAME	PAD NAME	X POINT
31	S24 (OUT1)	1567	– 1251
32	S23	1567	– 1006
33	S22	1567	– 799
34	S21	1567	– 601
35	S20	1567	– 450
36	S19	1567	– 300
37	S18	1567	– 150
38	S17	1567	0
39	S16	1567	150
40	S15	1567	300
41	S14	1567	450
42	S13	1567	600
43	S12	1567	799
44	S11	1567	1006
45	S10	1567	1251
46	S9	1336	1805
47	S8	1072	1805
48	S7	846	1805
49	S6	648	1805
50	S5	460	1805
51	S4	300	1805
52	S3	150	1805
53	S2	0	1805
54	S1	– 150	1805
55	COM4	– 300	1805
56	COM3	– 460	1805
57	COM2	– 648	1805
58	COM1	– 846	1805
59	VA	– 1072	1805
60	VB	– 1336	1805