LH5316500A

CMOS 16M (2M × 8 / 1M × 16)
Mask-Programmable ROM

FEATURES

- 2,097,152 × 8 bit organization
  (Byte mode)
  1,048,576 × 16 bit organization
  (Word mode)
- Access time: 150 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Package:
  42-pin, 600-mil DIP
  44-pin, 600-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)

DESCRIPTION

The LH5316500A is a 16M-bit mask-programmable ROM organized as 2,097,152 × 8 bits (Byte mode) or 1,048,576 × 16 bits (Word mode) that can be selected by a $\overline{BYTE}$ input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

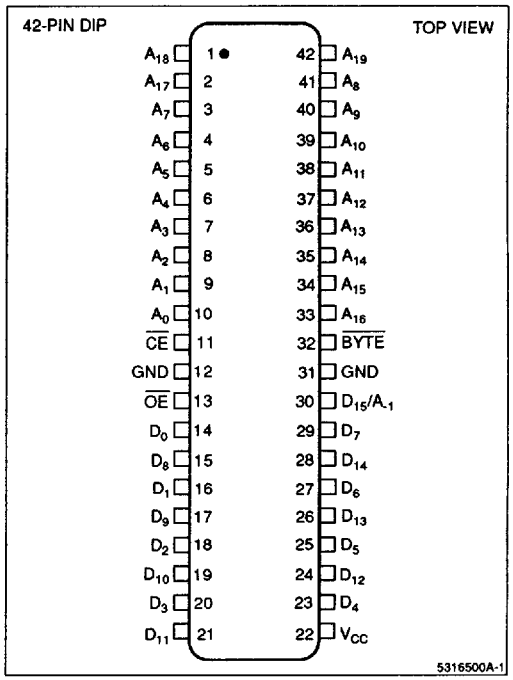


Figure 1. Pin Connections for DIP Package

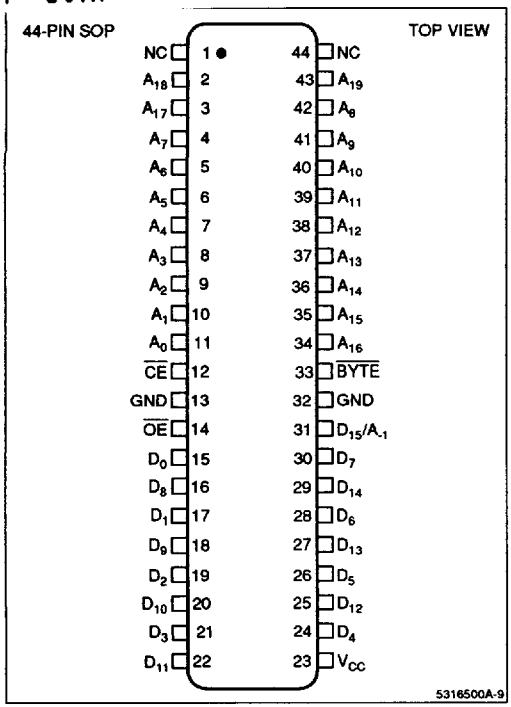


Figure 2. Pin Connections for SOP Package

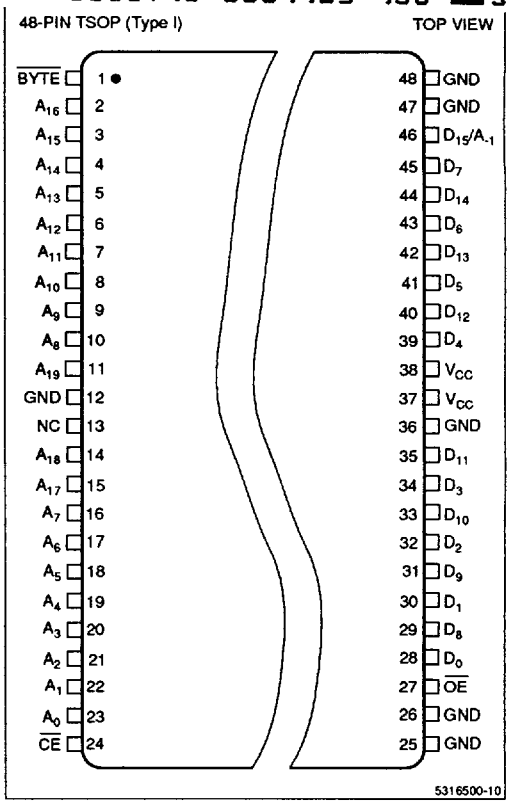


Figure 3. Pin Connections for TSOP Package

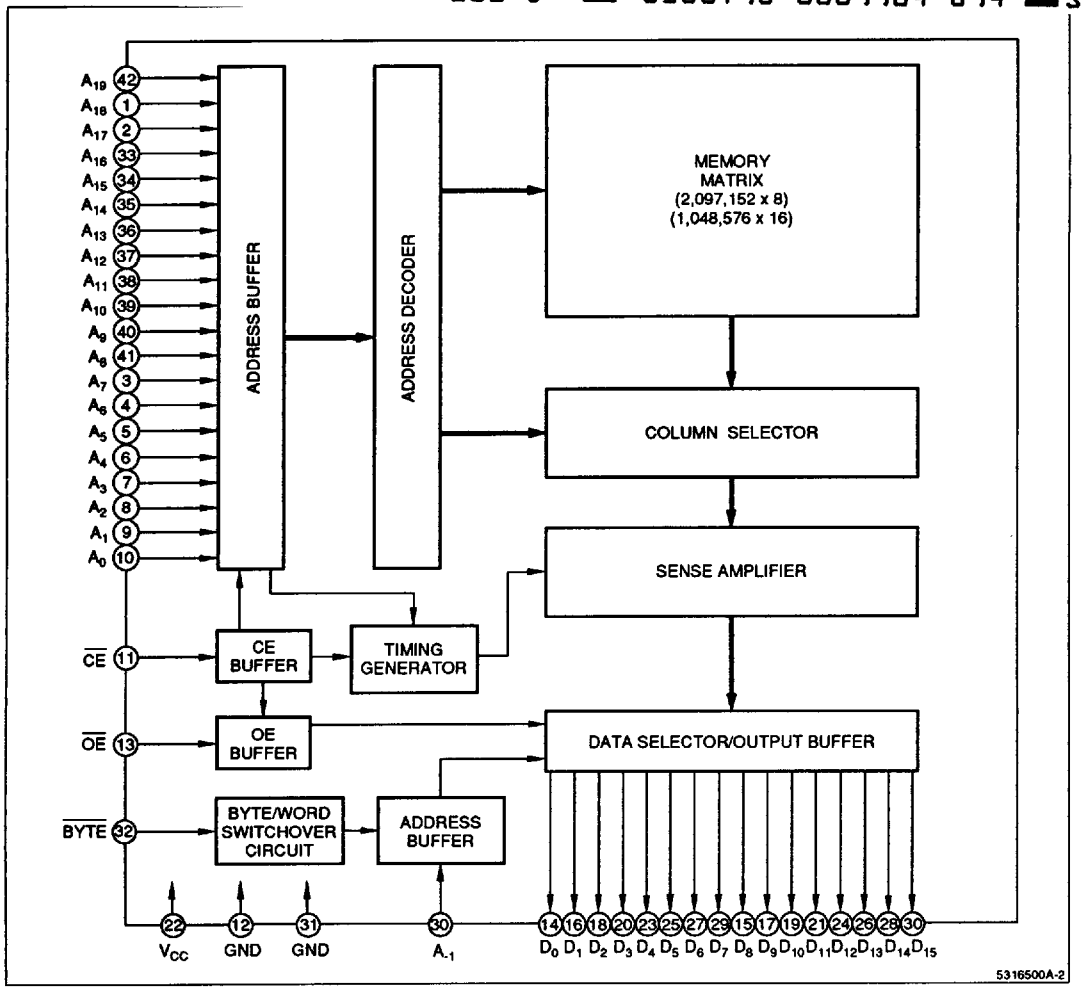


Figure 4. LH5316500A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_{-1} - A_{19}	Address input
D_0 - D_{15}	Data output
$\overline{BYTE}$	Byte/word switch
$\overline{CE}$	Chip Enable input

SIGNAL	PIN NAME
$\overline{OE}$	Output Enable input
V_{CC}	Power supply (+5 V)
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1} (D_{15})	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
				D_0 - D_7	D_8 - D_{15}	LSB	MSB	
H	X	X	X	High-Z	High-Z	–	–	Standby (I_{SB})
L	H	X	X	High-Z	High-Z	–	–	Operating (I_{CC})
L	L	H	–	D_0 - D_7	D_8 - D_{15}	A_0	A_{19}	Operating (I_{CC})
L	L	L	L	D_0 - D_7	High-Z	A_{-1}	A_{19}	Operating (I_{CC})
L	L	L	H	D_8 - D_{15}	High-Z	A_{-1}	A_{19}	Operating (I_{CC})

NOTES:
X = H or L; High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}		2.2	V_{CC} +0.3	V	
Input 'Low' voltage	V_{IL}		-0.3	0.8	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4		V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns		50	mA	2
	I_{CC2}	t_{RC} = 1 µs		40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	
Input capacitance	C_{IN}	f = 1 MHz, t_A = 25°C		10	pF	
Output capacitance	C_{OUT}			10	pF	

NOTES:
1. $\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, outputs open
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150		ns	
Address access time	t_{AA}		150	ns	
Chip enable time	t_{ACE}		150	ns	
Output enable time	t_{OE}		70	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		60	ns	1
OE to output in High-Z	t_{OHZ}		60	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL + 100 pF

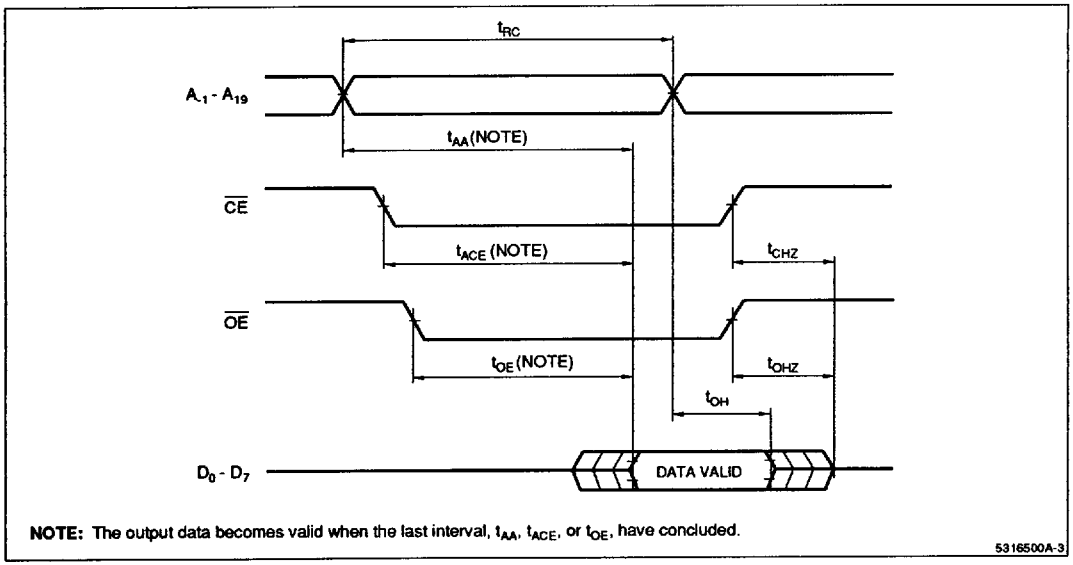
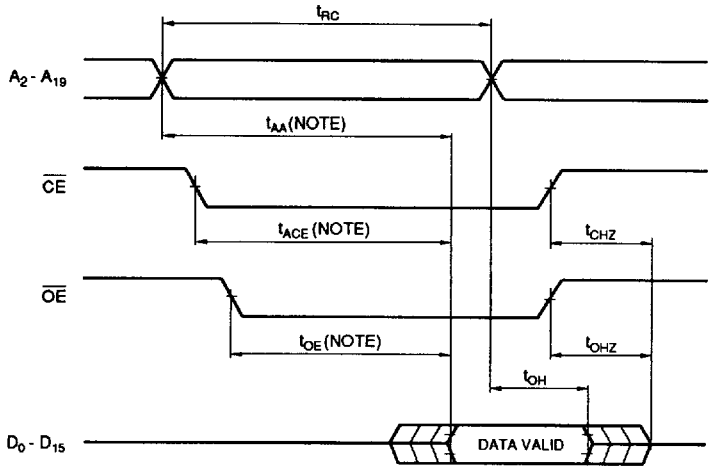


Figure 5. Byte Mode ($\overline{BYTE}$ = V_{IL})

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.



NOTE: The output data becomes valid when the last interval, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

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Figure 6. Word Mode ($\overline{BYTE}$ = V_{IH})

ORDERING INFORMATION

LH5316500A	X	- ##
Device Type	Package	Speed

- Speed: 15 150 Access Time (ns)
- Package:
  - D 42-pin, 600-mil DIP (DIP42-P-600)
  - N 44-pin, 600-mil SOP (SOP44-P-600)
  - T 48-pin, 12 x 18 mm² TSOP (Type I) (TSOP48-P-1218)
- Device Type: CMOS 16M (2M x 8 OR 1M x 16) Mask-Programmable ROM

Example: LH5316500AD-15 (CMOS 16M (2M x 8) Mask-Programmable ROM, 150 ns, 42-pin, 600-mil DIP)

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