LH52D1000

CMOS 1M (128K × 8) Static Ram

FEATURES

- Access time: 85 ns (MAX.), 100 ns (MAX.)
- Current consumption:
  Operating: 40 mA (MAX.)
  6 mA (MAX.) (t_{RC}, t_{WC} = 1 µs)
  Standby: 45 µA (MAX.)
- Data Retention:
  1.0 µA (MAX. V_{CCDR} = 3 V, t_A = 25°C)
- Single power supply: 2.7 V to 3.6 V
- Operating temperature: -40°C to +85°C
- Fully-static operation
- Three-state output
- Not designed or rated as radiation hardened
- Packages:
  32-pin 8 × 20 mm² TSOP
  32-pin 8 × 13.4 mm² STSOP
- N-type bulk silicon

DESCRIPTION

The LH52D1000 is a static RAM organized as 131,072 × 8 bits which provides low-power standby mode. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

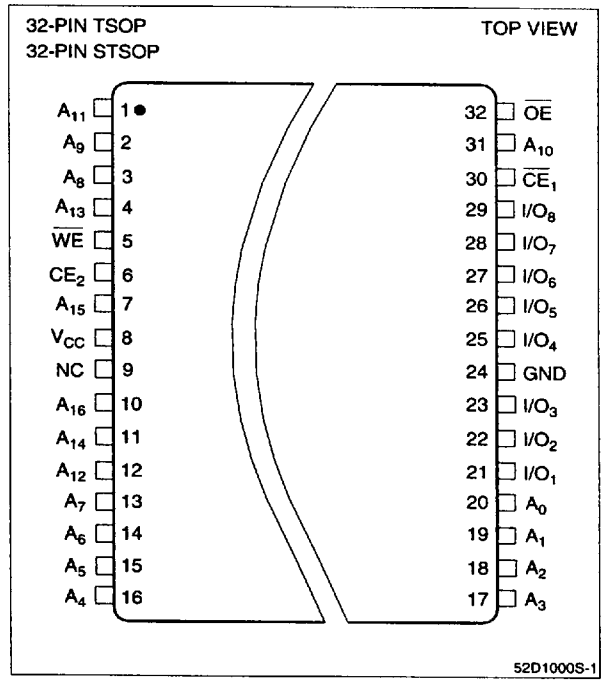


Figure 1. Pin Connections for TSOP and STSOP Packages

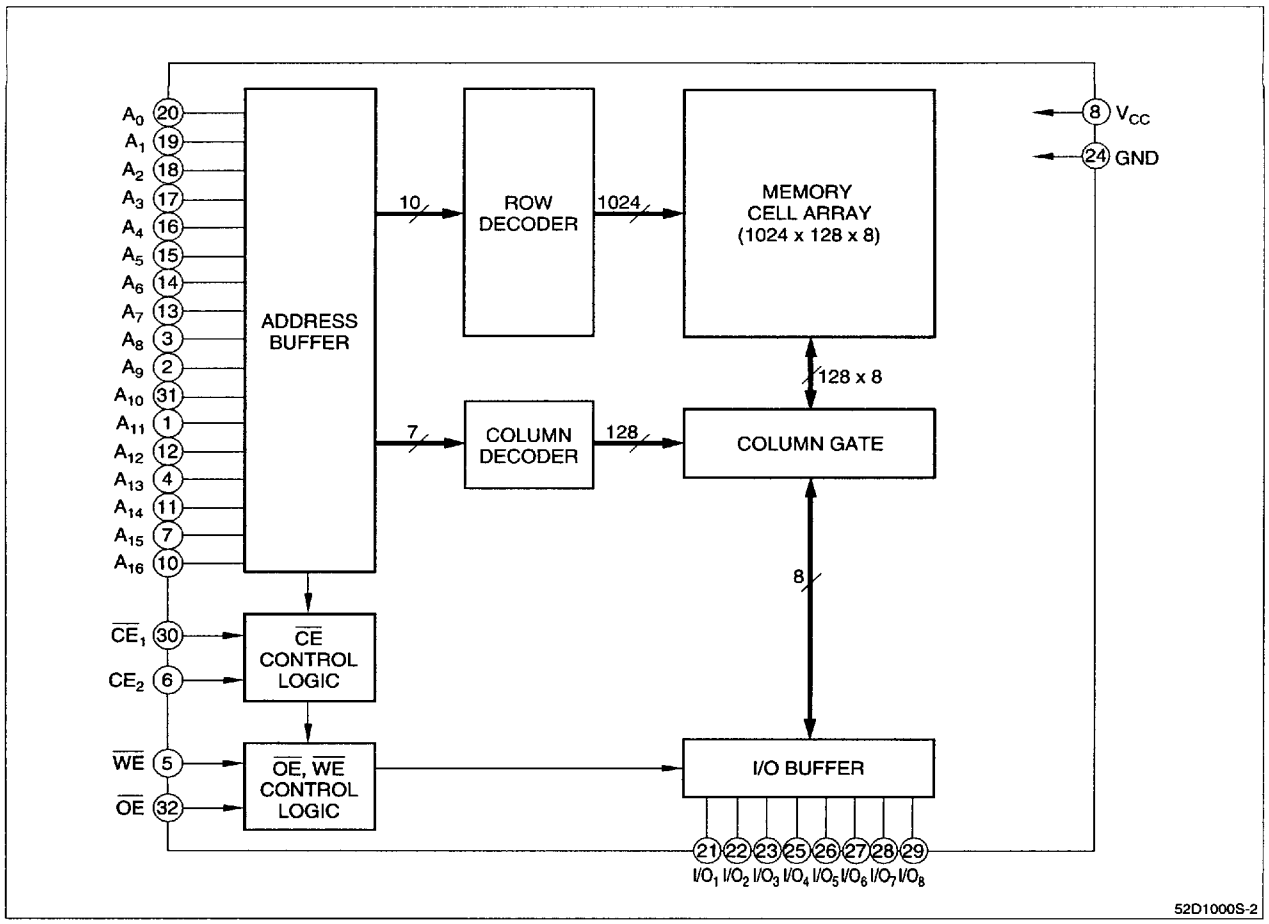


Figure 2. LH52D1000 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	SIGNAL	PIN NAME
$A_0 - A_{16}$	Address inputs	$I/O_1 - I/O_8$	Data inputs and outputs
CE_1	Chip enable 1	V_{CC}	Power supply
CE_2	Chip enable 2	GND	Ground
WE	Write enable	NC	No connection
OE	Output enable		

TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	$I/O_1 - I/O_8$	SUPPLY CURRENT	NOTE
H	—	—	—	Standby	High impedance	Standby (I_{SB})	1
—	L	—	—				
L	H	L	—	Write	Data input	Active (I_{CC})	1
L	H	H	L	Read	Data output	Active (I_{CC})	—
L	H	H	H	Output disable	High impedance	Active (I_{CC})	—

NOTE:
1. — = Don't care
   L = Low
   H = High

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +4.6	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V	1, 2
Operating temperature	T_{OPR}	-40 to +85	°C	—
Storage temperature	T_{STG}	-55 to +150	°C	—

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.
2. Undershoot of -3.0 V is allowed width of pulse below 50 ns.

RECOMMENDED DC OPERATING CONDITIONS (T_A = -40°C to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	2.7	3.0	3.6	V	—
Input voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V	—
	V_{IL}	−0.3	—	0.6	V	1

NOTE:
1. Undershoot of −3.0 V is allowed width of pulse below 50 ns.

DC ELECTRICAL CHARACTERISTICS (T_A = -25°C to +85°C, V_{CC} = 2.7 V to 3.6 V)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input leakage current	I_{LI}	VIN = 0 to V_{CC}		−1.0	—	1.0	µA
Output leakage current	I_{LO}	$CE_1 = V_{IH}$ or $CE_2 = V_{IL}$ or OE = V_{IH} or WE = V_{IL} $V_{I/O}$ = 0 V to V_{CC}		−1.0	—	1.0	µA
Operating supply current	I_{CC}	$V_{IN} = V_{IL}$ or V_{IH}, $CE_1 = V_{IL}$, WE = V_{IH} $CE_2 = V_{IH}$, $I_{I/O}$ = 0 mA	t_{CYCLE} = Min	—	—	40	mA
	I_{CC1}	CE_1 = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2, WE = V_{CC} - 0.2 V, $I_{I/O}$ = 0 mA	t_{CYCLE} = 1.0 µs	—	—	6	
Standby current	I_{SB}	$CE_1 = V_{CC} - 0.2$ V or CE_2 = 0.2 V		—	—	45	µA
	I_{SB1}	$CE_1 = V_{IH}$ or $CE_2 = V_{IL}$		—	—	2.0	mA
Output voltage	V_{OL}	I_{OL} = 2.1 mA		—	—	0.4	V
	V_{OH}	I_{OH} = −0.5 mA		V_{CC} - 0.5	—	—	V

AC ELECTRICAL CHARACTERISTICS
AC Test Conditions

PARAMETER	MODE	NOTE
Input pulse level	0.4 V to 2.4 V	—
Input rise and fall time	5 ns	—
Input and output timing Ref. level	1.5 V	—
Output load	100 pF + 1TTL	1

NOTE:
1. Including scope and jig capacitance.

READ CYCLE (T_A = -40°C to +85°C, V_{CC} = 2.7 V to 3.6 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	85		ns	—
Address access time	t_{AA}	—	85	ns	—
CE_1 access time	t_{ACE1}	—	85	ns	—
CE_2 access time	t_{ACE2}	—	85	ns	—
Output enable to output valid	t_{OE}	—	45	ns	—
Output hold from address change	t_{OH}	10	—	ns	—
CE_1 Low to output active	t_{LZ1}	5	—	ns	1
CE_2 High to output active	t_{LZ2}	5	—	ns	1
OE Low to output active	t_{OLZ}	0	—	ns	1
CE_1 High to output in High impedance	t_{HZ1}	0	35	ns	1
CE_2 Low to output in High impedance	t_{HZ2}	0	35	ns	1
OE High to output in High impedance	t_{OHZ}	0	35	ns	1

NOTE:
1. Active output to High impedance and High impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

WRITE CYCLE (T_A = -40°C to +85°C, V_{CC} = 2.7 V to 3.6 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	85	—	ns	—
CE_1 Low to end of write	t_{CW1}	75	—	ns	—
CE_2 High to end of write	t_{CW2}	75	—	ns	—
Address setup time	t_{AS}	0	—	ns	—
Write pulse width	t_{WP}	60	—	ns	—
Write recovery time	t_{WR}	0	—	ns	—
Input data setup time	t_{DW}	35	—	ns	—
Input data hold time	t_{DH}	0	—	ns	—
WE High to output active	t_{OW}	0	—	ns	1
WE Low to output in High impedance	t_{WZ}	0	—	ns	1
OE High to output in High impedance	t_{OHZ}	0	35	ns	1

NOTE:
1. Active output to High impedance and High impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

DATA RETENTION CHARACTERISTICS (T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP	MAX.	UNIT	NOTE
Data retention supply voltage	V_{CCDR}	$CE_2 \le 0.2$ V or $CE_1 \ge V_{CCDR} - 0.2$ V		2.0	—	3.6	V	1
Data retention supply current	I_{CCDR}	V_{CCDR} = 3.0 V, $CE_2 \le 0.2$ V or $CE_1 \ge V_{CCDR} - 0.2$ V	T_A = 25°C	—	—	1.0	µA	1
			T_A = 40°C	—	—	3.0 35		
Chip enable setup time	t_{CDR}	—		0	—	—	ms	—
Chip enable hold time	t_R	—		5	—	—	ms	—

NOTE:
1. $CE_2 \ge V_{CCDR} - 0.2$ V or $CE_2 \le 0.2$ V
2. Typical values at T_A = 25°C

PIN CAPACITANCE (T_A = 25°C, f = 1 MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input capacitance	C_{IN}	V_{IN} = 0 V	—	—	10	pF	1
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V	—	—	10	pF	1

NOTE:
1. This parameter is sampled and not production tested.

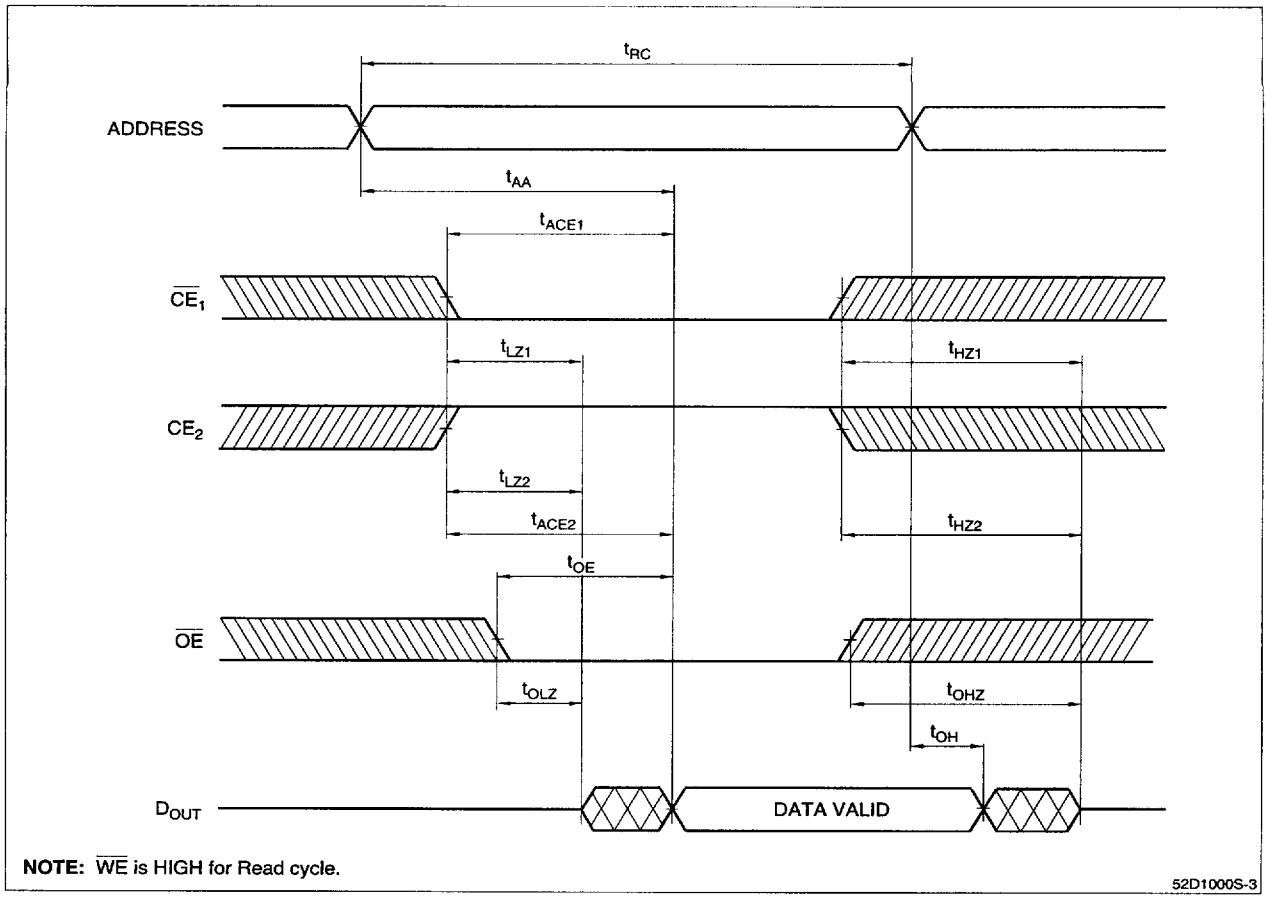
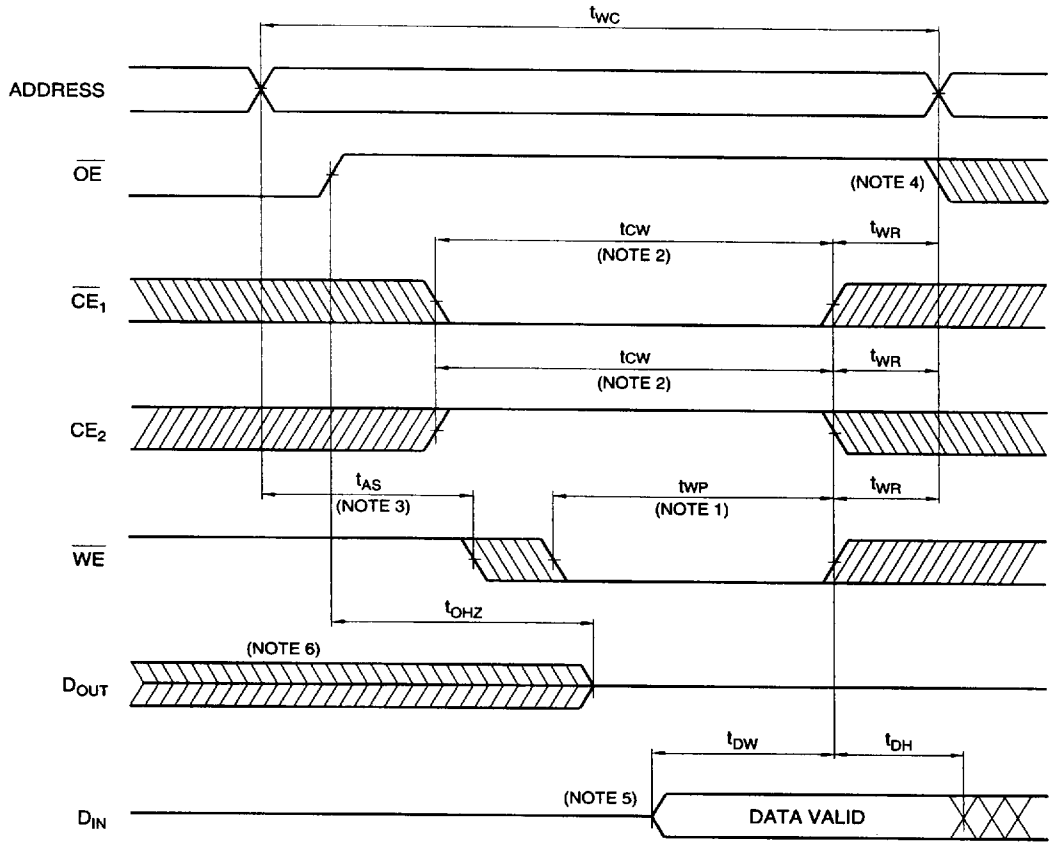


Figure 3. Read Cycle



NOTES:

1. A write occurs during the overlap of a LOW $\overline{CE}_1$, a HIGH CE_2 and a LOW $\overline{WE}$. A write begins at the latest transition among $\overline{CE}_1$ going LOW, CE_2 going HIGH and $\overline{WE}$ going LOW. A write ends at the earliest transition among $\overline{CE}_1$ going HIGH, CE_2 going LOW and $\overline{WE}$ going HIGH. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CE}_1$ going LOW or CE_2 going HIGH to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applies in case a write ends at $\overline{CE}_1$ or $\overline{WE}$ going HIGH. t_{WR2} applies in case a write ends at CE_2 going LOW.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CE}_1$ goes LOW simultaneously with $\overline{WE}$ going LOW or after $\overline{WE}$ going LOW, the outputs remain in high impedance state.
7. If $\overline{CE}_1$ goes HIGH simulaneously with $\overline{WE}$ going HIGH or before $\overline{WE}$ going HIGH, the outputs remain in high impedance state.

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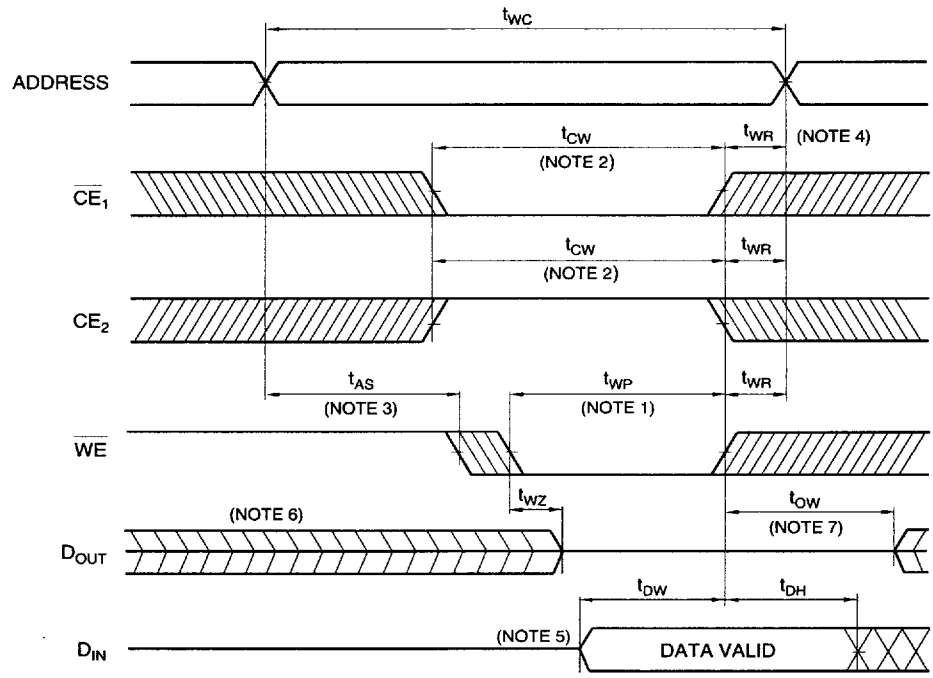
Figure 4. Write Cycle (OE Controlled)



NOTES:

1. A write occurs during the overlap of a LOW $\overline{CE}_1$, a HIGH CE_2 and a LOW $\overline{WE}$. A write begins at the latest transition among $\overline{CE}_1$ going LOW, CE_2 going HIGH and $\overline{WE}$ going LOW. A write ends at the earliest transition among $\overline{CE}_1$ going HIGH. CE_2 going LOW and $\overline{WE}$ going HIGH. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CE}_1$ going LOW or CE_2 going HIGH to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applies in case a write ends at $\overline{CE}_1$ or $\overline{WE}$ going HIGH. t_{WR2} applies in case a write ends at CE_2 going LOW.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CE}_1$ goes LOW simultaneously with $\overline{WE}$ going LOW or after $\overline{WE}$ going LOW, the outputs remain in high impedance state.
7. If $\overline{CE}_1$ goes HIGH simulaneously with $\overline{WE}$ going HIGH or before $\overline{WE}$ going HIGH, the outputs remain in high impedance state.

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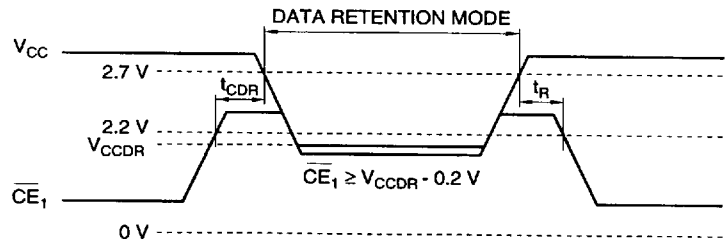
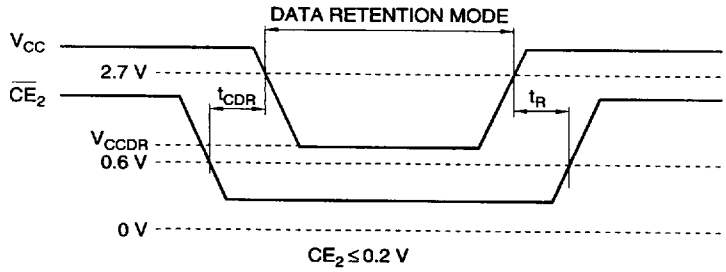
Figure 5. Write Cycle (OE Low Fixed)

$\overline{CE_1}$ CONTROL (NOTE)



CE_2 CONTROL



NOTE: To control the data retention mode at $\overline{CE}_1$, fix the input level of CE_2 between V_{CCDR} and V_{CCDR} - 0.2 V or 0 V to 0.2 V during the data retention mode.

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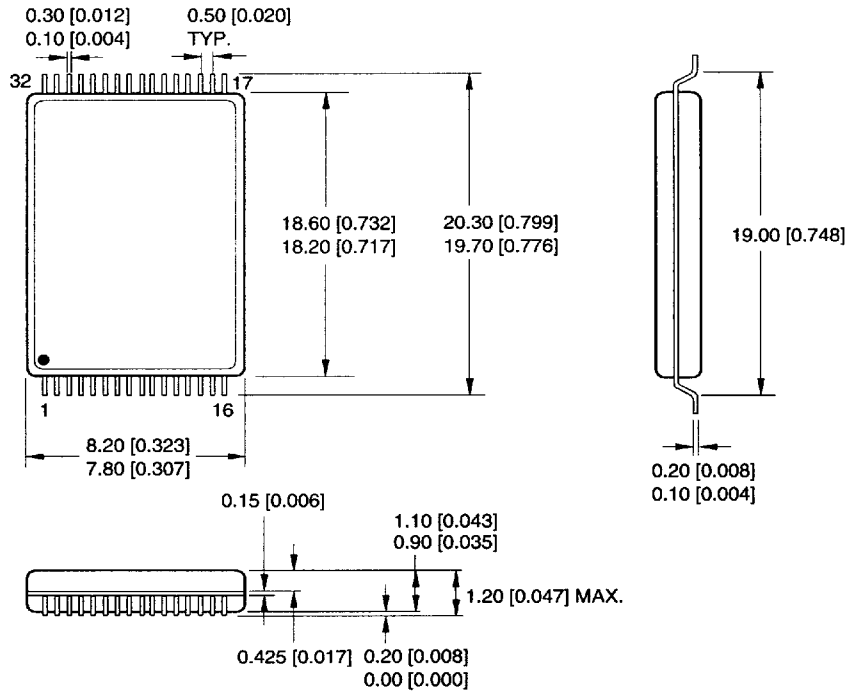
Figure 6. Data Retention (CE_1 Controlled)

PACKAGE DIAGRAM

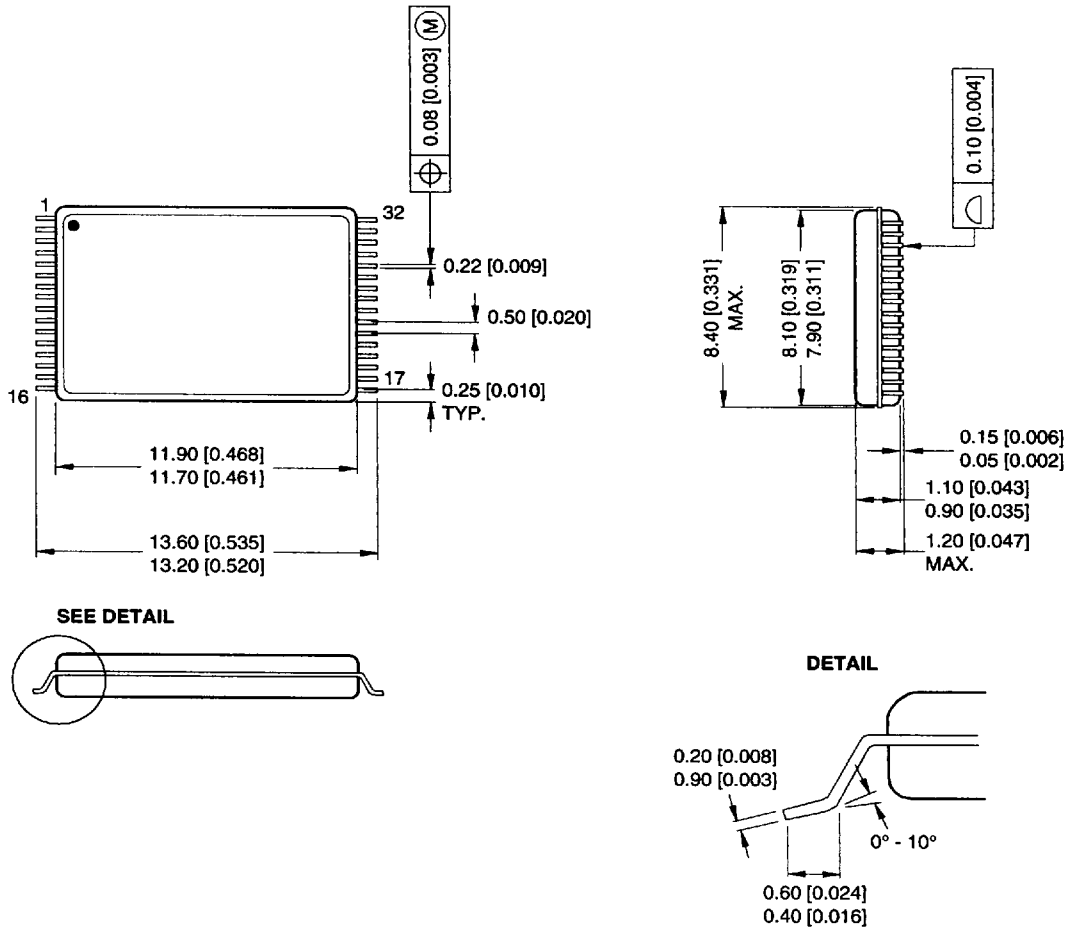
32TSOP (Type I) (TSOP032-P-0820)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

32TSOP

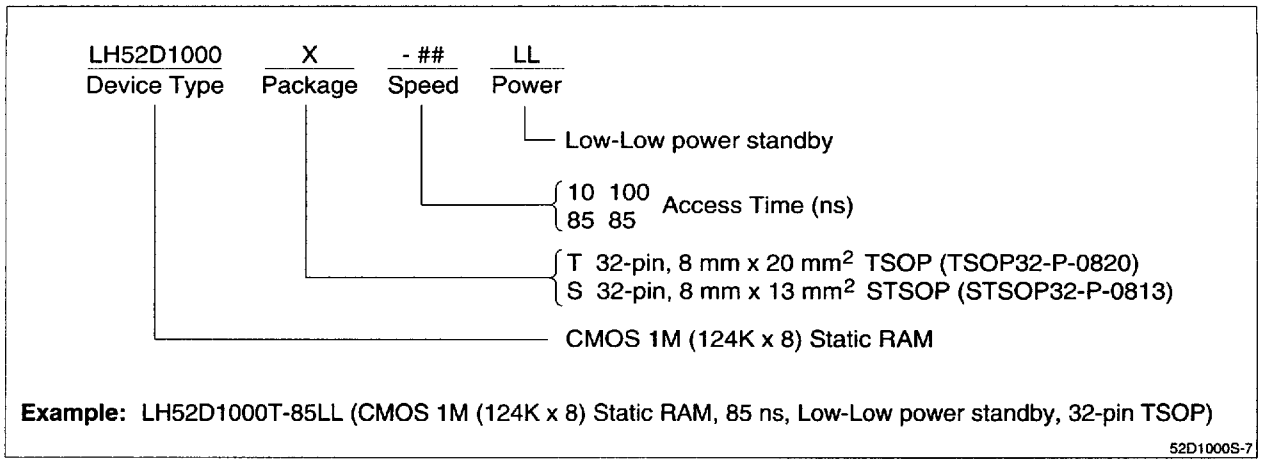
32TSOP (TSOP032-P-0813)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

32STSOP

ORDERING INFORMATION



Example: LH52D1000T-85LL (CMOS 1M (124K x 8) Static RAM, 85 ns, Low-Low power standby, 32-pin TSOP)

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