T-46-23-18

1M x 4-Bit Dynamic RAM

HYB 514400-80/-10

Preliminary

- 1 048 576 words by 4-bit organization
- Fast access and cycle time
  80 ns access time
  160 ns cycle time (HYB 514400-80)
  100 ns access time
  190 ns cycle time (HYB 514400-10)
- Fast page mode cycle time
  45 ns (HYB 514400-80)
  55 ns (HYB 514400-10)
- Single + 5 V (± 10 %) supply with a built-in V_{CC} generator
- Low power dissipation
  max. active 578 mW (HYB 514400-80)
  max. active 495 mW (HYB 514400-10)
  max. 5.5 mW standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "early write" operation
- Read, write, Read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh, fast page mode
- All inputs and outputs TTL-compatible
- 1024 refresh cycles/16 ms
- Plastic Package: P-SOJ-26/20 350 mil (Plastic small outline J-lead)

The HYB 514400 is the new generation dynamic RAM organized as 1 048 576 words by 4-bits. The HYB 514400 utilizes a submicron triple poly, single metal CMOS technology with a depletion type trench capacitor and a fully overlapping bitline contact (FOBIC) as well as advanced CMOS circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514400 to be packaged in a 26/20-pin SOJ 350 mil plastic package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.

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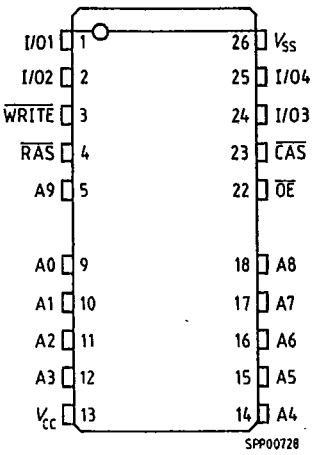
Ordering Information

Type	Ordering code	Package	Description
HYB 514400J-80	Q67100-Q421	P-SOJ-26/20 350 mil	DRAM (access time 80 ns)
HYB 514400J-10	Q67100-Q422	P-SOJ-26/20 350 mil	DRAM (access time 100 ns)

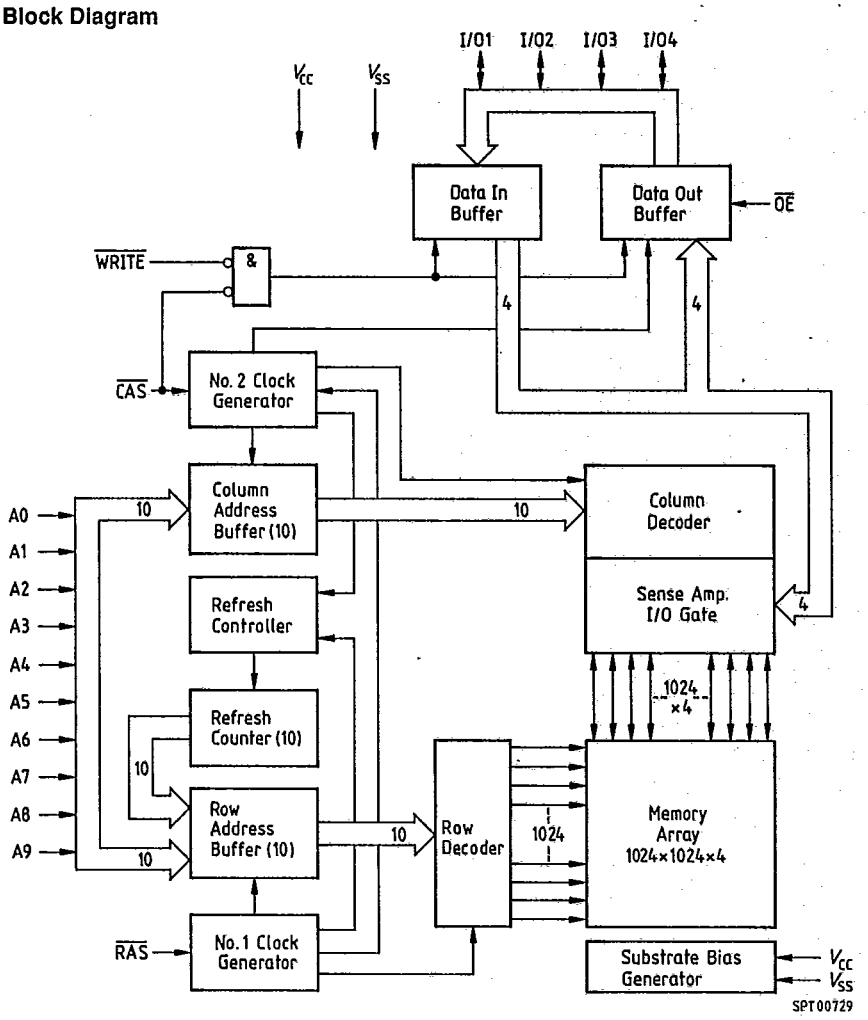
Pin Configuration



Pin Names

A0-A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O4	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)

Block Diagram



Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to +150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 0.6 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 5 V ± 10 %

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IH}	Input high voltage	2.4	6.5	V	–
V_{IL}	Input low voltage	– 1.0	0.8	V	–
V_{OH}	Output high voltage (I_{OUT} = – 5 mA)	2.4	–	V	–
V_{OL}	Output low voltage (I_{OUT} = 4.2 mA)	–	0.4	V	–
$I_{I(L)}$	Input leakage current (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	– 10	10	µA	–
$I_{O(L)}$	Output leakage current, any input (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC}	– 10	10	µA	–
I_{CC1}	Average V_{CC} supply current: HYB 514400-80 HYB 514400-10 ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = $t_{RC\ (min.)}$)	– –	95 85	mA mA	1) 2) 1) 2)
I_{CC2}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	–	2	mA	–
I_{CC3}	Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles: HYB 514400-80 HYB 514400-10 ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = $t_{RC\ (min.)}$)	– –	95 85	mA mA	1) 1)
I_{CC4}	Average V_{CC} supply current, during fast page mode: HYB 514400-80 HYB 514400-10 ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ address cycling: t_{PC} = $t_{PC\ (min.)}$)	– –	70 60	mA mA	1) 2) 1) 2)
I_{CC5}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	–	1	mA	–
I_{CC6}	Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode HYB 514400-80 HYB 514400-10 ($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = $t_{RC\ (min.)}$)	– –	95 85	mA mA	1) 1)

Notes see page 121.

AC Characteristics[3) 4)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Symbol	Parameter		Limit values				Unit
			HYB 514400-80		HYB 514400-10		
			min.	max.	min.	max.	
t_{RC}	Random read or write cycle time		160	–	190	–	ns
t_{RWC}	Read-write cycle time		205	–	245	–	ns
t_{PC}	Fast page mode cycle time		50	–	60	–	ns
t_{PRWC}	Fast page mode read/write cycle time		100	–	115	–	ns
t_{RAC}	Access time from $\overline{RAS}$	5) 10)	–	80	–	100	ns
t_{CAC}	Access time from $\overline{CAS}$	5) 10)	–	20	–	25	ns
t_{AA}	Access time from column address	5) 11)	–	40	–	50	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	5)	–	45	–	55	ns
t_{CLZ}	$\overline{CAS}$ to output in low-Z	5)	0	–	0	–	ns
t_{OFF}	Output buffer turn-of delay	6)	0	20	0	20	ns
t_T	Transition time (rise and fall)	4)	3	50	3	50	ns
t_{RP}	$\overline{RAS}$ precharge time		70	–	80	–	ns
t_{RAS}	$\overline{RAS}$ pulse width		80	10.000	100	10.000	ns
t_{RASP}	$\overline{RAS}$ pulse width (fast page mode)		80	200.000	100	200.000	ns
t_{RSH}	$\overline{RAS}$ hold time		20	–	25	–	ns
t_{CSH}	$\overline{CAS}$ hold time		80	–	100	–	ns
t_{CAS}	$\overline{CAS}$ pulse width		20	10.000	25	10.000	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	10)	20	60	25	75	ns
t_{RAD}	$\overline{RAS}$ to column address delay time	11)	15	40	20	50	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time		5	–	10	–	ns
t_{CP}	$\overline{CAS}$ precharge time (Fast page mode)		10	–	10	–	ns
t_{ASR}	Row address setup time		0	–	0	–	ns
t_{RAH}	Row address hold time		10	–	15	–	ns
t_{ASC}	Column address setup time		0	–	0	–	ns
t_{CAH}	Column address hold time		15	–	20	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$		60	–	75	–	ns
t_{RAL}	Column address to $\overline{RAS}$ lead time		40	–	50	–	ns
t_{RCS}	Read command setup time		0	–	0	–	ns
t_{RCH}	Read command hold time	7)	0	–	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$	7)	0	–	0	–	ns
t_{WCH}	Write command hold time		15	–	20	–	ns
t_{WCR}	Write command hold time referenced to $\overline{RAS}$		60	–	75	–	ns

Notes see page 121.

AC Characteristics [3] [4] (cont'd)

Symbol	Parameter	Limit values				Unit
		HYB 514400-80		HYB 514400-10		
		min.	max.	min.	max.	
t_{WP}	Write command pulse width	15	–	20	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	15	–	25	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time	15	–	25	–	ns
t_{DS}	Data setup time [8]	0	–	0	–	ns
t_{DH}	Data hold time [8]	15	–	20	–	ns
t_{DHR}	Data hold time referenced to $\overline{RAS}$	60	–	75	–	ns
t_{REF}	Refresh period	–	16	–	16	ms
t_{WCS}	Write command set-up time [9]	0	–	0	–	ns
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay time [9]	45	–	50	–	ns
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay time [9]	105	–	125	–	ns
t_{AWD}	Column address to $\overline{WRITE}$ delay time [9]	65	–	75	–	ns
t_{CSR}	$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	10	–	10	–	ns
t_{CHR}	$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	30	–	30	–	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	0	–	0	–	ns
t_{CPT}	$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	40	–	50	–	ns
t_{CPN}	$\overline{CAS}$ precharge time	10	–	15	–	ns
t_{WTS}	Write command setup time (in test mode entry cycle)	10	–	10	–	ns
t_{WTH}	Write command hold time (in test mode entry cycle)	10	–	10	–	ns
t_{WRP}	Write to $\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ cycle)	10	–	10	–	ns
t_{WRH}	Write hold time referenced to $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$ cycle)	10	–	10	–	ns
t_{OEH}	$\overline{OE}$ command hold time	20	–	25	–	ns
t_{OEA}	$\overline{OE}$ access time	–	20	–	25	ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	20	–	25	–	ns
t_{OEZ}	Output buffer turn-off delay from $\overline{OE}$	0	20	0	20	ns
t_{DZC}	Data to $\overline{CAS}$ low delay [13]	0	–	0	–	ns
t_{DZO}	Data to $\overline{OE}$ low delay [13]	0	–	0	–	ns
t_{CDD}	$\overline{CAS}$ high to data delay [14]	20	–	20	–	ns
t_{ODD}	$\overline{OE}$ high to data delay [14]	20	–	20	–	ns
t_{OECH}	$\overline{CAS}$ hold time after $\overline{OE}$ low	20	–	25	–	ns

Notes see page 121.

Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

Symbol	Parameter	Limit values		Unit
		min.	max.	
C_{I1}	Input capacitance (A0 to A9, DI)	–	6	pF
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	–	7	pF
C_O	Output capacitance (DO)	–	7	pF

Notes for pages 118 to 120

1) I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
2) I_{CC1}, I_{CC4} depend on output loading. Specified values are measured with output open.
3) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
5) Measured with a load equivalent to 2 TTL loads and 100 pF.
6) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ defines the time at which the output achieves the open-circuit condition and are not referenced to output voltage levels.
7) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
8) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WRITE}$ leading edge in read-write cycles.
9) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS\ (min.)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$ and $t_{AWD} \geq t_{AWD\ (min.)}$ the cycle is a read-write cycle and DO will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of DO (at access time) is indeterminate.
10) Operation within the $t_{RCD\ (max.)}$ limit insures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.
11) Operation within the $t_{RAD\ (max.)}$ limit insures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.
12) AC measurements assume t_T = 5 ns.
13) Either t_{DZC} or t_{DZO} must be satisfied.
14) Either t_{CDD} or t_{ODD} must be satisfied.

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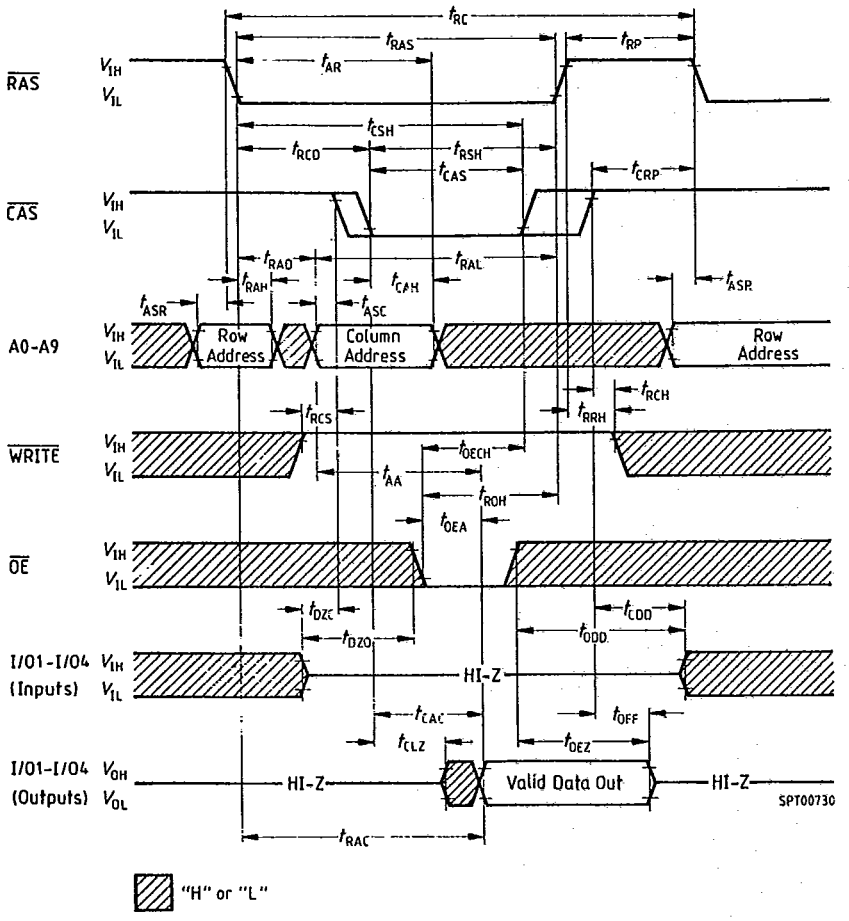
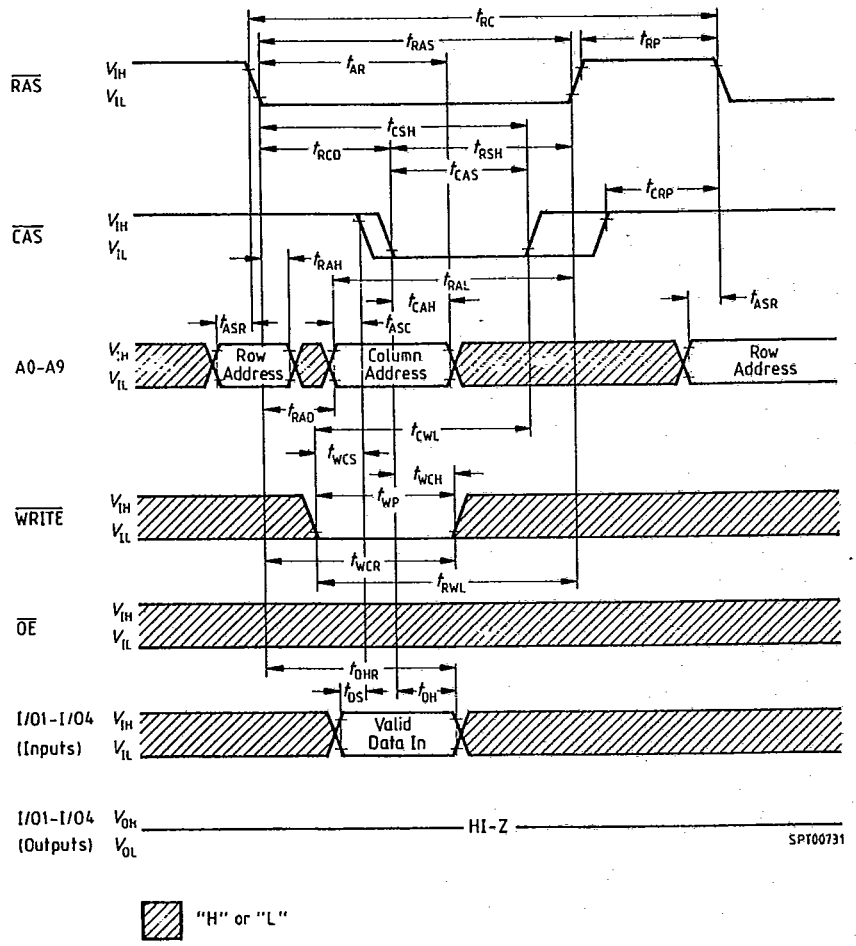
Waveforms

Read Cycle



Write Cycle (Early Write)



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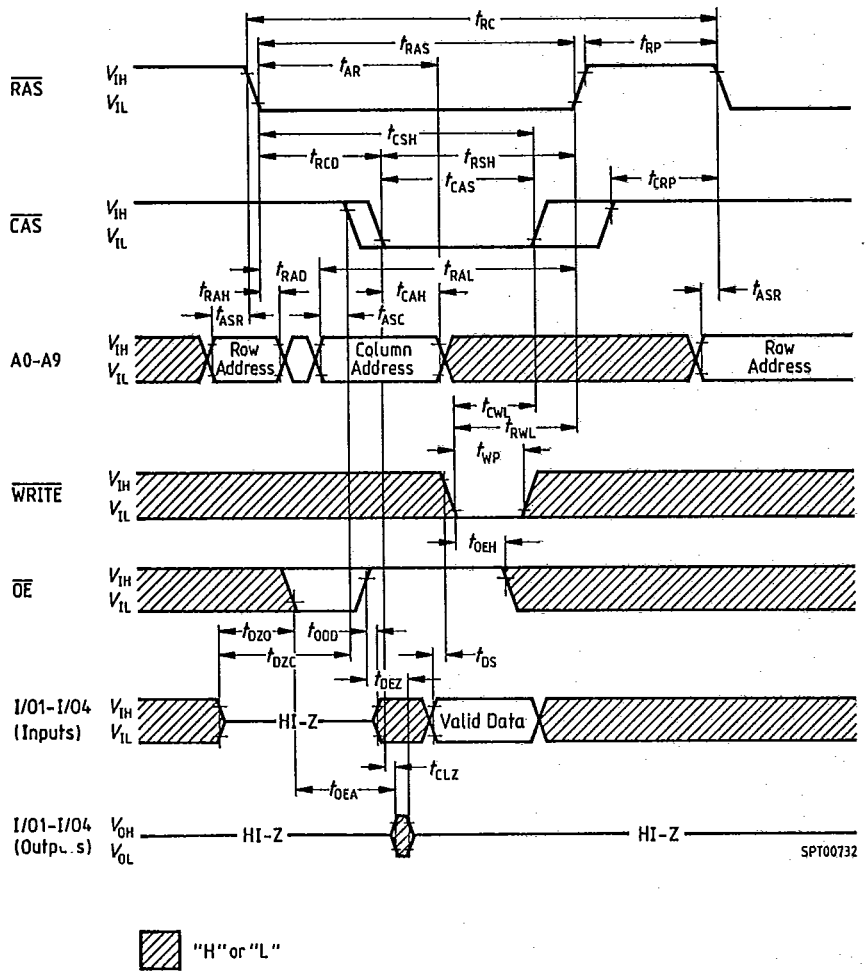
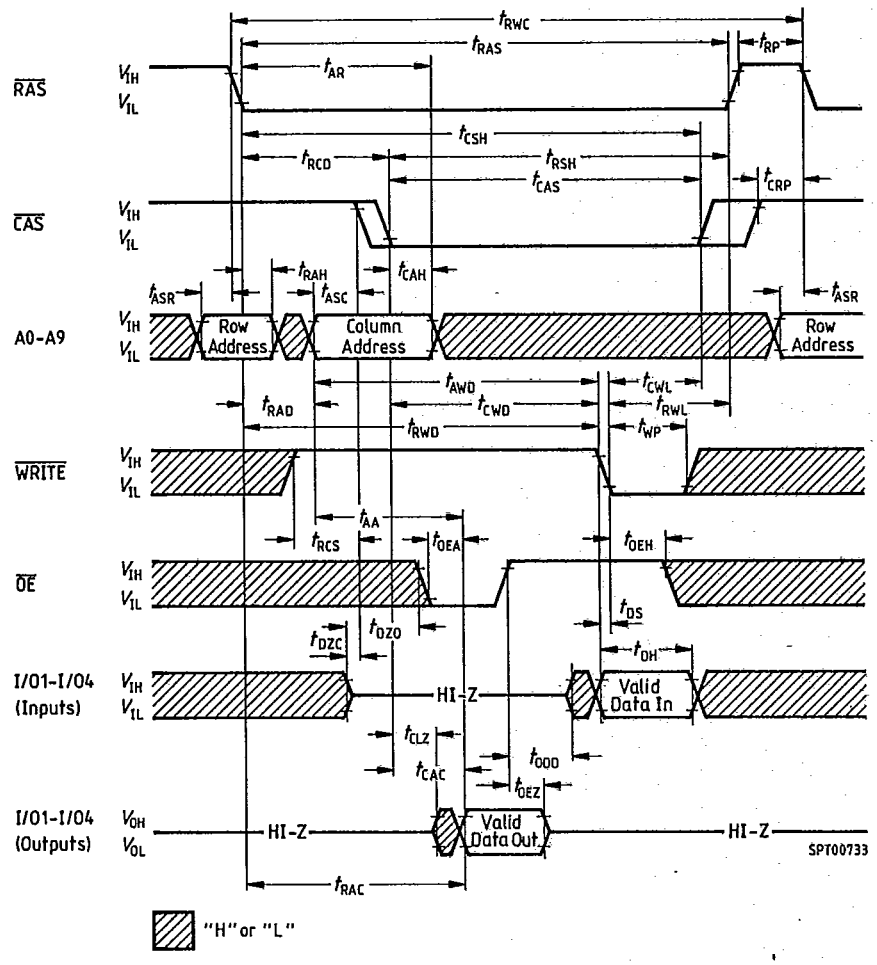
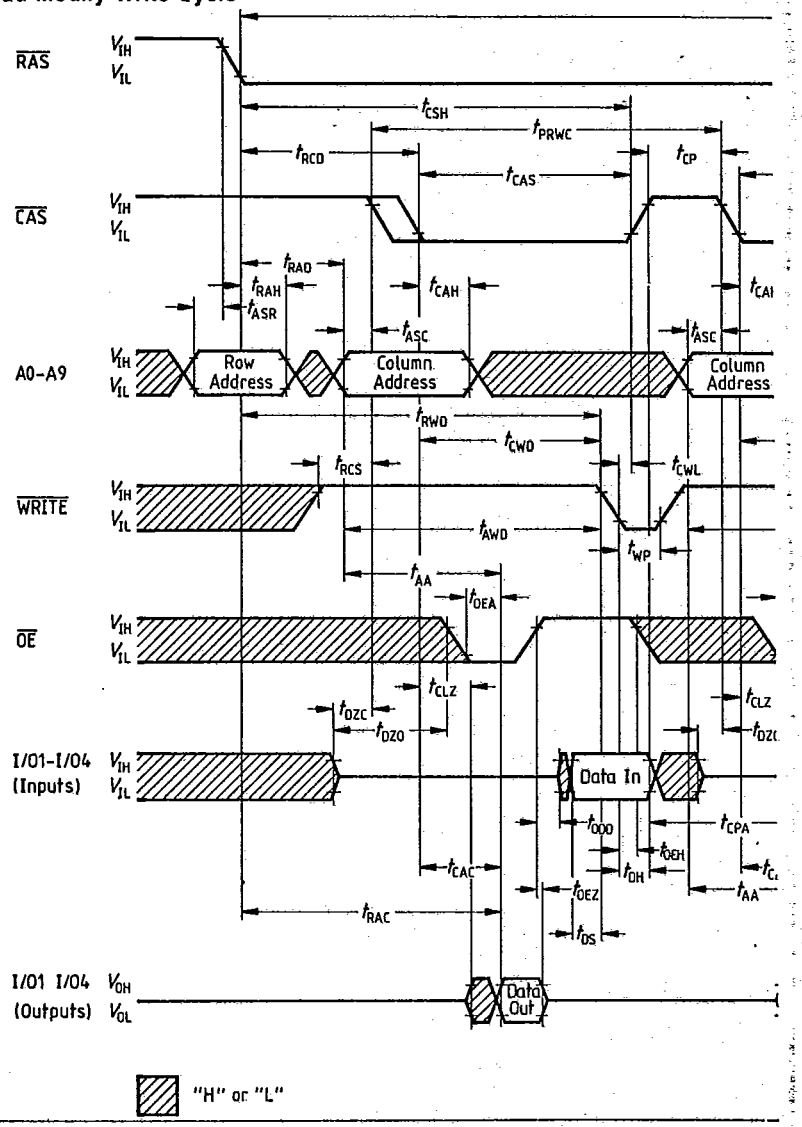
Write Cycle ($\overline{OE}$ Controlled Write)



Read-Write (Read-Modify-Write) Cycle



Fast Page Mode Read-Modify-Write Cycle



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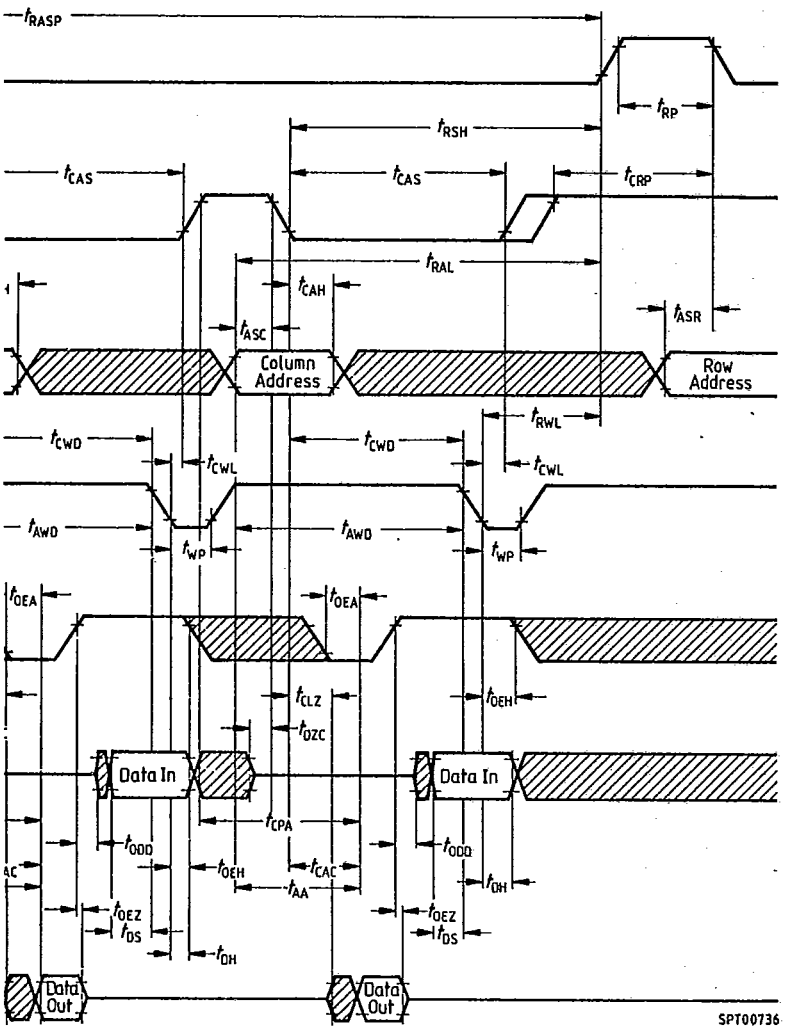
t_{RASP}
t_{RP}
t_{RSH}
t_{CAS}
t_{CAS}
t_{CRP}
t_{RAL}
t_{CAH}
t_{ASR}
t_{ASC}
Column Address
Row Address
t_{RWL}
t_{CWD}
t_{CWD}
t_{CWL}
t_{CWL}
t_{AWD}
t_{AWD}
t_{WP}
t_{WP}
t_{OEA}
t_{OEA}
t_{CLZ}
t_{OEH}
t_{OZC}
Data In
Data In
t_{CPA}
t_{ODD}
t_{ODD}
t_{OEH}
t_{CAC}
t_{AA}
t_{OH}
t_{OEZ}
t_{DS}
t_{OEZ}
t_{DS}
t_{OH}
Data Out
Data Out
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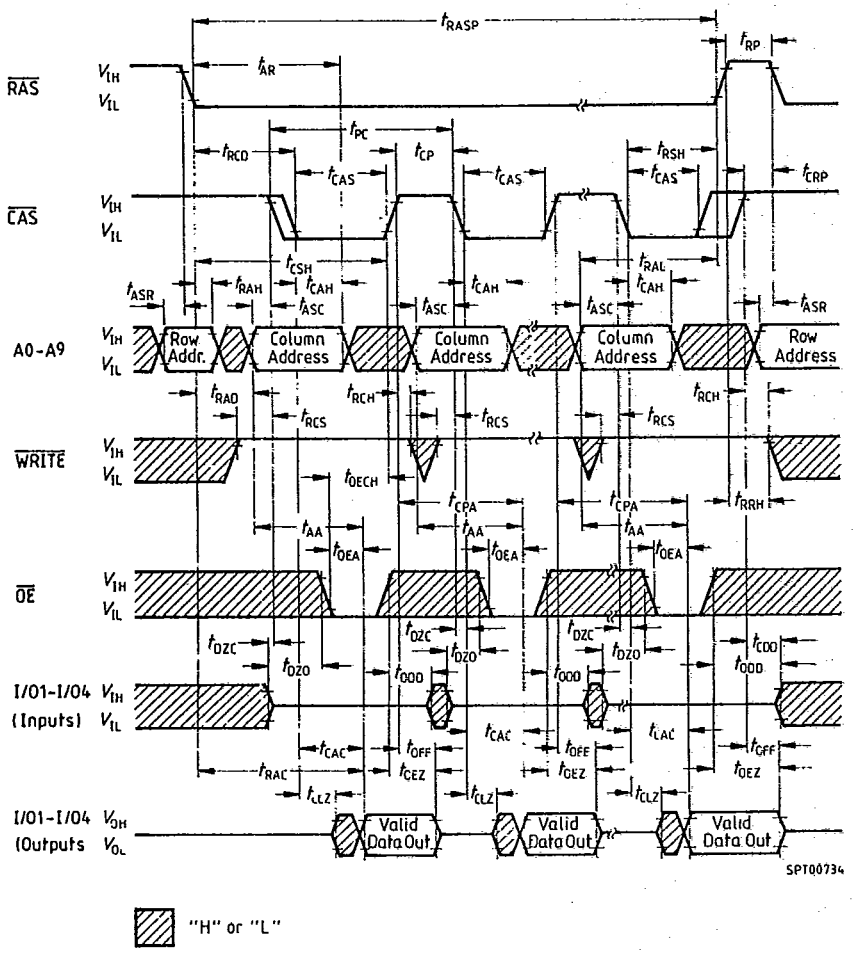
Fast Page Mode Read Cycle



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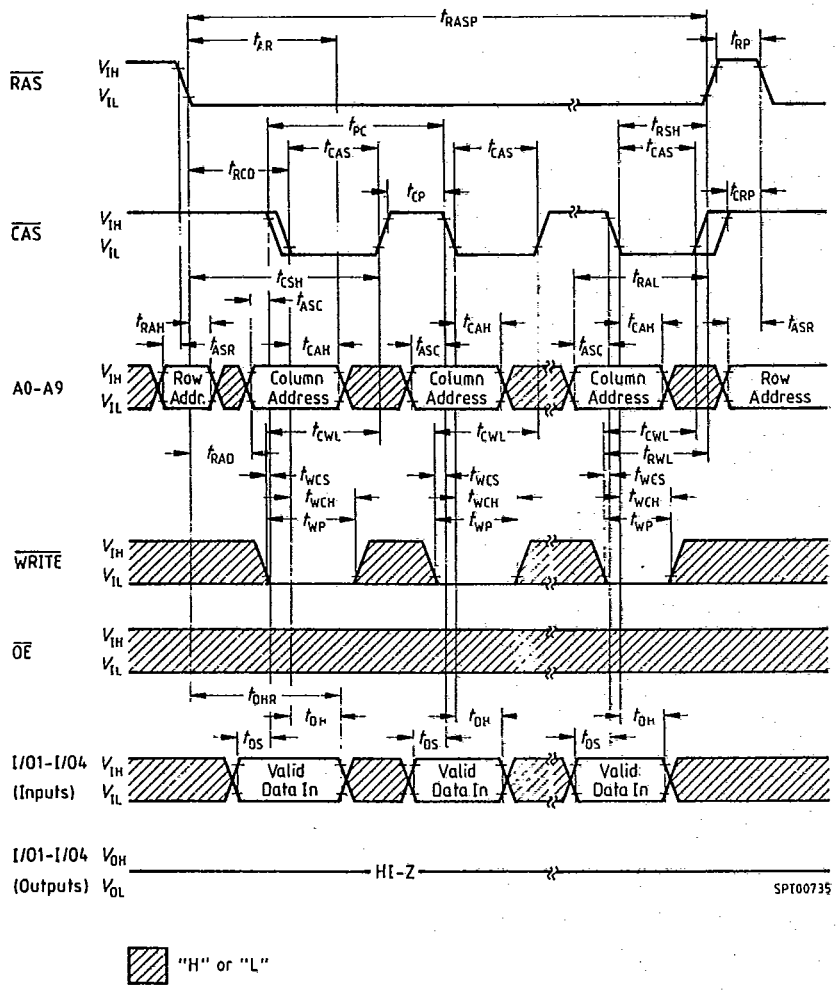
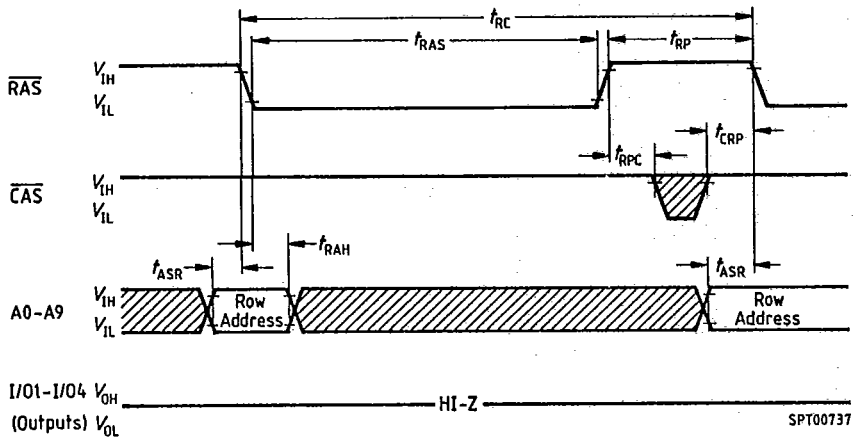
Fast Page Mode Early Write Cycle



RAS-Only Refresh Cycle



Note: $\overline{WRITE}$, $\overline{OE}$, I/O1-I/O4(Inputs) = Don't Care

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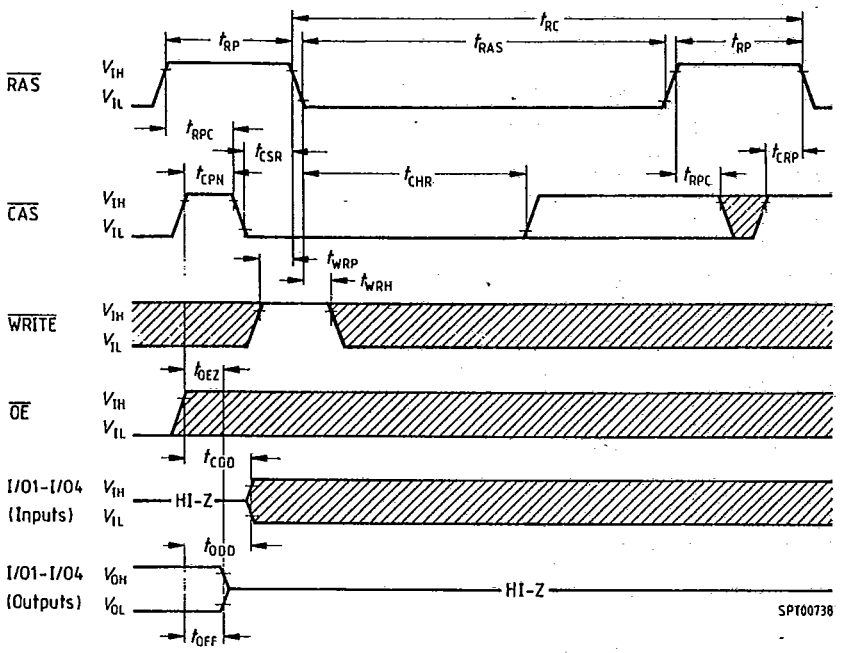
CAS-Before-RAS Refresh Cycle



"H" or "L"

Note: A0 - A9 = Don't Care

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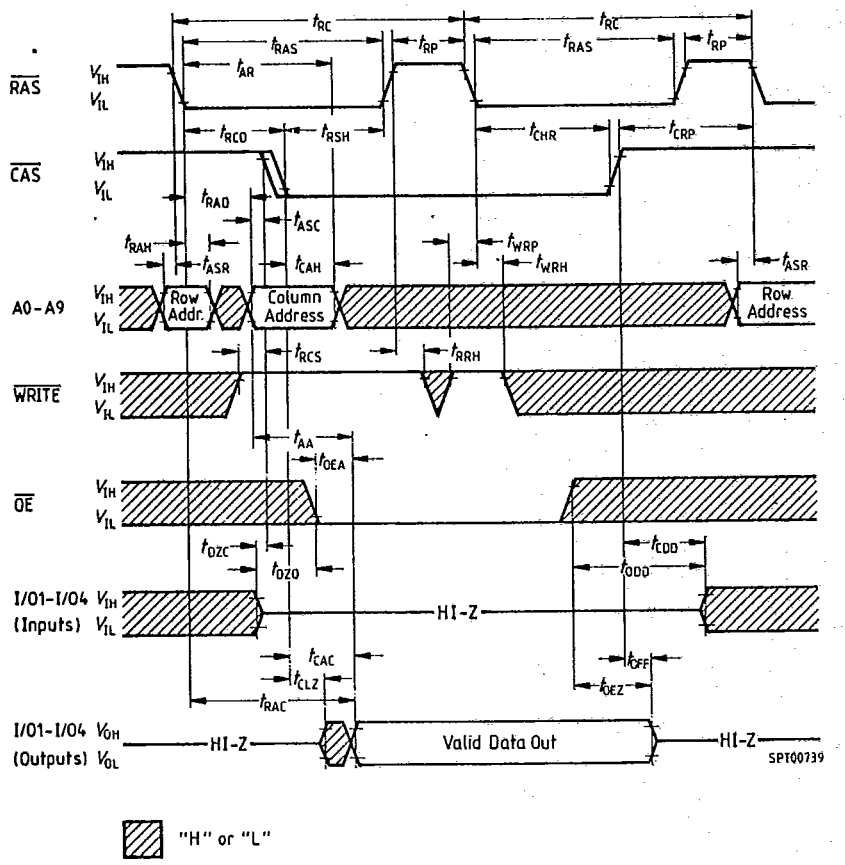
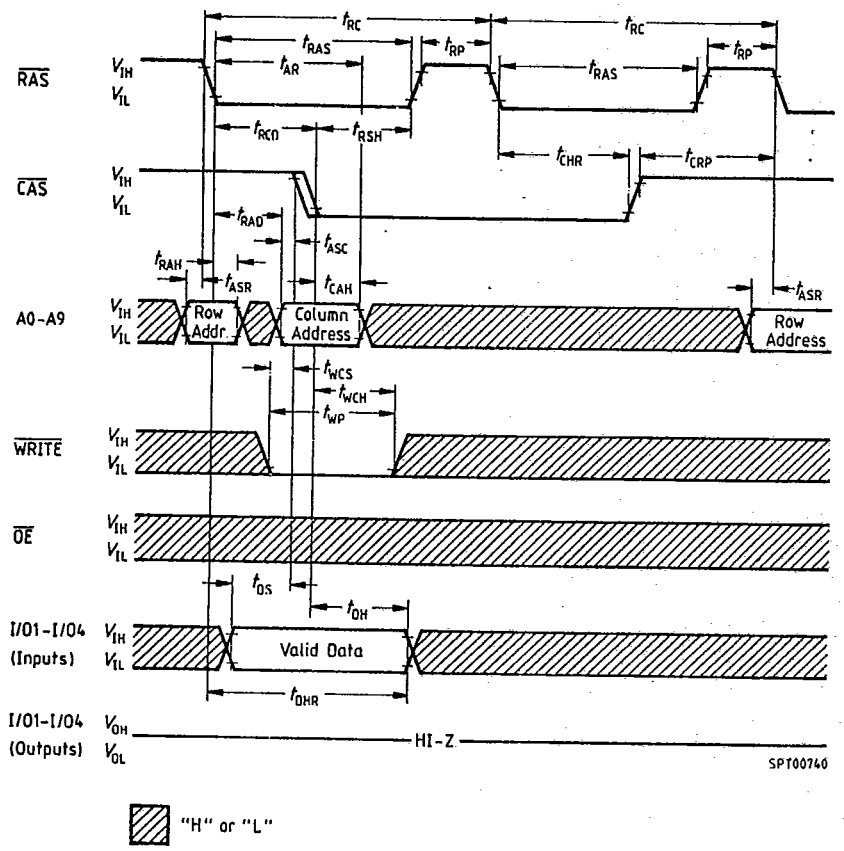
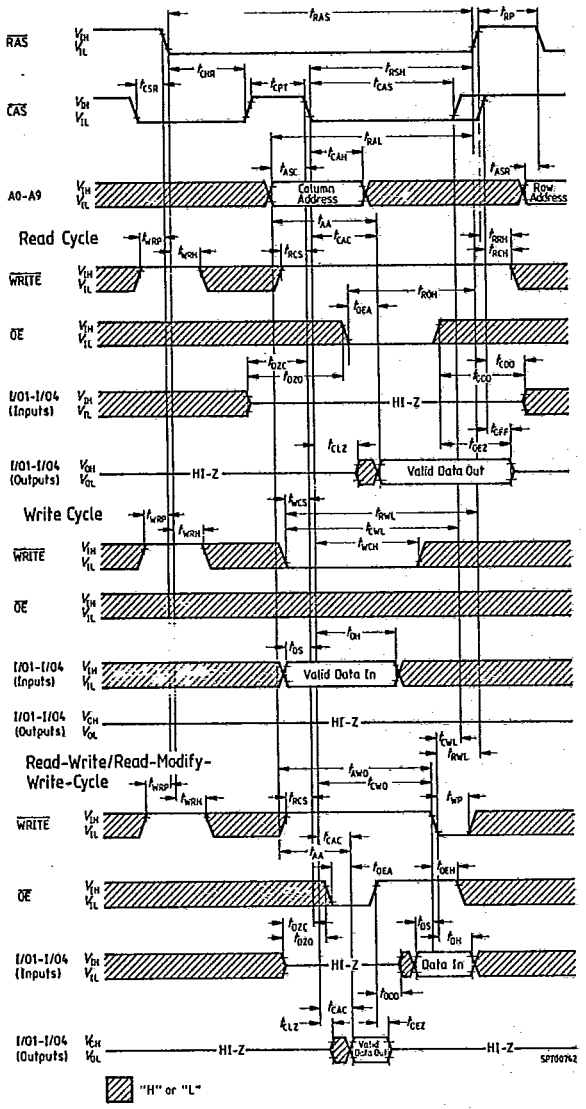
Hidden Refresh Cycle (Read)



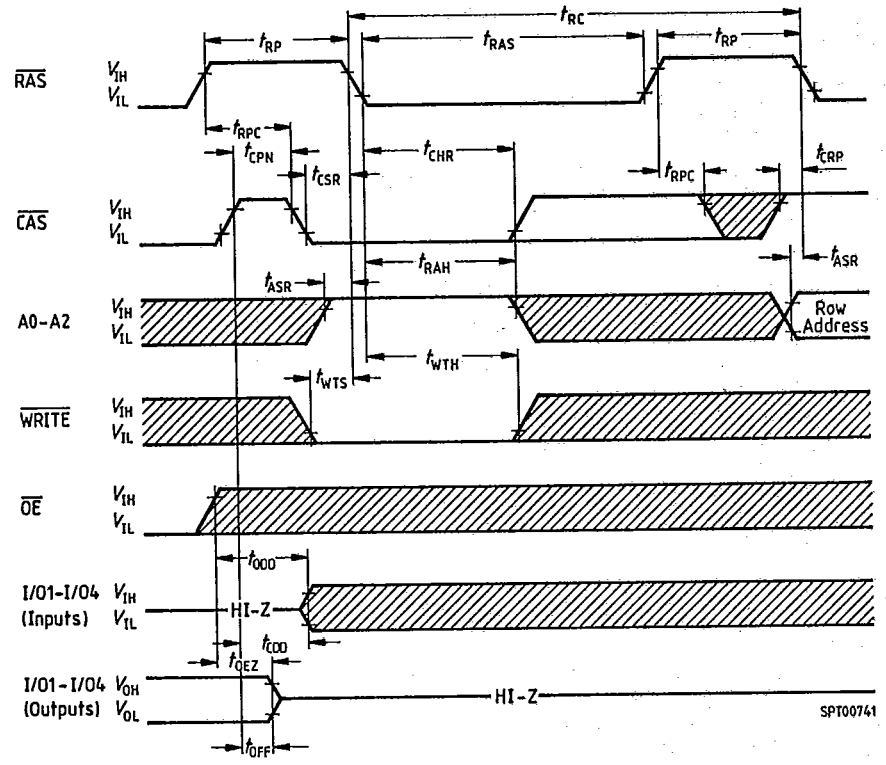
Hidden Refresh Cycle (Early Write)



CAS-Before-RAS Refresh Counter Test Cycle



Test Mode Entry

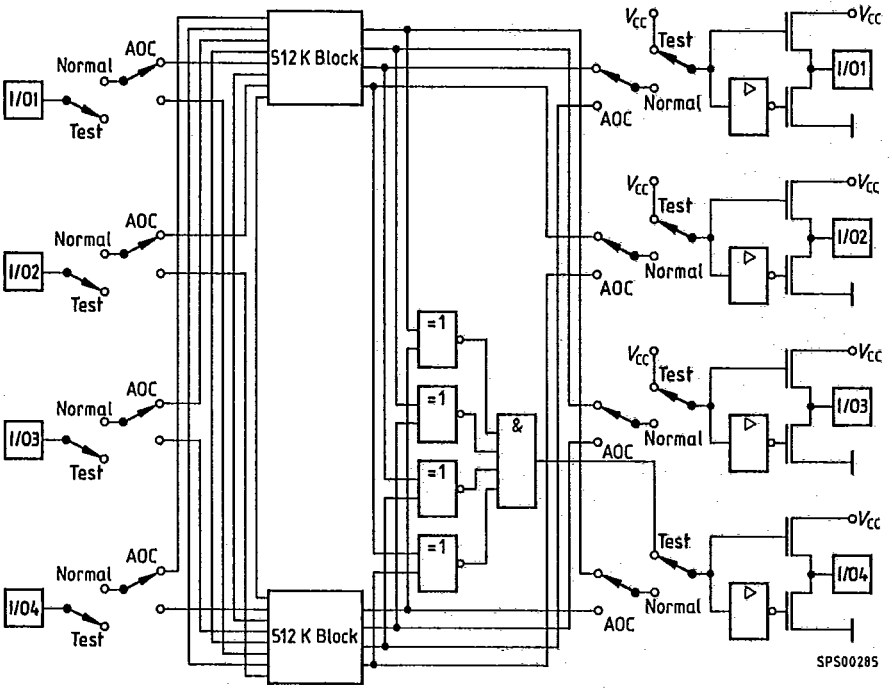


Test Mode

As the HYB 514400 RAM (1M x 4) is organized internally as 512 K x 8-bits, a test mode cycle using 8:1 compression can be used to improve test time. Note theat in the 1M x 4 version the test time is reduced by 1/2 for a N test pattern.

In a test mode "write" the data from the I/O1 pin is written into all eight bits simultaneously (all "1" s or all "0" s). The I/O2-I/O4 inputs are not used for writing in test mode. In test mode "read" the I/O4 output is used for indicating the test mode result. If the internal eight bits are equal, I/O4 would indicate a "1". If they were not equal, I/O4 would indicate a "0". Note that in a test mode "read" I/O1-I/O3 are always driven to "1" s, i. e. all outputs will be "1" s for a test mode "pass" (See test mode block diagram). The "$\overline{\text{WRITE}}$", $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh" cycle puts the device into test mode. To exit from test mode, a "$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh", "$\overline{\text{RAS}}$ only refresh" or "Hidden refresh" can be used.

Block Diagram In Test Mode



The 4M DRAM is divided into eight 512 K blocks. In test mode, information from two of the eight blocks is compared as shown in the diagram above. The 2 of 8 block selection is determined by the row addresses A8R and A9R.