

## DESCRIPTION

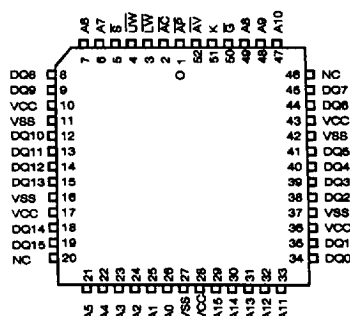
This device integrates high-speed 64Kx16 SRAM core, address registers, data input registers, a 2-bit burst address counter and Non-pipelined output. All synchronous inputs pass through registers controlled by a positive-edge triggered clock(K).

The device is ideally suited for 486/Pentium system by including all necessary timing and control logic on a chip. Any external address latches, counters, or other timing and control logic are not necessary.

## FEATURES

- Single 3.3V±5% power supply.
- 20ns/25ns/30ns access times from clock
- Support up to 50MHz System Operation
- Optimized for use with Interleaved 486/Pentium secondary cache applications (Interleaved burst sequence and Linear burst sequence)
- Byte writable using separate upper/lower byte write input controls
- On-chip burst address counter
- On-chip clocked input and output registers
- 3-state buffered output with asynchronous output enable control
- Standard 52-lead PLCC package with JEDEC pinout

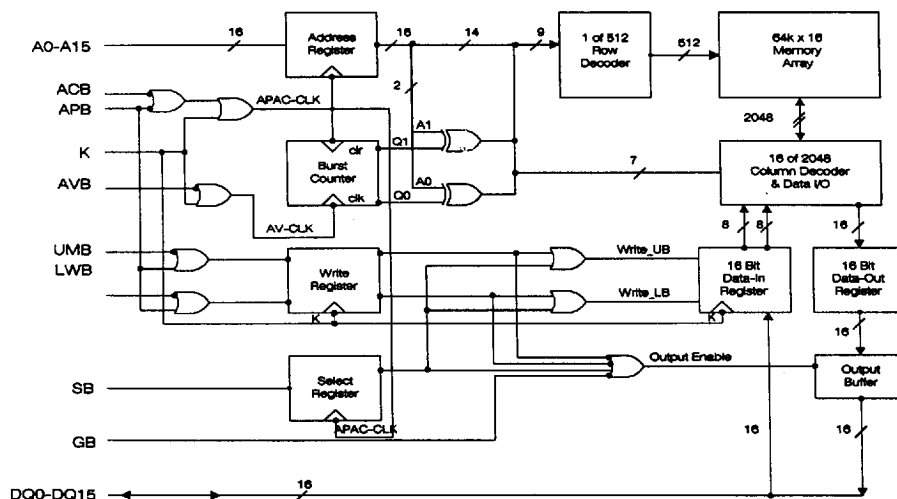
## PIN CONNECTION



## PART NUMBER EXAMPLES

| Part NO.   | Burst Sequence |
|------------|----------------|
| HY67V16110 | Interleaved    |
| HY67V16111 | Linear         |

## FUNCTION BLOCK DIAGRAM



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305

**PIN DESCRIPTIONS**

| SYMBOL      | PIN NUMBER                                                   | TYPE             | DESCRIPTION                                                                                                                                                                                                                                                                                                                                               |
|-------------|--------------------------------------------------------------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| K           | 51                                                           | Input            | Clock.<br>This signal is used to synchronize the device with the system timing. It registers the Addresses, Data inputs, Byte Write Enables and Chip Enable. It may clear or increment the burst counter depending on the state of APB, ACB and AVB.                                                                                                      |
| A0-An       | 6, 7, 21, 22, 23, 24, 25, 26, 29, 30, 31, 32, 33, 47, 48, 49 | Input            | Synchronous Address.<br>The addresses are registered at rising edge of the clock.                                                                                                                                                                                                                                                                         |
| SB          | 5                                                            | Input            | Chip Select.<br>A synchronous control input used to enable(LOW state) and disable(HIGH state) the device. This input is sampled and registered only when a new base address cycle is initiated.                                                                                                                                                           |
| UWB/<br>LWB | 3, 4                                                         | Input            | Upper and Lower Byte Write Enable.<br>Synchronous control input registered by rising edge of the clock. A LOW state allows data to be written into the device, and a HIGH state initiates a read cycle. UWB controls upper byte(DQ8-15) and LWB controls lower byte(DQ0-7).                                                                               |
| APB         | 1                                                            | Input            | Address Status from Processor.<br>A synchronous control input registered by rising edge of the clock. A LOW state interrupts the burst sequence and loads in a new address. The device will read out the data at new address. This input over-rides ACB and UWB/LWB.                                                                                      |
| ACB         | 2                                                            | Input            | Address Status from Cache Controller.<br>A synchronous control input registered by rising edge of the clock. When this input is at LOW state and APB is HIGH state, burst sequence is interrupted and new addresses are loaded into the device. The device will perform a read or write cycle with new addresses.                                         |
| AVB         | 52                                                           | Input            | Burst Address Advance.<br>A synchronous control input registered by rising edge of the clock. When this input is at LOW state, the burst counter increments at rising clock edge. A HIGH state will insert wait states into the burst sequence. The burst addresses will wrap around to the initial state after burst counter completed a burst sequence. |
| GB          | 50                                                           | Input            | Output Enable.<br>An asynchronous control input. A LOW state will enable the DQs and a HIGH state will tri-state the DQs.                                                                                                                                                                                                                                 |
| DQ0-n       | 8, 9, 12, 13, 14, 15, 18, 19, 34, 35, 38, 39, 40, 41, 44, 45 | Input/<br>Output | Data Input/Outputs.<br>A bi-directional common I/O data pins. GB controls the pins when the device is outputting the data(read cycle). At write cycle, input data are registered at rising edge of the clock.                                                                                                                                             |
| VCC         | 28                                                           | Supply           | Positive Power Supply: +3.3V±5%                                                                                                                                                                                                                                                                                                                           |
| VSS         | 27                                                           | Supply           | Negative Power Supply and Ground Return.                                                                                                                                                                                                                                                                                                                  |
| VCCQ        | 10, 17, 36, 43                                               | Supply           | Isolated Output Buffer Supply: +3.3V±5%                                                                                                                                                                                                                                                                                                                   |
| VSSQ        | 11, 16, 37, 42                                               | Supply           | Isolated Output Buffer Ground: GND                                                                                                                                                                                                                                                                                                                        |
| NC          | 20, 46                                                       | Supply           | No Connection                                                                                                                                                                                                                                                                                                                                             |

TRUTH TABLE

| OPERATION                                                                | ADD. | SB | LWB | UWB | APB | ACB | AVB | K   | GB | DQ   |
|--------------------------------------------------------------------------|------|----|-----|-----|-----|-----|-----|-----|----|------|
| Deselected, Outputs High Z                                               | X    | H  | X   | X   | X   | L   | X   | L-H | X  | Hi-Z |
| Output Disabled, Outputs High Z                                          | X    | X  | X   | X   | X   | X   | X   | X   | H  | Hi-Z |
| Register New Base Address, Read from Base Address During Next Cycle      | NBA  | L  | X   | X   | L   | X   | X   | L-H | L  | VQ   |
| Register New Base Address, Read from Base Address During Next Cycle      | NBA  | L  | H   | H   | H   | L   | X   | L-H | L  | VQ   |
| Increment Burst Address, Read from Incremented Address During Next Cycle | X    | X  | H   | H   | H   | H   | L   | L-H | L  | VQ   |
| Read, Non-Incremented Burst Address : Wait-State                         | X    | X  | H   | H   | H   | H   | H   | L-H | L  | VQ   |
| Register New Base Address, Write Both Bytes at Base Address              | NBA  | L  | L   | L   | H   | L   | X   | L-H | X  | VD   |
| Register New Base Address, Write Only the Lower Byte at Base Address     | NBA  | L  | L   | H   | H   | L   | X   | L-H | X  | VD   |
| Register New Base Address, Write Only the Upper Byte at Base Address     | NBA  | L  | H   | L   | H   | L   | X   | L-H | X  | VD   |
| Increment Burst Address, Write Both Bytes at Incremented Address         | X    | X  | L   | L   | H   | H   | L   | L-H | X  | VD   |
| Increment Burst Address, Write Only Lower Byte at Incremented Address    | X    | X  | L   | H   | H   | H   | L   | L-H | X  | VD   |
| Increment Burst Address, Write Only Upper Byte at Incremented Address    | X    | X  | H   | L   | H   | H   | L   | L-H | X  | VD   |
| Write Both Bytes, Non-Incremented Burst Address : Wait-State             | X    | X  | L   | L   | H   | H   | H   | L-H | X  | VD   |
| Lower Byte Write, Non-Incremented Burst Address : Wait-State             | X    | X  | L   | H   | H   | H   | H   | L-H | X  | VD   |
| Upper Byte Write, Non-Incremented Burst Address : Wait-State             | X    | X  | H   | L   | H   | H   | H   | L-H | X  | VD   |

Note :

All inputs except GB must meet set-up and hold times on the rising edge(LOW to HIGH) of K. The burst counter is cleared or incremented by the rising edge of K combined with the control inputs APB, ACB and AVB.

Hi-Z = High Impedance  
VQ = Valid Data Output  
VD = Valid Data Input  
NBA = New Base Address

X = Don't Care : Input  
Changing : Output  
L = Low  
H = High

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**INTERLEAVED BURST SEQUENCE TABLE**

Note that in every case the sequence starts with the initial address, then complements the RAM LSB, then complements both, and finally complements the RAM 2nd LSB, It is only when application-specific address weights are assigned that the sequence appears to differ.

| APPLICATION TYPE        | SEQUENCE 0  | SEQUENCE 1  | SEQUENCE 2  | SEQUENCE 3  |
|-------------------------|-------------|-------------|-------------|-------------|
| '486 Application :      |             |             |             |             |
| Initial                 | 00          | 04          | 08          | 0C          |
| First in Burst          | 04          | 00          | 0C          | 08          |
| Second in Burst         | 08          | 0C          | 00          | 04          |
| Third in Burst          | 0C          | 08          | 04          | 00          |
| Pentium Application :   |             |             |             |             |
| Initial                 | 00          | 08          | 10          | 18          |
| First in Burst          | 08          | 00          | 18          | 10          |
| Second in Burst         | 10          | 18          | 00          | 08          |
| Third in Burst          | 18          | 10          | 08          | 00          |
| Arbitrary Application : |             |             |             |             |
| Initial                 | RAM A1 A0   | RAM A1 A0   | RAM A1 A0   | RAM A1 A0   |
| First in Burst          | RAM A1 A0B  | RAM A1 A0B  | RAM A1 A0B  | RAM A1 A0B  |
| Second in Burst         | RAM A1B A0  | RAM A1B A0  | RAM A1B A0  | RAM A1B A0  |
| Third in Burst          | RAM A1B A0B | RAM A1B A0B | RAM A1B A0B | RAM A1B A0B |

**LINEAR BURST SEQUENCE TABLE**

|                 | SEQUENCE 0  | SEQUENCE 1  | SEQUENCE 2  | SEQUENCE 3  |
|-----------------|-------------|-------------|-------------|-------------|
| Initial         | RAM A1B A0B | RAM A1B A0  | RAM A1 A0B  | RAM A1 A0   |
| First in Burst  | RAM A1B A0  | RAM A1 A0B  | RAM A1 A0   | RAM A1B A0B |
| Second in Burst | RAM A1 A0B  | RAM A1 A0   | RAM A1B A0B | RAM A1B A0  |
| Third in Burst  | RAM A1 A0   | RAM A1B A0B | RAM A1B A0  | RAM A1 A0B  |

4675088 0006319 9T4

**ABSOLUTE MAXIMUM RATINGS**

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in the excess of those given in the operation sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

| Parameter                   | SYMBOL | MIN  | MAX     | UNIT |
|-----------------------------|--------|------|---------|------|
| Storage Temperature         | TSTG   | -55  | 125     | °C   |
| Junction Temperature        | Tc     | ...  | 125     | °C   |
| Case Temperature Under Bias | ...    | -10  | 85      | °C   |
| Vcc Potential to Vss        | ...    | -0.5 | 4.6     | V    |
| Input Voltage(dc)           | ...    | -0.3 | Vcc+0.3 | V    |

**RECOMMENDED OPERATING CONDITIONS**

Recommended Operating Conditions are defined as the range of operating conditions over which the device performance meets or exceeds the specified DC characteristics.

| PARAMETER                      | SYMBOL | MIN  | MAX     | UNIT |
|--------------------------------|--------|------|---------|------|
| Operating Supply               | Vcc    | 3.1  | 3.5     | V    |
| Supply Return, Reference Level | Vss    | 0.0  | 0.0     | V    |
| Input Low Voltage Level        | VIL    | -0.3 | 0.8     | V    |
| Input High Voltage Level       | VIH    | 2.0  | Vcc+0.3 | V    |
| Case Temperature               | Tc     | 0    | 70      | °C   |

**ELECTRICAL CHARACTERISTIC**

| PARAMETER                          | SYMBOL           | TEST CONDITIONS                                                                                                                                                                                                                                   | MIN  | TYP | MAX                  | UNIT |
|------------------------------------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-----|----------------------|------|
| Input Voltage : High<br>Low        | V <sub>IH</sub>  | ...                                                                                                                                                                                                                                               | 2.0  | ... | V <sub>CC</sub> +0.3 | V    |
|                                    | V <sub>IL</sub>  | ...                                                                                                                                                                                                                                               | -0.3 | ... | 0.8                  | V    |
| Output Voltage : High<br>Low       | V <sub>OH</sub>  | I <sub>OH</sub> =-4.0mA                                                                                                                                                                                                                           | 2.4  | ... | ...                  | V    |
|                                    | V <sub>OL</sub>  | I <sub>OL</sub> =8.0mA                                                                                                                                                                                                                            | ...  | ... | 0.4                  | V    |
| Input Leakage Current              | I <sub>L1</sub>  | 0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                                                                                                                                                                                                            | -2   | ... | 2                    | μA   |
| Output Leakage Current             | I <sub>LO</sub>  | G <sub>B</sub> ≥ V <sub>CC</sub> -0.2,<br>0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>                                                                                                                                                                 | -2   | ... | 2                    | μA   |
| Power Supply Current:<br>Operating | I <sub>CC</sub>  | Device selected,<br>all inputs ≤ V <sub>IL</sub> or ≥ V <sub>IH</sub> ,<br>V <sub>CC</sub> =MAX,<br>T <sub>cyc</sub> ≥ t <sub>KC</sub> min,<br>outputs open.                                                                                      | 20ns | ... | 170                  | mA   |
|                                    |                  |                                                                                                                                                                                                                                                   | 25ns | ... | 120                  | mA   |
|                                    |                  |                                                                                                                                                                                                                                                   | 30ns | ... | 80                   | mA   |
| CMOS Standby                       | I <sub>sb1</sub> | Device deselected ;<br>S ≥ V <sub>CC</sub> -0.2,<br>A <sub>C</sub> ≤ V <sub>SS</sub> +0.2,<br>all inputs ≤ V <sub>SS</sub> +0.2 or<br>≥ V <sub>CC</sub> -0.2,<br>all inputs static,<br>V <sub>CC</sub> =MAX,<br>f <sub>CLK</sub> =0.              | ...  | ... | 2                    | mA   |
|                                    | I <sub>sb2</sub> | Device deselected ;<br>S ≥ V <sub>CC</sub> -0.2,<br>A <sub>C</sub> ≤ V <sub>SS</sub> +0.2,<br>all inputs ≤ V <sub>SS</sub> +0.2 or<br>≥ V <sub>CC</sub> -0.2,<br>all inputs static,<br>V <sub>CC</sub> =MAX,<br>cycle time ≥ t <sub>KC</sub> min. | ...  | ... | 60                   | mA   |
|                                    | I <sub>sb3</sub> | Device deselected;<br>S ≥ V <sub>IH</sub> ,<br>A <sub>C</sub> ≤ V <sub>IL</sub> ,<br>all inputs ≤ V <sub>IL</sub> or ≥ V <sub>IH</sub> ,<br>all inputs static,<br>V <sub>CC</sub> =MAX,<br>f <sub>CLK</sub> =0.                                   | ...  | ... | 8                    | mA   |
| Short Circuit Output<br>Current    | I <sub>OS</sub>  | -                                                                                                                                                                                                                                                 | ...  | ... | 35                   | mA   |

**TIMING CHARACTERISTICS**

| SYMBOL                                                  | '486/P5 Local Bus Rate                                                                                                                                    | 33MHz |     | 40MHz |     | 50MHz |     | Unit |
|---------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-----|-------|-----|-------|-----|------|
|                                                         | Cache RAM                                                                                                                                                 | 30ns  |     | 25ns  |     | 20ns  |     |      |
|                                                         | Parameter                                                                                                                                                 | Min   | Max | Min   | Max | Min   | Max |      |
| tcyc                                                    | Cycle Time                                                                                                                                                | 30    | ... | 25    | ... | 20    | ... | ns   |
| tkqv                                                    | Access Time from Clock                                                                                                                                    | ...   | 30  | ...   | 25  | ...   | 20  | ns   |
| tis<br>tas<br>tss<br>taps<br>tacs<br>tavs<br>tws<br>tds | Input Setup Time<br>Address<br>Select<br>Address Status - $\mu$ P<br>Address Status - Controller<br>Address Advance<br>Write Enables(LWB, UWB)<br>Data In | 3     | ... | 2.0   | ... | 2.0   | ... | ns   |
| tih<br>tah<br>tsh<br>taph<br>tach<br>tavh<br>twh<br>tdh | Input Hold Time<br>Address<br>Select<br>Address Status - $\mu$ P<br>Address Status - Controller<br>Address Advance<br>Write Enables (LWB, UWB)<br>Data In | 3     | ... | 2.0   | ... | 2.0   | ... | ns   |
| tkh                                                     | Clock High Pulse Width                                                                                                                                    | 12    | ... | 10    | ... | 7     | ... | ns   |
| tkl                                                     | Clock Low Pulse Width                                                                                                                                     | 12    | ... | 10    | ... | 7     | ... | ns   |
| tglqx                                                   | Output Enable to Output<br>Active                                                                                                                         | 3     | ... | 2     | ... | 1     | ... | ns   |
| tglqv                                                   | Output Enable Time                                                                                                                                        | ...   | 7   | ...   | 6   | ...   | 6   | ns   |
| tghqz                                                   | Output Disable Time                                                                                                                                       | ...   | 7   | ...   | 6   | ...   | 6   | ns   |
| tkqx                                                    | Output Change from Clock &<br>Output Enable from Clock                                                                                                    | 4     | ... | 3     | ... | 3     | ... | ns   |
| tkqz                                                    | Output Disable from Clock                                                                                                                                 | ...   | 10  | ...   | 8   | ...   | 7   | ns   |

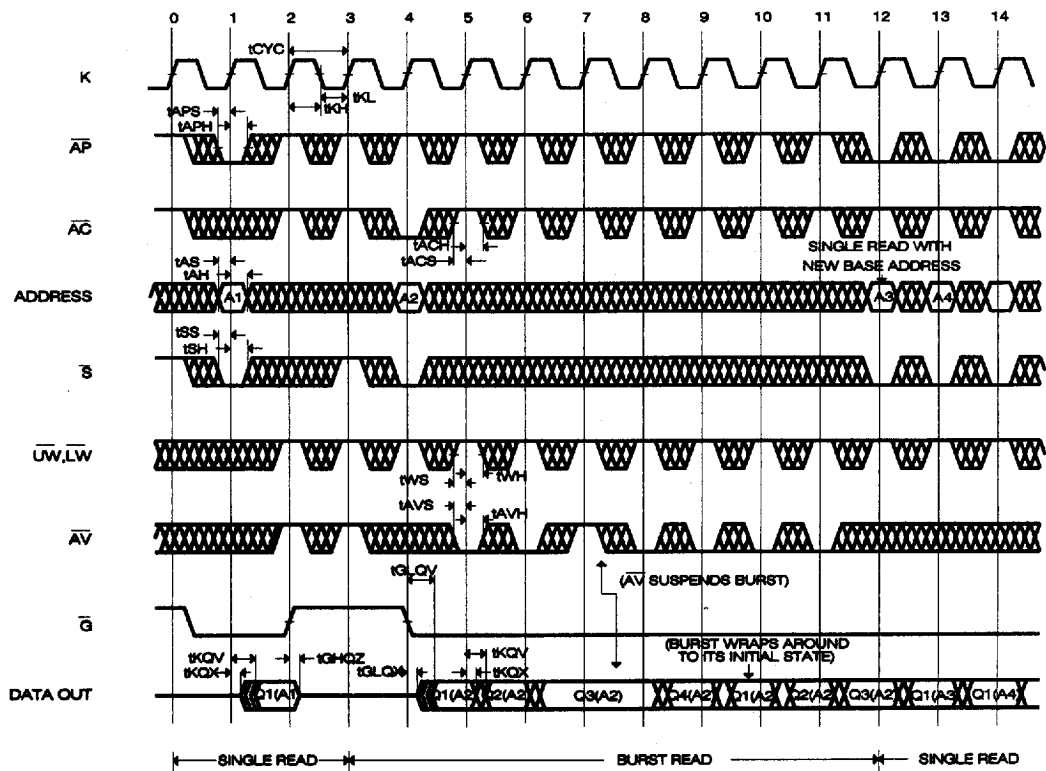
**NOTE :**

1. Switching measurements are from 1.5V levels on the inputs to 1.5V levels on the outputs, except for enable and disable times.
2. Enable and disable time measurements are from 1.5V levels on the inputs to change-of 0.1V in the output levels.
3. See figure AC TEST LOAD A. for output load.
4. Input levels for switching measurements are 0V to 3.0V.
5. Input rise and fall times for switching measurements are  $\leq 2.0\text{ns}$ (20% to 80%).
6. This unit is measured using output loading as specified in figure AC TEST LOAD B.

4675088 0006322 499

**TIMING DIAGRAM**

**READ CYCLE**



4675088 0006323 325



The diagram illustrates the timing for burst read and write operations across 11 clock cycles (0 to 11). The signals and their timing parameters are as follows:

- K**: Clock signal.
- AP**: Address Strobe (Active Low). Timing parameters:  $t_{APHS}$  (setup),  $t_{APH}$  (hold),  $t_{APSS}$  (setup),  $t_{APSH}$  (hold).
- AC**: Address Latch Enable (Active Low). Timing parameters:  $t_{ACYS}$  (setup),  $t_{ACL}$  (hold).
- ADDRESS**: Address bus. Shows burst addresses A1, A2, and A3.
- S**: Strobe (Active Low). Timing parameters:  $t_{SS}$  (setup),  $t_{SH}$  (hold).
- UW, LW**: Write Enable (Active Low). Timing parameters:  $t_{WS}$  (setup),  $t_{WH}$  (hold).
- AV**: Address Valid (Active Low). Timing parameters:  $t_{VS}$  (setup),  $t_{VH}$  (hold).
- G**: Gate (Active Low). Timing parameter:  $t_{GHQZ}$  (hold).
- DATA IN**: Data bus for writes. Shows data D1(A1), D1(A2), D2(A2), D2(A2), D3(A2), D4(A2), D1(A3), D2(A3), D3(A3).
- DATA OUT**: Data bus for reads.

Legend for operations:

- BURST READ**: Indicated by a double asterisk (\*\*) at the start of the burst.
- SINGLE WRITE**: Indicated by a single asterisk (\*) at the start of the burst.
- BURST WRITE**: Indicated by a double asterisk (\*\*) at the start of the burst.
- EXTENDED BURST WRITE**: Indicated by a double asterisk (\*\*) at the start of the burst.

4675088 0006324 261

The timing diagram illustrates the operation of the 68000 microprocessor over 10 clock cycles (0 to 9). The signals shown are:

- K**: Clock signal.
- AP**: Address Strobe (Active Low).
- ADDRESS**: Address bus data.
- S**: Status signal (Active Low).
- UW/LW**: User/Write/Local signal (Active Low).
- AV**: Address Valid (Active Low).
- G**: Gate signal (Active Low).
- DATA IN**: Data bus input.
- DATA OUT**: Data bus output.

Key timing parameters and data bus activity are indicated:

- Address Valid (AV)**: tAS (Address Setup), tAH (Address Hold), tVS (Valid Setup), tVH (Valid Hold).
- Write Strobe (WS)**: tWS (Write Strobe Setup), tWH (Write Strobe Hold).
- Gate (G)**: tDS (Gate Setup), tDH (Gate Hold), tGLOV (Gate Low to Valid).
- Data Valid (Q)**: tQOV (Output Valid), tQOX (Output X), tGHOZ (Gate High to Output Z), tGLOX (Gate Low to Output X), tKQX (Clock to Output X), tKQV (Clock to Output V).

The data bus activity shows:

- Reads**: Indicated by a horizontal line with a right-pointing arrow.
- Single Write**: Indicated by a horizontal line with a single vertical bar.
- Burst Read**: Indicated by a horizontal line with a double vertical bar.

Diagram A shows a circuit with a DATA OUT line connected to a TEST POINT. A 317 ohm resistor is connected in series between the DATA OUT line and the TEST POINT. A 351 ohm resistor is connected in parallel between the DATA OUT line and ground. A 30 pF capacitor is connected in parallel between the TEST POINT and ground.

Diagram B shows a circuit with a DATA OUT line connected to a TEST POINT. A 317 ohm resistor is connected in series between the DATA OUT line and the TEST POINT. A 351 ohm resistor is connected in parallel between the DATA OUT line and ground. A 5 pF capacitor is connected in parallel between the TEST POINT and ground.

795(20.19)  
 785(19.94)  
 756(19.20)  
 750(18.06)

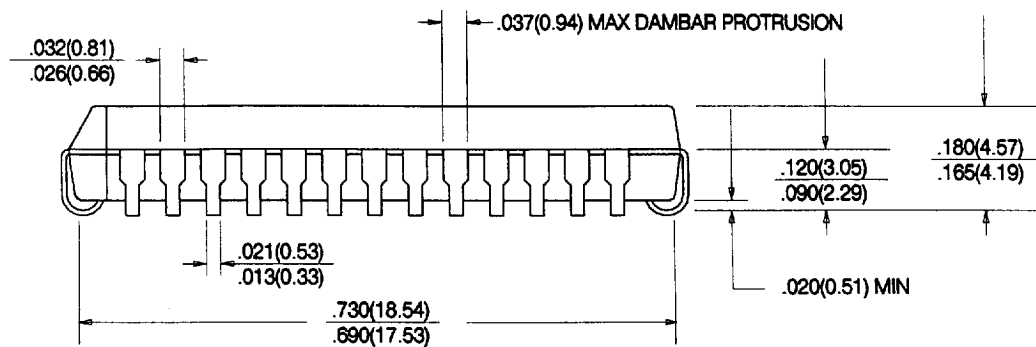
795(20.19)  
 785(19.94)  
 756(19.20)  
 750(18.06)

600(15.24)  
 TYP

0.045(1.14)X45° TYP

0.050(1.27) TYP

PIN #1 INDEX



4675088 0006326 034

**ORDERING INFORMATION**

| <b>PART NO.</b> | <b>SPEED(ns)</b> | <b>FEATURES</b>             | <b>PACKAGE</b> |
|-----------------|------------------|-----------------------------|----------------|
| HY67V16110C     | 20/25/30         | Non-Pipelined (Interleaved) | 52pin PLCC     |
| HY67V16111C     | 20/25/30         | Non-Pipelined (Linear)      | 52pin PLCC     |

■ 4675088 0006327 T70 ■