H0550
H0551
H0552

Intelligent LCD Dot Matrix Controller/Driver

HUGHES AIRCRAFT COMPANY
MICROELECTRONICS CENTER

DESCRIPTION

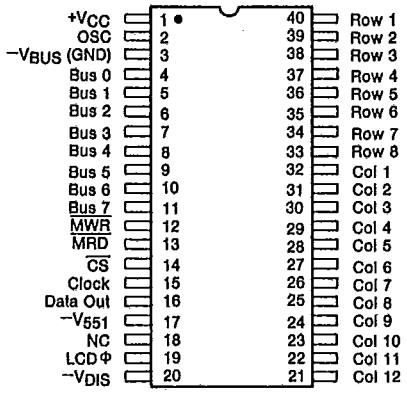
Hughes H0550 and H0551 Chip Set will drive 5 x 7 or 5 x 8 liquid crystal dot matrix of up to 32 characters. Control of the display is handled through an 8 bit bidirectional I/O port. The H0550 controller handles character decode, display manipulation, cursor control, and all display drive functions including refresh and generation of multiple-level AC waveforms. The H0551 is a dumb driver and functions as a column extender when larger display areas are required. An alternative column extender, the H0552, offers 54 additional column drives (rather than the 34 drives of the H0551) and is available in chip form only (H suffix).

The H0550/H0551 is available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request. Commercial (HC prefix) and Industrial (HI prefix) versions are available.

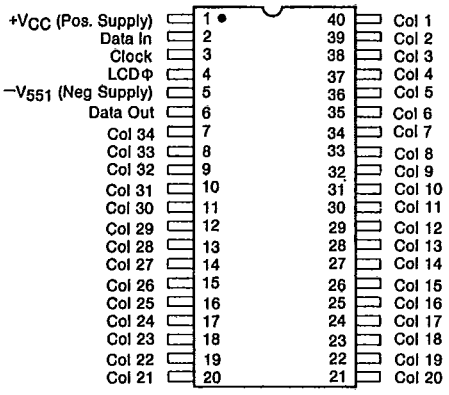
FEATURES

- CMOS circuitry
  - Low power dissipation
  - Wide supply variation
  - High noise immunity
- Microcomputer compatible
- ASCII input format
- Display of 64 different characters
- Control of up to a 32 character display
- Generation of all drive waveforms
- Automatic refresh
- Cursor control
- Display manipulation instructions to accomplish:
  - Shift
  - Rotate
  - Blank
  - Blink
  - Fast load
  - Power down
- Instructions to control output of:
  - Characters
  - Cursor position
  - Display control flags
  - Busy status

H0550
PIN CONFIGURATION



H0551
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, ($+V_{DD}$) ..... −.3V to + 13 Volts
Input Voltage, (V_I) ..... V_{SS} −0.3V to V_{DD} + 0.3V
Operating Temperature, (T_{OP})
Plastic Package ..... − 40 to + 85°C
Ceramic Package ..... − 55 to + 125°C
Storage Temperature, (T_{STO}) .. − 50 to + 125°C

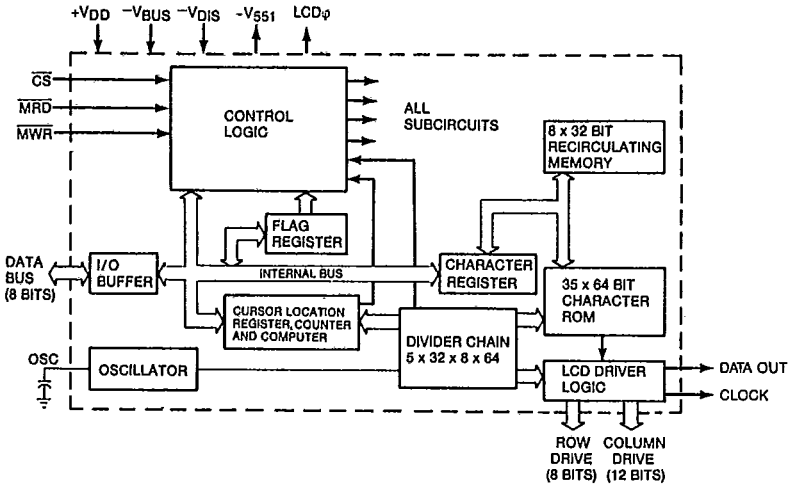
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS at T_A = + 25°C unless otherwise specified ($-V_{BUS}$ pin is considered GND) $V_{DD} = V_{CC} + V_{DIS}$.

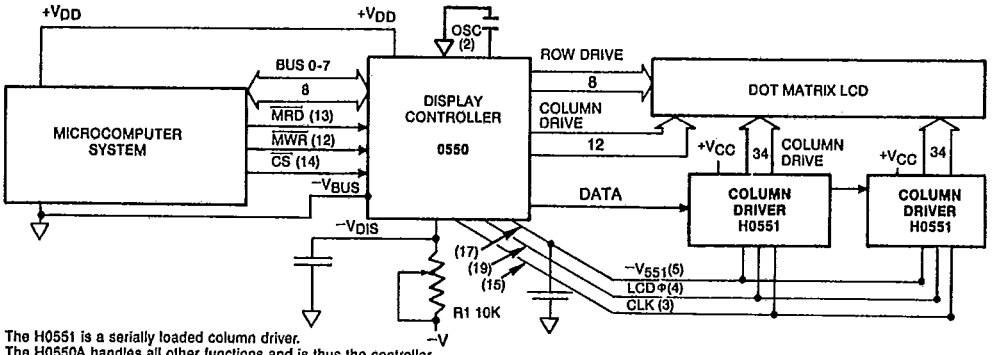
PARAMETER		SYMBOL	CONDITION	0550A[3]	0551	0552	UNITS
Environmental							
Power Supply Voltage		$+V_{DD}$		5 −10	5 −10	5 −10	V
Power Supply Current (0550 and 0551)[5]		I_{DD}	Operating at 5V	750	750	N/A	μA
Quiescent Current (0550)[5]		I_Q	5V, Power Down Mode Inputs at Either Supply[1]	20	N/A	N/A	μA
Inputs – H0550							
High Level	H0550 Inputs	V_{IH}	V_{DD} = 3 to 10V	.8V_{DD}	N/A	N/A	V
Low Level	8 Data Bus	V_{IL}	8 Data Bus	.5V_{DD}	N/A	N/A	V
Low Level	$\overline{CS}$, $\overline{MRD}$, $\overline{MWR}$	V_{IL}	$\overline{CS}$, $\overline{MRD}$, $\overline{MWR}$	V_{CC} −10	N/A	N/A	V
Leakage[5]		I_L	V_{IN} = 0, V_{DD} = 10	5	N/A	N/A	μA
Capacitance[4]		C_{IN}		5	N/A	N/A	pf
Inputs – H0551/H0552							
High Level	H0551/52 Inputs	V_{IH}		N/A	.8V_{DD}	.8V_{DD}	V
Low Level	Data In	V_{IL}		N/A	.5V_{DD}	.5V_{DD}	V
Leakage	LCDΦ	I_L	V_{IN} = 0, V_{DD} = 10	N/A	5	5	μA
Capacitance[4]	Clock	C_{IN}		N/A	5	5	pf
Outputs	Signals to H0551/52						
High Level[4]	LCDΦ	V_{OH}	V_{DD} = 5V	V_{CC} −.05	V_{CC} −.2	N/A	V
Low Level[4]	Data Out	V_{OL}	V_{DD} = 5V	−V_{DIS}+.05	−V_{DIS}+.2	N/A	V
Impedance	Clock	R_{ON}	V_{DD} = 5V, I = 100 μA	3	N/A	N/A	KΩ
Column Drive Impedance		R_{OUT}	V_{DD} = 5V	40	40	40	KΩ
Row Drive Impedance		R_{OUT}	V_{DD} = 5V	10	N/A	N/A	KΩ
Bus Drive High		V_{IH}	V_{DD} = 5V, I = 1.6 mA source	4	N/A	N/A	V
Bus Drive Low		V_{IL}	V_{DD} = 5V, I = 1.6 mA sink	.4	N/A	N/A	V
Timing[2]							
Data Set-up Time		t_{DS}	Data valid to $\overline{MWR}$ fall	20	N/A	N/A	ns
Data Hold Time		t_{DH}	$\overline{MWR}$ pulse to data change	75	N/A	N/A	ns
$\overline{MWR}$ Pulse Width High		t_{PWH}		600	N/A	N/A	ns
$\overline{MWR}$ Pulse Width Low		t_{PWL}		600	N/A	N/A	ns
$\overline{MRD}$ Delay		t_{PD}	$\overline{MRD}$ fall to data valid	600	N/A	N/A	ns
$\overline{MRD}$ Pulse Width High		t_{PWH}		600	N/A	N/A	ns
$\overline{MRD}$ Pulse Width Low		t_{PWL}		600	N/A	N/A	ns

NOTE 1: Oscillator high if driven.
NOTE 2: MWR and MRD negative pulses assumed to be coincident with or narrower than CS negative pulse.
NOTE 3: T_A = −55°C to +125°C.
NOTE 4: Design assured but not tested.
NOTE 5: Parameters guaranteed by other tests at −55°C for device 0550A.

FUNCTIONAL BLOCK DIAGRAM OF H0550

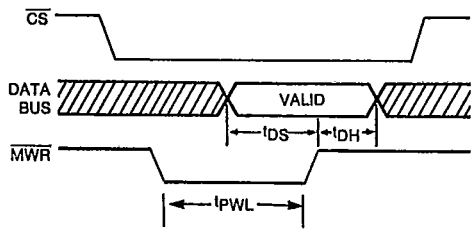


SYSTEM BLOCK DIAGRAM

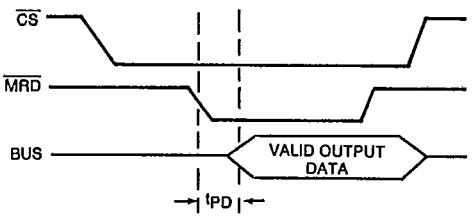


The H0551 is a serially loaded column driver.
The H0550A handles all other functions and is thus the controller.
(See Operating Notes, page 8, Variable Resistor (item 2) and Power Supply (item 4).

INPUT TIMING — 0550



OUTPUT TIMING — 0550



INSTRUCTION SET

Table 1

Description	OP Code 76543210 (see note 1)	HEX Code	BUS (see note 1)	Input or Output	Immed. Exec.	Creates Short Busy	Creates Long Busy	Not During PD	Not During Busy
Load Character	001XXXXX to 010XXXXX	20 to 5F		I	—	—	√	√	√
Load Cursor Location	000XXXXX	00 to 1F		I	√	—	—	—	√ (see note 2)
Set Display Control Flag	011XXXXY	60 to 71		I	√	—	—	—	—
Blink Cursor	0110 0000 - off 0110 0001 - on	60 61	0						
Blink Display	0110 0010 - off 0110 0011 - on	62 63	1						
Auto Inc/Dec	0110 0100 - off 0110 0101 - on	64 65	2						
Up/Down	0110 0110 - off 0110 0111 - on	66 67	3						
Blank Display	0110 1000 - off 0110 1001 - on	68 69	4						
Visible Cursor	0110 1010 - off 0110 1011 - on	6A 6B	5						
Cursor Type	0110 1100 - off 0110 1101 - on	6C 6D	6						
Busy	Output Only	—	7						
Rapid Load	0110 1110 - off 0110 1111 - on	6E 6F	—						
Power Down	0111 0000 - off 0111 0001 - on	70 71	—						
Get Character	10000100	84		O	√	—	—	√ (see note 3)	√ (see note 3)
Get Cursor Location	10000010	82		O	√	—	—	—	—
Get Display Control Flags	10000001	81		O	√	—	—	—	—
Decrement Cursor Increment Cursor	10001000 10001001	88 89		I	√	—	—	—	√ (see note 2)
Shift Right	10001111	8F		I	—	—	√	√	√
Shift Left	10001101	8D		I	—	—	√	√	√
Rotate Right	10001110	8E		I	—	√	—	√	√
Rotate Left	10001100	8C		I	—	√	—	√	√
Clear	10001010	8A		I	—	—	√	√	√
Reset Busy (Abort)	10001011	8B		I	√	—	—	—	—

NOTE: 1. Associated Bus Line for display control flags. Status appears on Bus Line on $\overline{MRD}$ input following a get control flags instruction.
2. Only if busy is due to Load Character.
3. See Instruction Set for special precautions.

X = Variable Data Y = Flag State
Short Busy is 5 to 10 periods of master oscillator, or 125 μsec. at 82 KHz.
Long Busy is up to 160 periods of master oscillator, or 2 msec. at 82 KHz.
Input instructions are accomplished when $\overline{MWR}$ and $\overline{CS}$ are held low.
Output instructions are accomplished when $\overline{MRD}$ and $\overline{CS}$ are held low.
(An output instruction must have been previously written.)

DISPLAY DRIVE LSI REQUIREMENTS

Number of Characters	8	16	20	32
Number of H0550 Required	1	1	1	1
Number of H0551 Required	1	2	3	5
Number of H0552 Required	1	2	2	3

Load Character
This instruction loads a specific character into a previously specified location. The instruction code is 0XXXXXXX where the 7 bit ASCII data must be the 64 character subset corresponding to hex addresses 20 through 5F. This instruction creates a long busy and cannot be performed during an existing busy condition or a power down. During the busy time, the ASCII data is loaded into a memory location which corresponds to the display position held in the cursor location register.

Load Cursor Location
This instruction sets the cursor location. The instruction code is 000XXXXX where XXXXX can be any binary number 0 through 31. The cursor location serves as a pointer to one of the 32 display positions. Zero corresponds to the 1st location and 31 corresponds to the 32nd location. The left most position is the 0 location and displays of less than 32 characters use positions 0, 1, 2.... N.

Set Display Control Flag
This instruction sets or resets the individual flags which control the display and enable special instructions. The instruction code is 011XXXXY, where the XXXX is a binary number 0 through 8 which corresponds to one of the 9 flag registers, and the Y is the flag status. Y= 0 is an OFF status, while Y=1 is an ON status.

Get Character
This instruction enables an output command ($\overline{MRD}$ = 0) to fetch the ASCII code for the character pointed to by the cursor location register. After a load cursor location instruction, a time of 160 oscillator periods must be allowed before the Get Character instruction will output correct data. Bus 7 contains the busy status.

Get Cursor Location
This instruction enables a subsequent output command ($\overline{MRD}$ = 0) to fetch the cursor location. Bus 0-4 contain the cursor location, Bus 5-6 float, and Bus 7 contains the Busy status.

Get Display Control Flags
This instruction enables an output command ($\overline{MRD}$ = 0) to fetch the status of the display control flag registers. See the Instruction Set Table for details of the positioning of the flags on the bus.
Note: Any "Get" command need be given only once. Being stored on the chip, it may be used until a different "Get" instruction is needed.

Inc/Dec Cursor
The instruction code is 1000100X, where X = 1 will cause an immediate advancement of the cursor one position to the right, and X = 0 will cause an immediate advancement of one position to the left.

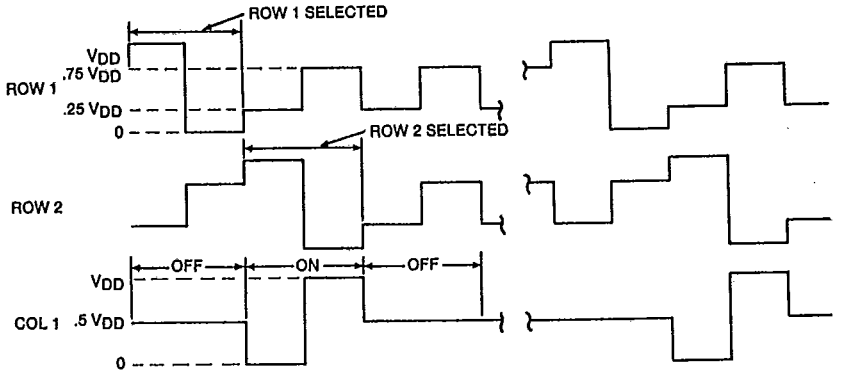
Shift
The shift right (left) instruction advances every character right (left) by one position and loads a blank into the first (last) position.

Rotate
The rotate right (left) instruction advances every character right (left) by one position and moves the last (first) character to the first (last) position.

Clear
This instruction loads a blank into every display location.

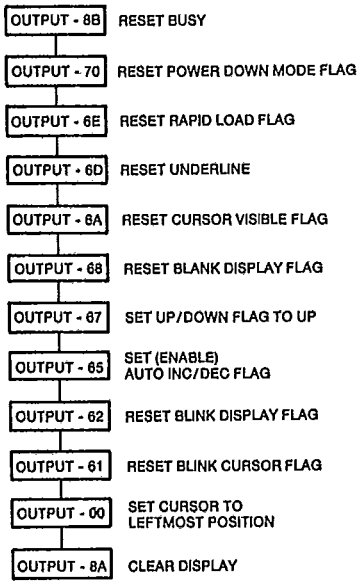
Reset Busy
This instruction aborts any instruction execution which has caused a busy signal, resets the busy flag, and allows the immediate loading of any instruction. Of course the aborted instruction may or may not have been completed.

TYPICAL OUTPUT WAVEFORMS

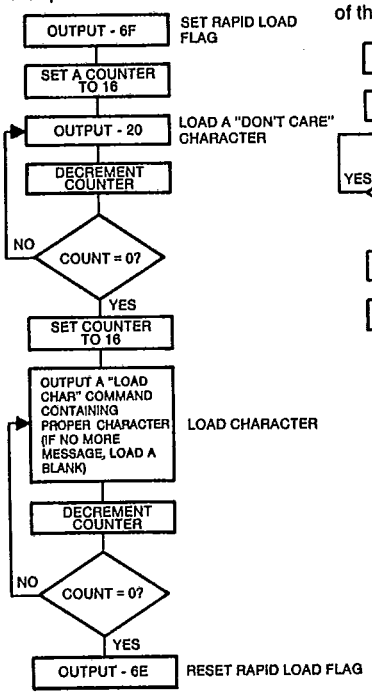


SAMPLE PROGRAMS

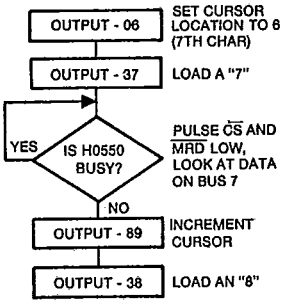
Initialize - This sequence, performed after system power up, will initialize everything, blank the cursor and set it at the left most position, and be ready for character loading from left to right.



Rapid Load Display - This sequence will display a 16 character message using the rapid load feature. Assume initialization was done as in example.



Character Load Display - Suppose the display shows the message SUM = 354.2 (left justified) and it is desired that this be changed to SUM = 357.8. Assume the initialization of the example.



DISPLAY CONTROL FLAG EXPLANATION **H0550/0551/0552**

Blink Cursor
A "1" in this flag register causes the cursor (the position pointed to by the cursor location register) to blink at approximately 1 Hz. The cursor visible flag must be set. The blinking is an on/off flashing for the underline cursor or an alternation between the character and solid fill (all 35 dots) for the full character cursor.

Blink Display
A "1" causes the entire display to flash on and off at approximately 1 Hz.

Auto Inc/Dec.
A "1" in this flag register causes the cursor location register to automatically be changed by one every time a character is read from or written to the character register. (See Up/Down flag.)

Up/Down
A "1" ("0") in this flag register works in conjunction with the Auto Inc/Dec flag to cause automatic incrementing (decrementing) of the cursor location register when a character is written to or read from the 0550.

Blank Display
A "1" in this flag register blanks the display, but leaves the display memory intact.

Visible Cursor
A "1" in this flag register causes the cursor (the position stored in the cursor location register) to be visible. The cursor cannot be blinked by the Cursor Blink flag unless it is made visible.

Cursor Type
A "1" in this register selects an underline on row 8 for the cursor, and a "0" selects a filled character, all 35 dots visible.

Power Down
A "1" in this flag register stops the oscillator and opens a switch in the resistor divider used in the multiple voltage generator circuit, so all LCD drive signals rise to the positive supply. To ensure ultra low power, the inputs should be near the power rails, and, if driven, OSC should be held high. During this condition memory is not lost, but the circuit will not respond properly to some instructions. See Table 1, column heading "Not During PD."

Busy
The busy state means the circuit is processing a previous instruction and cannot be given certain other instructions (see Table 1, column heading "Not During Busy"). Busy status will appear on Bus 7 during all output instructions, (hex. code 81, 82, and 84).

Rapid Load
A "1" in this flag register stops the oscillator and resets the circuit. Each character load instruction loads a character starting with the 31st location until the mode is terminated. Rapid load can be initiated at any time and creates a busy signal. The Rapid Load instruction needs 32 loads to function properly. No other instructions should be given during a rapid load sequence. Rapid loading does not change the cursor location.

OPERATING NOTES

1. Oscillator
The on-chip oscillator is controlled by an external capacitor. The frequency must be high enough (at least 50KHz) to ensure a flicker free display. The recommended clock output frequency is 82KHz for 64Hz update rate and 1Hz blink rate. The typical capacitor value is 100 pf.

2. The Variable Resistor
The variable resistor indicated in the system block diagram may not be necessary, but could assist in display drive optimization and is also meant to imply possible temperature compensation. The resistor may need capacitor bypass.

3. Input Signals
The H0550 will interface with signals that come from circuits with different power supply magnitudes, either higher or lower. The constraints are (1) no signal should go more positive than the positive supply (therefore positive common is recommended) and (2) input levels must be satisfied. Input swings which are more negative than supply are allowed and input levels are biased toward the positive supply. Note that input levels are referenced to $V_{DD} = (V_{CC} - [\ - V_{DIS}])$.

4. Power Supply Voltages
Two negative voltages are supplied to this chip. The microcomputer ground ($-V_{BUS}$) is used for the low output level on the I/O bus. The negative display supply ($-V_{DIS}$) is chosen to give proper levels to the LCD. $-V_{DIS}$ must be equal to or lower than $-V_{BUS}$.

5. Initialization
This circuit doesn't power up in a particular state. The recommended power up sequence is a reset busy instruction (not necessary if a long busy time period is allowed to pass), setting of all display control flags, and a clear instruction. See Sample Programs section.

6. Cascading Chips
If a display of over 32 characters is being driven, two H0550's can be used in the following manner:

a. Oscillators must be driven with common waveform
b. Give both H0550 chips simultaneous rapid load instructions to synchronize them.
c. Connect the $\overline{MRD}$, $\overline{MWR}$ and data I/O lines together. The $\overline{CS}$ signals are unique, but the two chips may, for certain purposes, be simultaneously selected.
d. The row lines of the second H0550 should not be connected to the display, unless there is a capacitive load problem.

7. RMS Drive Voltages
The RMS voltages supplied to the LCD by the H0550 and H0551/0552 are as follows:

V_{DD} = voltage across chip ($V_{CC} + V_{DIS}$)
V_{RMS} on = .424 V_{DD}
V_{RMS} off = .293 V_{DD}

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