Order Number M11T096

NEW PRODUCT

HB56A440B Series

4,194,304-Word×40-Bit High Density Dynamic RAM Module

- Under development -

HITACHI

Rev.3
May. 22. 1992

Description

The HB56A440B is a 4M×40 dynamic RAM module, mounted 10 pieces of 16Mbit DRAM (HM5116400J) sealed in SOJ package. An outline of the HB56A440B is 72-pin single in-line package.
Therefore, the HB56A440B makes high density mounting possible without surface mount technolgy. The HB56A440B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ of its module board.

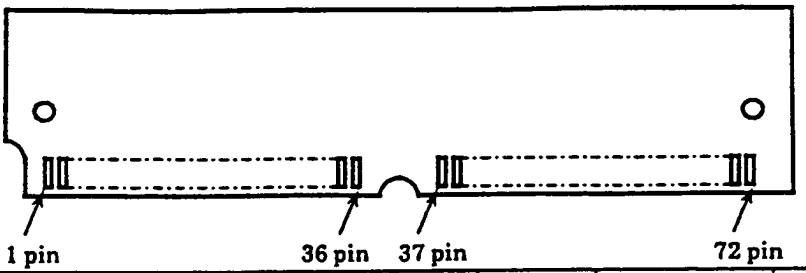
■ Feature

- 72-pin single in-line package
  - Lead pitch 1.27mm
- Single 5V (± 5%) supply
- High speed
  - Access time ..... 60ns / 70ns / 80ns / 100ns (max)
- Low power dissipation
  - Active mode ..... 4.20W / 3.68W / 3.42W / 3.15W (max)
  - Standby mode ..... 105mW (max)
- Fast page mode capability
- 4,096 refresh cycle / 64ms
- 3 variations of refresh
  - $\overline{RAS}$ only refresh
  - $\overline{CAS}$ before $\overline{RAS}$ refresh
  - Hidden refresh
- Test function

■ Ordring Information

Part No.	Access time	Package
HB56A440B–6	60ns	72-pin single in-line package
HB56A440B–7	70ns	
HB56A440B–8	80ns	
HB56A440B–10	100ns	

■ Pinout



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	$\overline{OE}$	37	DQ19	55	DQ28
2	DQ0	20	DQ8	38	DQ20	56	DQ29
3	DQ1	21	DQ9	39	V_{SS}	57	DQ30
4	DQ2	22	DQ10	40	$\overline{CAS0}$	58	DQ31
5	DQ3	23	DQ11	41	A10	59	V_{CC}
6	DQ4	24	DQ12	42	A11	60	DQ32
7	DQ5	25	DQ13	43	NC	61	DQ33
8	DQ6	26	DQ14	44	$\overline{RAS0}$	62	DQ34
9	DQ7	27	DQ15	45	NC	63	DQ35
10	V_{CC}	28	A7	46	DQ21	64	DQ36
11	PD4	29	DQ16	47	$\overline{WE}$	65	DQ37
12	A0	30	V_{CC}	48	×40 (V_{SS})	66	DQ38
13	A1	31	A8	49	DQ22	67	PD0
14	A2	32	A9	50	DQ23	68	PD1
15	A3	33	NC	51	DQ24	69	PD2
16	A4	34	NC	52	DQ25	70	PD3
17	A5	35	DQ17	53	DQ26	71	DQ39
18	A6	36	DQ18	54	DQ27	72	V_{SS}

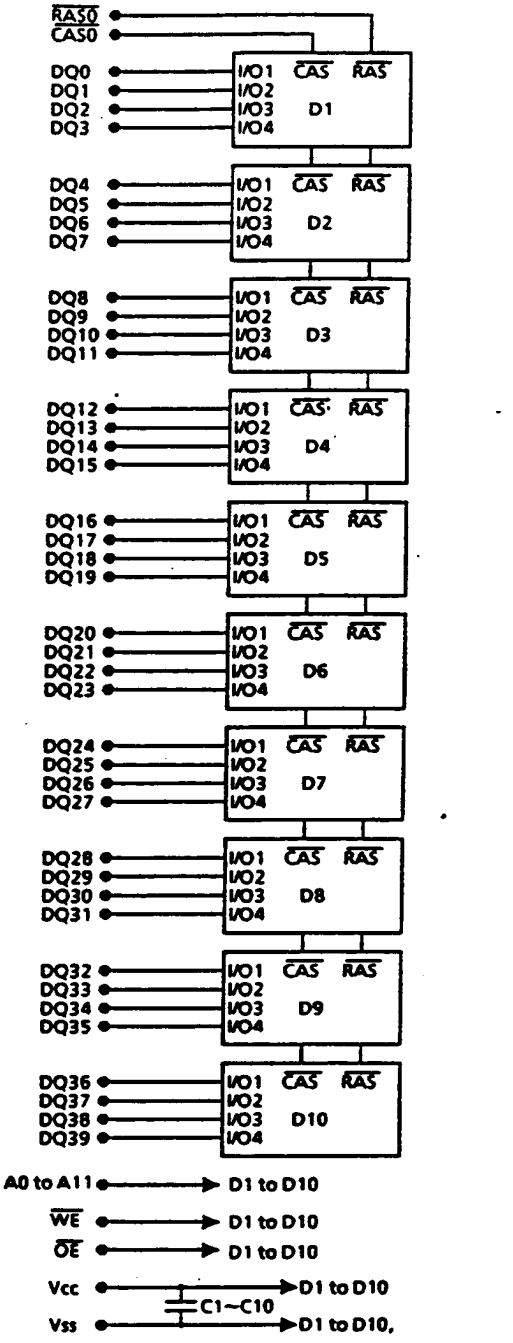
■ Pin Description

Pin Name	Function
A0 – A11	Address Input : A0 – A11 Row Address : A0 – A11 Column Address: A0 – A9 Refresh Address: A0 – A11
DQ0 – DQ39	Data-in / Data-out
$\overline{CAS0}$	Column Address Strobe
$\overline{RAS0}$	Row Address Strobe
$\overline{WE}$	Read / Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
PD0 – PD4	Presence Detect Pin
NC	No connection

■ Presence Detect Pin

Pin No.	Pin Name	-6	-7	-8	-10
67	PD0	V_{SS}	V_{SS}	V_{SS}	V_{SS}
68	PD1	NC	NC	NC	NC
69	PD2	NC	V_{SS}	NC	V_{SS}
70	PD3	NC	NC	V_{SS}	V_{SS}
11	PD4	V_{SS}	V_{SS}	V_{SS}	V_{SS}

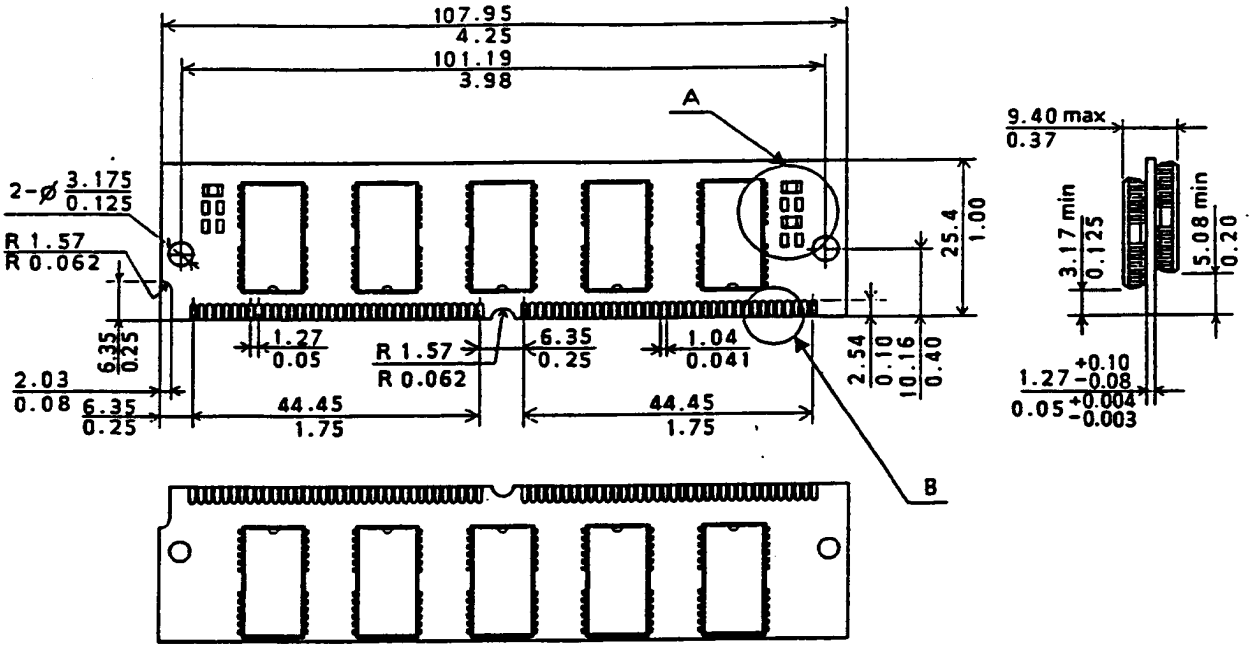
■ Block Diagram



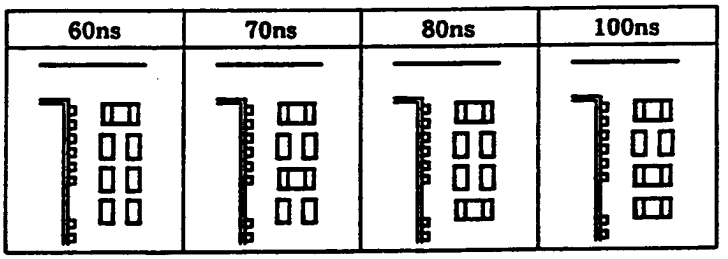
* D1 to D10 : HM5116400J

■ Physical Outline

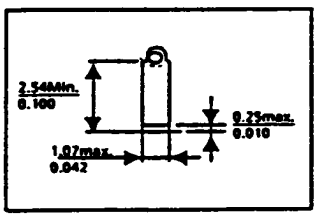
Unit : mm / inch



Detail A



Detail B



■ Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	10	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

■ Electrical Characteristics

☆ Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	−	5.5	V	1
Input low voltage	V_{IL}	−1.0	−	0.8	V	1

Note : 1. All voltage referenced to V_{SS}

☆ DC Electrical Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Parameter	Symbol	-6		-7		-8		-10		Unit	Test Condition	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.			
Operating current	I_{CC1}	–	800	–	700	–	650	–	600	mA	t_{RC} = min	1,2
Standby current	I_{CC2}	–	20	–	20	–	20	–	20	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		–	10	–	10	–	10	–	10	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≧ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	–	800	–	700	–	650	–	600	mA	t_{RC} = min	2
Standby current	I_{CC5}	–	50	–	50	–	50	–	50	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	–	800	–	700	–	650	–	600	mA	t_{RC} = min	
Page mode current	I_{CC7}	–	900	–	800	–	750	–	700	mA	t_{PC} = min	1,3
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	−10	10	μA	0V ≦ V_{in} ≦ 7V	
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	−10	10	μA	0V ≦ V_{out} ≦ 7V D_{OUT} = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.

3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

☆ Capacitance (Ta = 25°C, V_{CC} = 5V ± 5%)

Parameter		Symbol	Typ.	Max.	Unit	Note
Input capacitance	(Address)	C_{I1}	–	90	pF	1
Input capacitance	($\overline{WE}$, $\overline{OE}$)	C_{I2}	–	90	pF	1
Input capacitance	($\overline{RAS}$, $\overline{CAS}$)	C_{I3}	–	90	pF	1
Output capacitance	(DQ)	$C_{I/O1}$	–	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

☆ AC Characteristics (Ta = 0 to 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V) 1), 2), 3), 19), 20)

● Read, Write and Refresh Cycle (Common parameters)

Parameter	Symbol	-6		-7		-8		-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Ramdom read or write cycle time	t_{RC}	110	–	130	–	150	–	180	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	60	–	70	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	18	10000	20	10000	25	10000	ns	
Row address setup time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	10	–	10	–	10	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	15	–	15	–	15	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	52	20	60	20	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	15	55	ns	5
$\overline{RAS}$ hold time	t_{RSH}	15	–	18	–	20	–	25	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	80	–	100	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	5	–	ns	
$\overline{OE}$ to Din delay time	t_{OED}	15	–	18	–	20	–	25	–	ns	6
$\overline{OE}$ delay time from Din	t_{DZO}	0	–	0	–	0	–	0	–	ns	7
$\overline{CAS}$ delay time from Din	t_{DZC}	0	–	0	–	0	–	0	–	ns	7
Transition time (rise and fall)	t_T	3	30	3	30	3	30	3	30	ns	8
Refresh period	t_{REF}	–	64	–	64	–	64	–	64	ms	22

• Read Cycle

Parameter	Symbol	-6		-7		-8		-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	–	80	–	100	ns	9,10,21
Access time from $\overline{CAS}$	t_{CAC}	–	15	–	18	–	20	–	25	ns	10,11, 18,21
Access time from address	t_{AA}	–	30	–	35	–	40	–	45	ns	10,12, 18,21
Access time from $\overline{OE}$	t_{OEA}	–	15	–	18	–	20	–	25	ns	10,21
Read command setup time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	13
Read command hold time to $\overline{RAS}$	t_{RRH}	5	–	5	–	5	–	5	–	ns	13
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	40	–	45	–	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	30	–	35	–	40	–	45	–	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	–	0	–	0	–	0	–	ns	
Output data hold time	t_{OH}	3	–	3	–	3	–	3	–	ns	
Output data hold time from $\overline{OE}$	t_{OHO}	3	–	3	–	3	–	3	–	ns	
Output buffer turn-off time	t_{OFF}	–	15	–	18	–	20	–	25	ns	14
Output buffer turn-off to $\overline{OE}$	t_{OEZ}	–	15	–	18	–	20	–	25	ns	14
$\overline{CAS}$ to Din delay time	t_{CDD}	15	–	18	–	20	–	25	–	ns	6

• Write Cycle

Parameter	Symbol	-6		-7		-8		-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Write command setup time	t_{WCS}	0	–	0	–	0	–	0	–	ns	15
Write command hold time	t_{WCH}	15	–	15	–	15	–	15	–	ns	
Write command pulse width	t_{WP}	15	–	15	–	15	–	15	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	18	–	20	–	25	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	18	–	20	–	25	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	0	–	ns	16
Data-in hold time	t_{DH}	15	–	15	–	15	–	15	–	ns	16

- Read-Modify-Write Cycle

Parameter	Symbol	-6		-7		-8		-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Read-modify-write cycle time	t_{RWC}	155	–	181	–	205	–	245	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	85	–	98	–	110	–	135	–	ns	15
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	40	–	46	–	50	–	60	–	ns	15
Column address to $\overline{WE}$ delay time	t_{AWD}	55	–	63	–	70	–	80	–	ns	15
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	15	–	18	–	20	–	25	–	ns	

- Refresh Cycle

Parameter	Symbol	-6		-7		-8		-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	10	–	10	–	10	–	10	–	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	20	–	20	–	20	–	20	–	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	10	–	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	0	–	0	–	0	–	0	–	ns	

- Fast Page Mode Cycle

Parameter	Symbol	-6		-7		-8		-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Fast page mode cycle time	t_{PC}	40	–	45	–	50	–	55	–	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASP}	–	100000	–	100000	–	100000	–	100000	ns	17
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	35	–	40	–	45	–	50	ns	10,18, 21
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	35	–	40	–	45	–	50	–	ns	

- Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	-6		-7		-8		-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Fast page mode read-modify-write cycle time	t_{PRWC}	85	–	96	–	105	–	120	–	ns	
$\overline{WE}$ delay time from CAS precharge	t_{CPW}	60	–	68	–	75	–	85	–	ns	15

- Test Mode Cycle *20)

Parameter	Symbol	-6		-7		-8		-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Test mode $\overline{WE}$ setup time	t_{WTS}	10	–	10	–	10	–	10	–	ns	
Test mode $\overline{WE}$ hold time	t_{WTH}	10	–	10	–	10	–	10	–	ns	

- Counter Test Cycle

Parameter	Symbol	-6		-7		-8		-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
CAS precharge time in counter test cycle	t_{CPT}	40	–	40	–	40	–	50	–	ns	

Notes

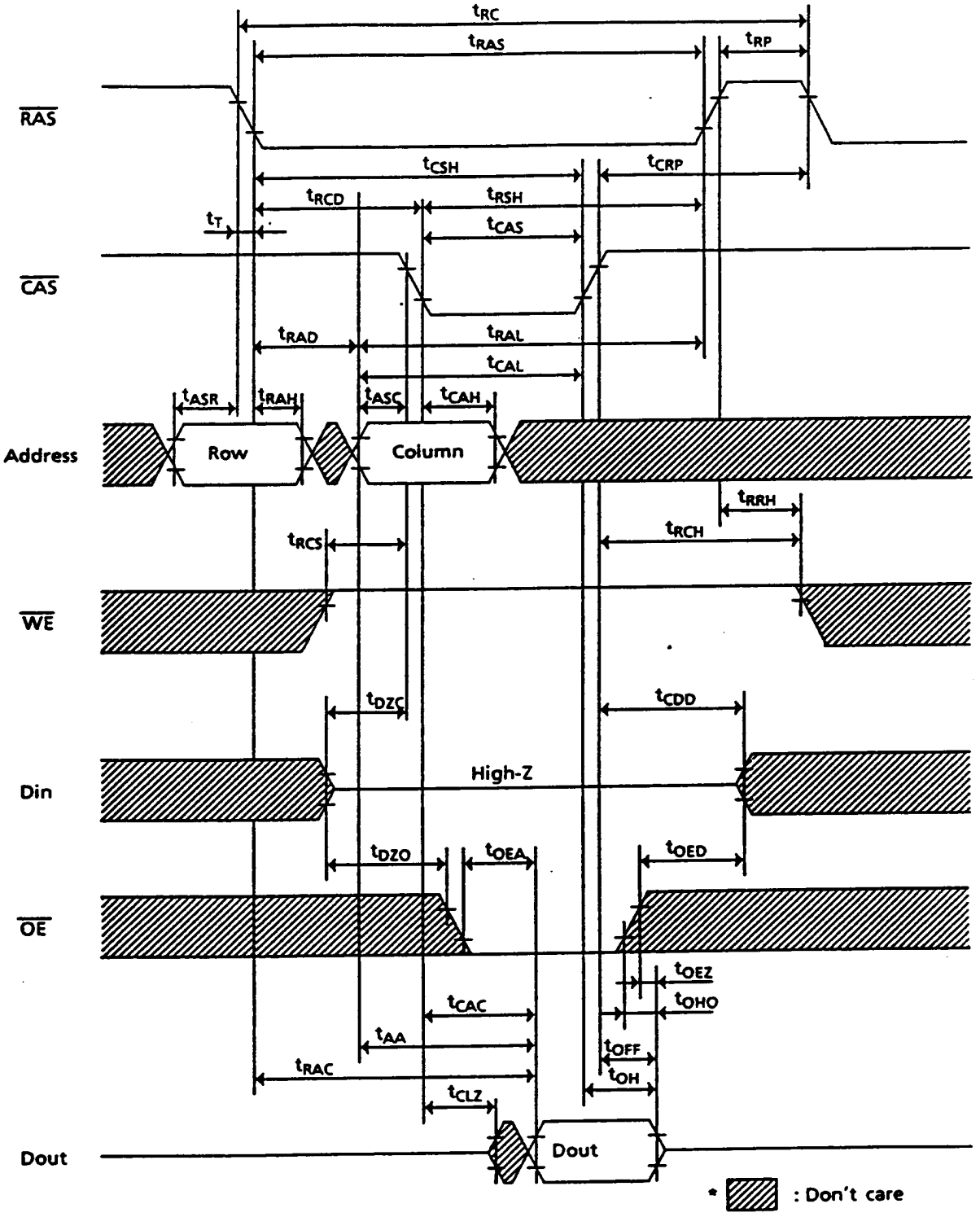
1. AC measurements assume $t_T = 5ns$.
2. An initial pause of 100μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minmum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Only row address is indispensable on address A10 and A11.
4. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
6. Either t_{OED} or t_{CDD} must be satisfied.
7. Either t_{DZO} or t_{DZC} must be satisfied.
8. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL}(max).
9. Assumes that $t_{RCD} < t_{RCD}$(max) and $t_{RAD} < t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
10. Measured with a load circuit equivalent to 2TTL loads and 100pF.
11. Assumes that $t_{RCD} \geq t_{RCD}$(max) and $t_{RAD} \leq t_{RAD}$(max).
12. Assumes that $t_{RCD} \leq t_{RCD}$(max) and $t_{RAD} \geq t_{RAD}$(max).
13. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
14. t_{OFF}(max) and t_{OEZ}(max) is define the time at which the output achieve the open circuit condition and are not referenced to output voltage levels.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), or $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPW} \geq t_{CPW}$(min) the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
16. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
17. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
18. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
19. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OEH} \geq t_{CWL}$, the I/O pins will remain open circuit (high impedance) ; if $t_{OEH} < t_{CWL}$, invalid data will be out at each I/O.

Notes (Continued):

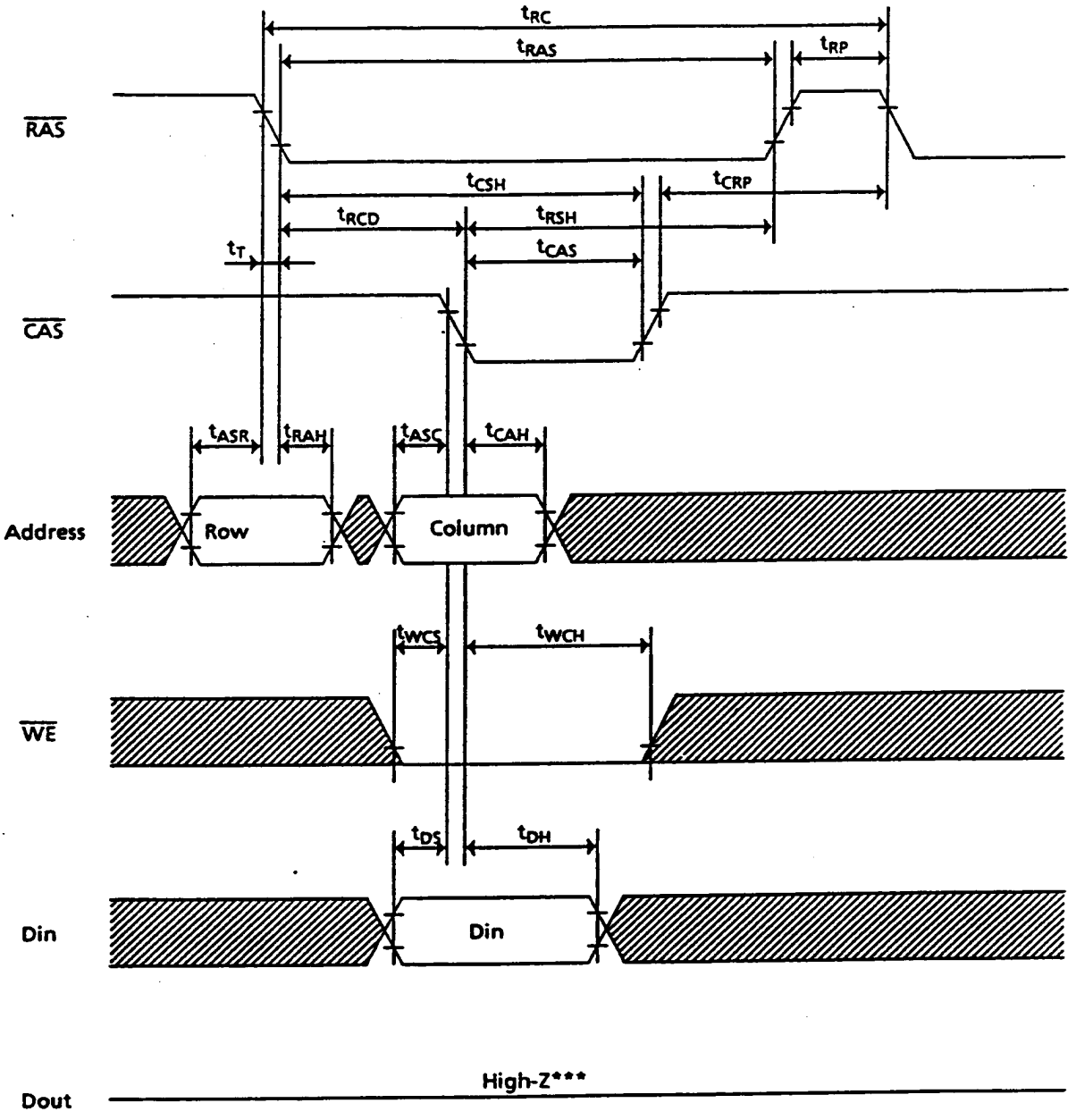
20. The 16M DRAM offers a 16-bits time saving parallel test mode. Address CA0 and CA1 for the 4M × 4 are don't care during test mode. Test mode is set by performing a $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) cycle. In 16-bits parallel test mode, data is written into 4 bits in parallel at each I/O and read out from each I/O. If 4 bits of each I/O are equal (all 1s or 0s), data output pin is a high state during test mode read cycle, then the device has passed. If they are not equal, data output pin is a low state, then the device has failed. Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles. To get out of test mode and enter a normal operation mode, perform either a regular $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle or $\overline{RAS}$-only refresh cycle.
21. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{CPA} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
22. t_{REF} is determined by 4,096 refresh cycles.

■ Timing Waveform

Read Cycle



Early Write Cycle

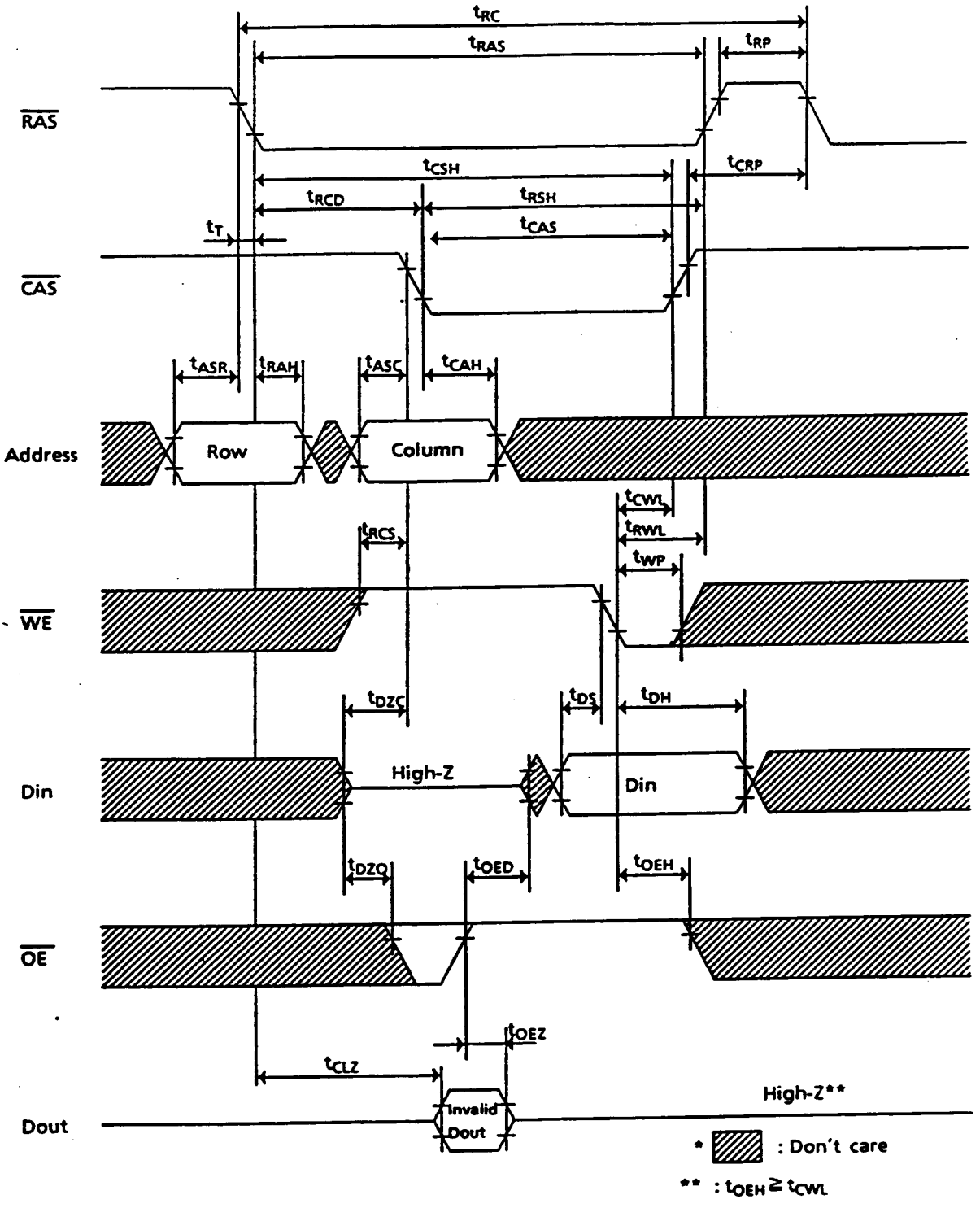


* $\overline{OE}$: Don't care

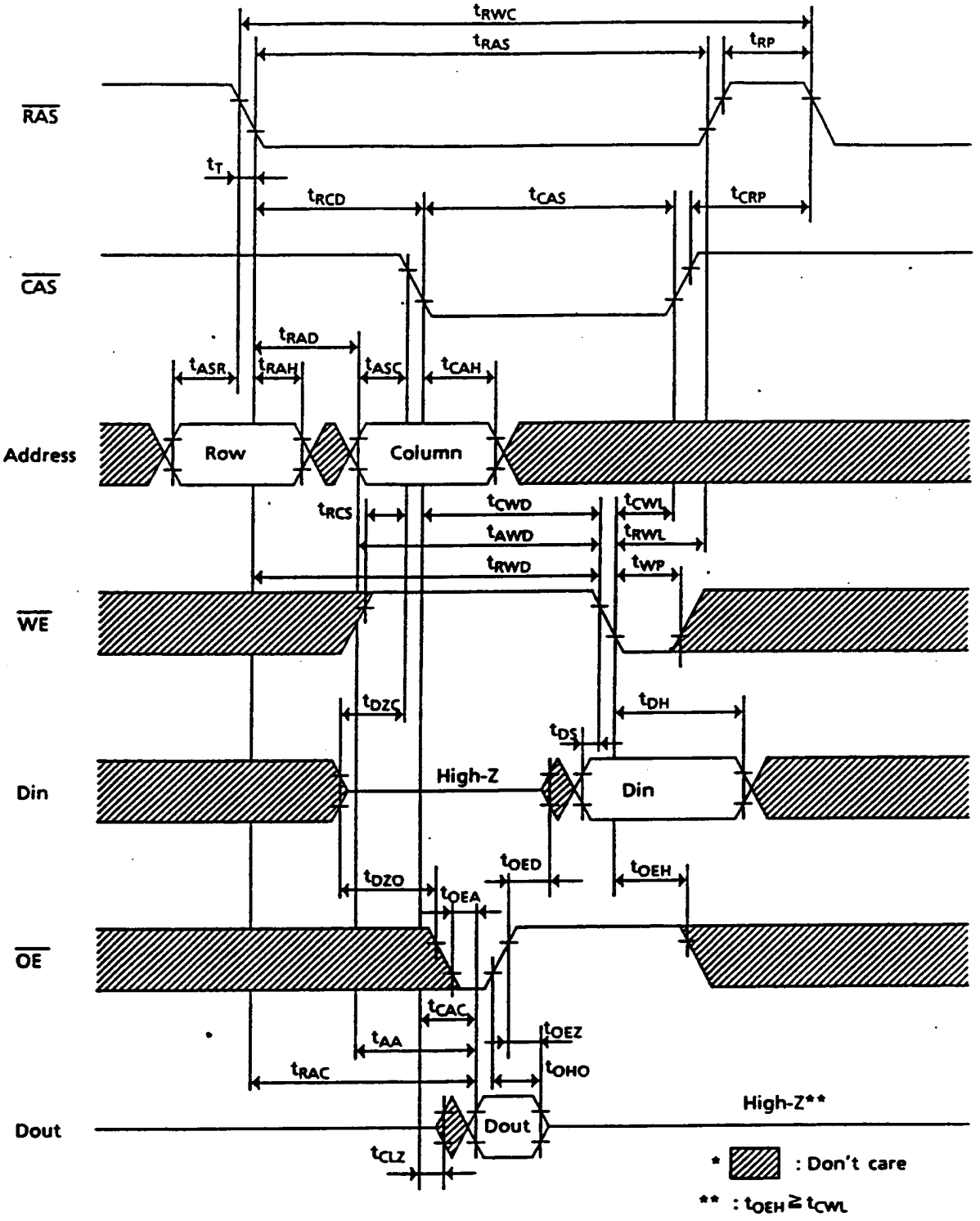
** : Don't care

*** $t_{WCS} \geq t_{WCS}$ (min)

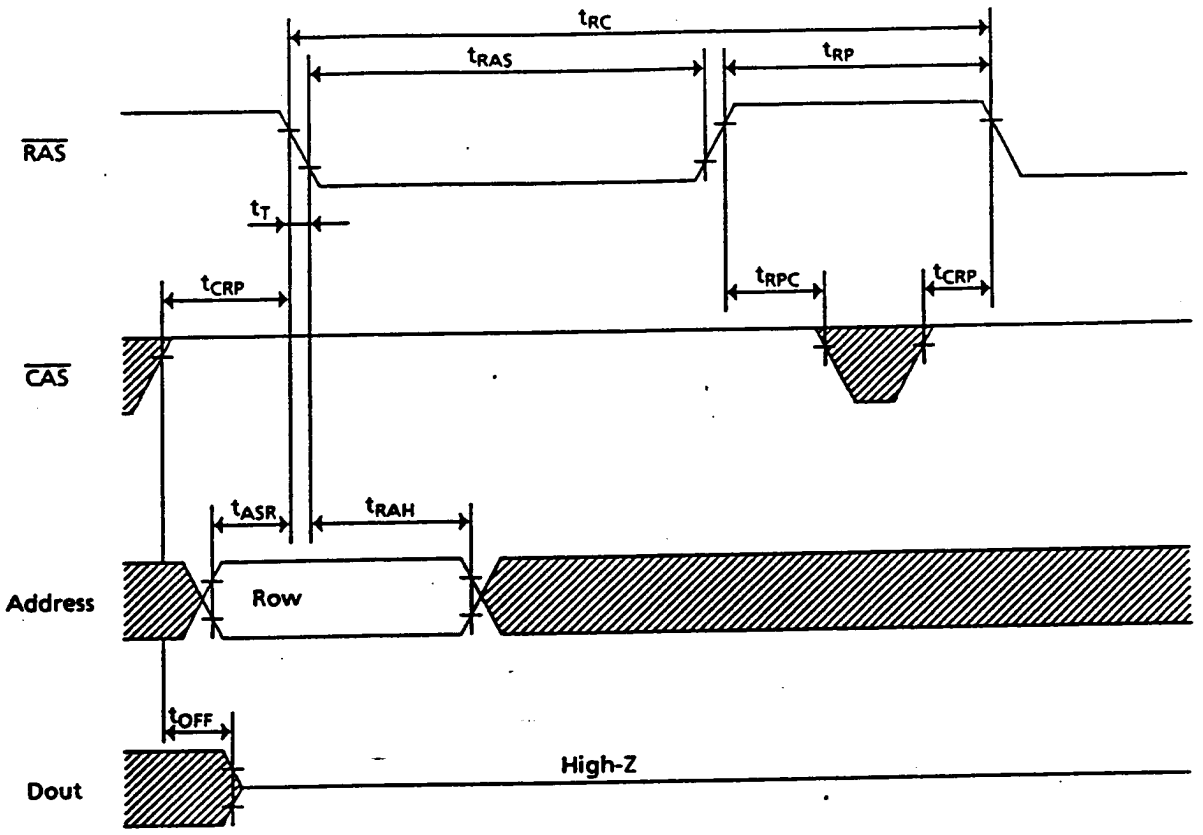
Delayed Write Cycle *19



Read-Modify-Write Cycle *19

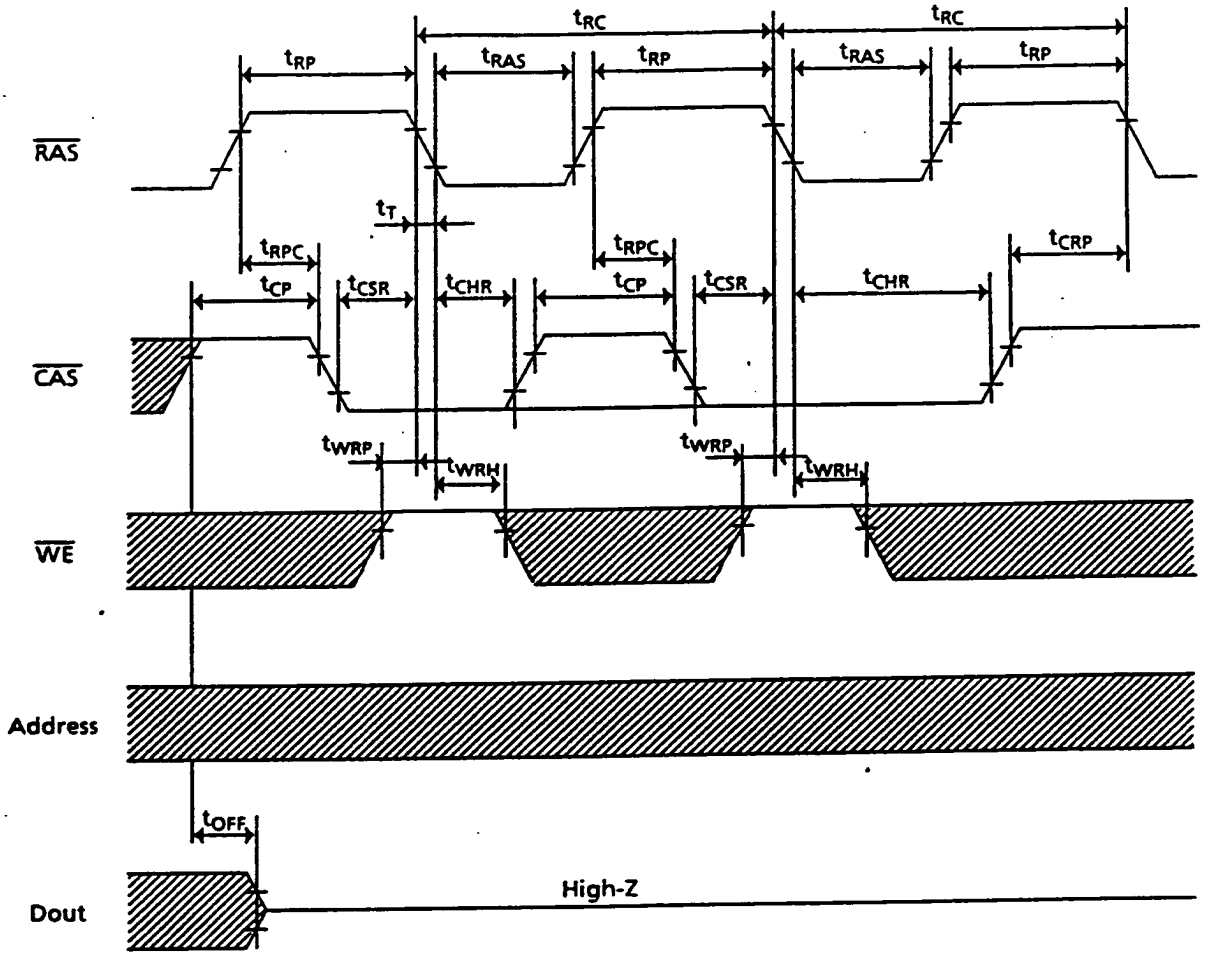


$\overline{RAS}$-Only Refresh Cycle



* $\overline{OE}$, $\overline{WE}$: Don't care
** ▨ : Don't care
*** Refresh address : A0 – A11 (RA0 – RA11)

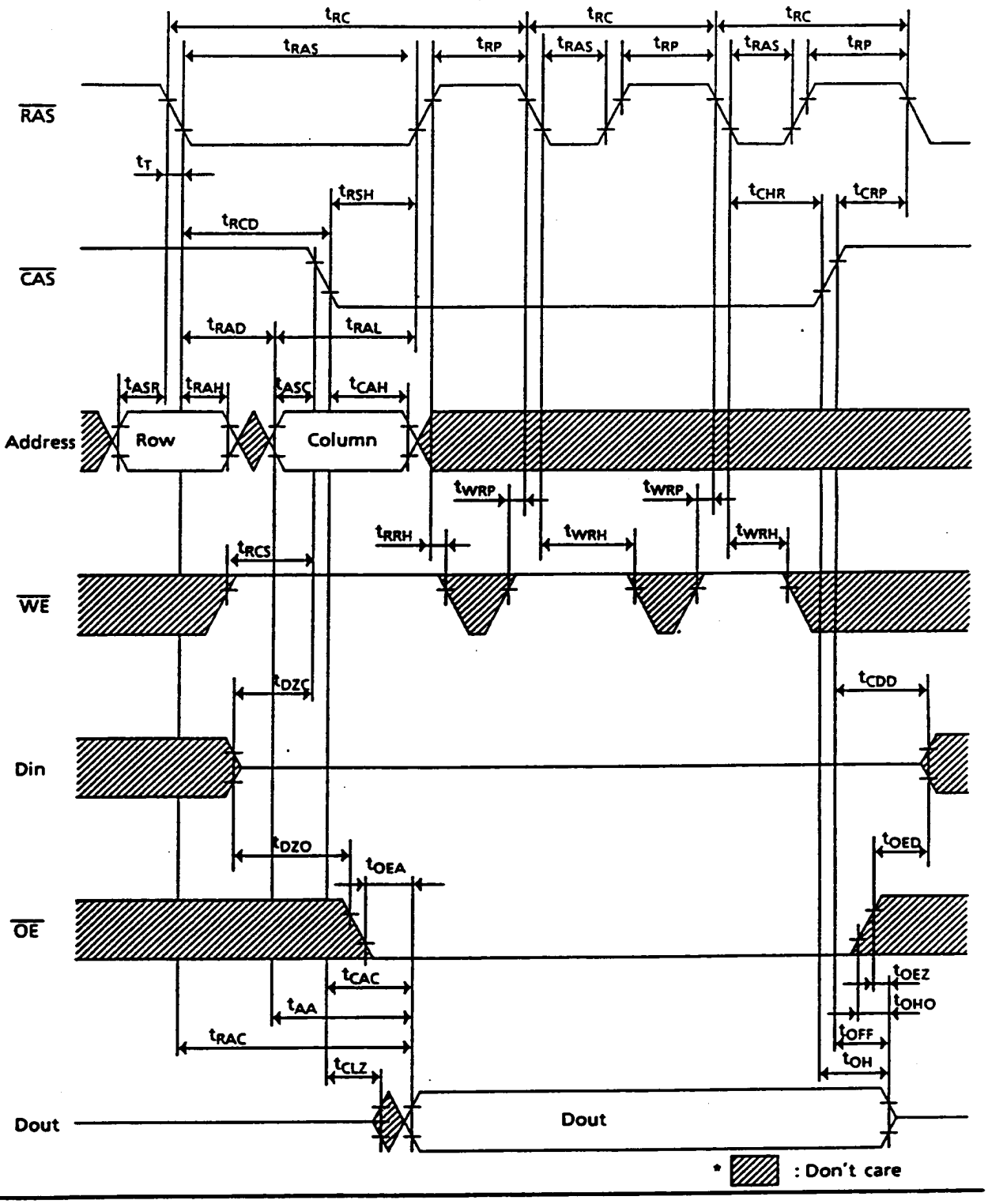
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



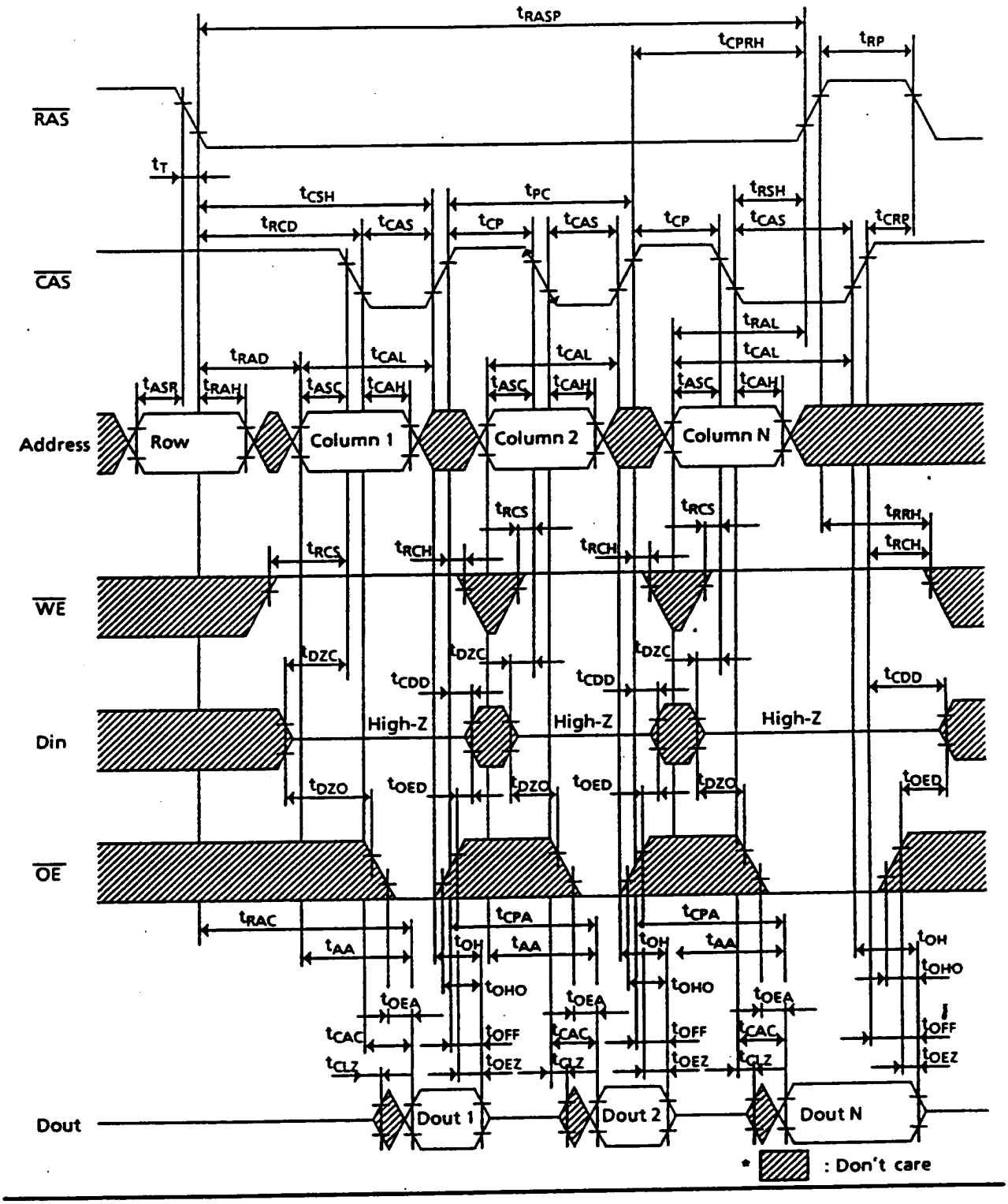
* $\overline{OE}$: Don't care

** : Don't care

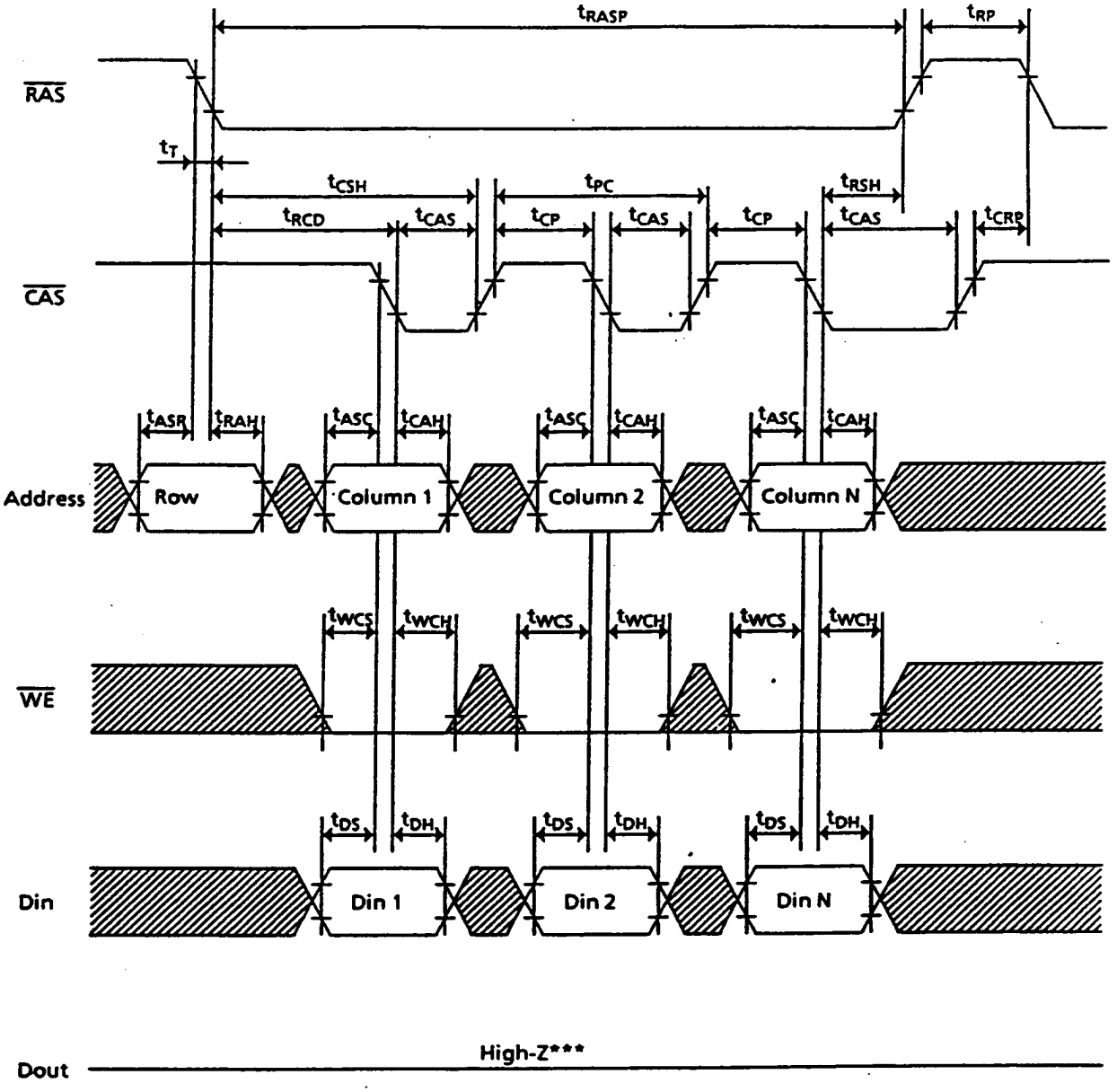
Hidden Refresh Cycle



Fast Page Mode Read Cycle



Fast Page Mode Early Write Cycle

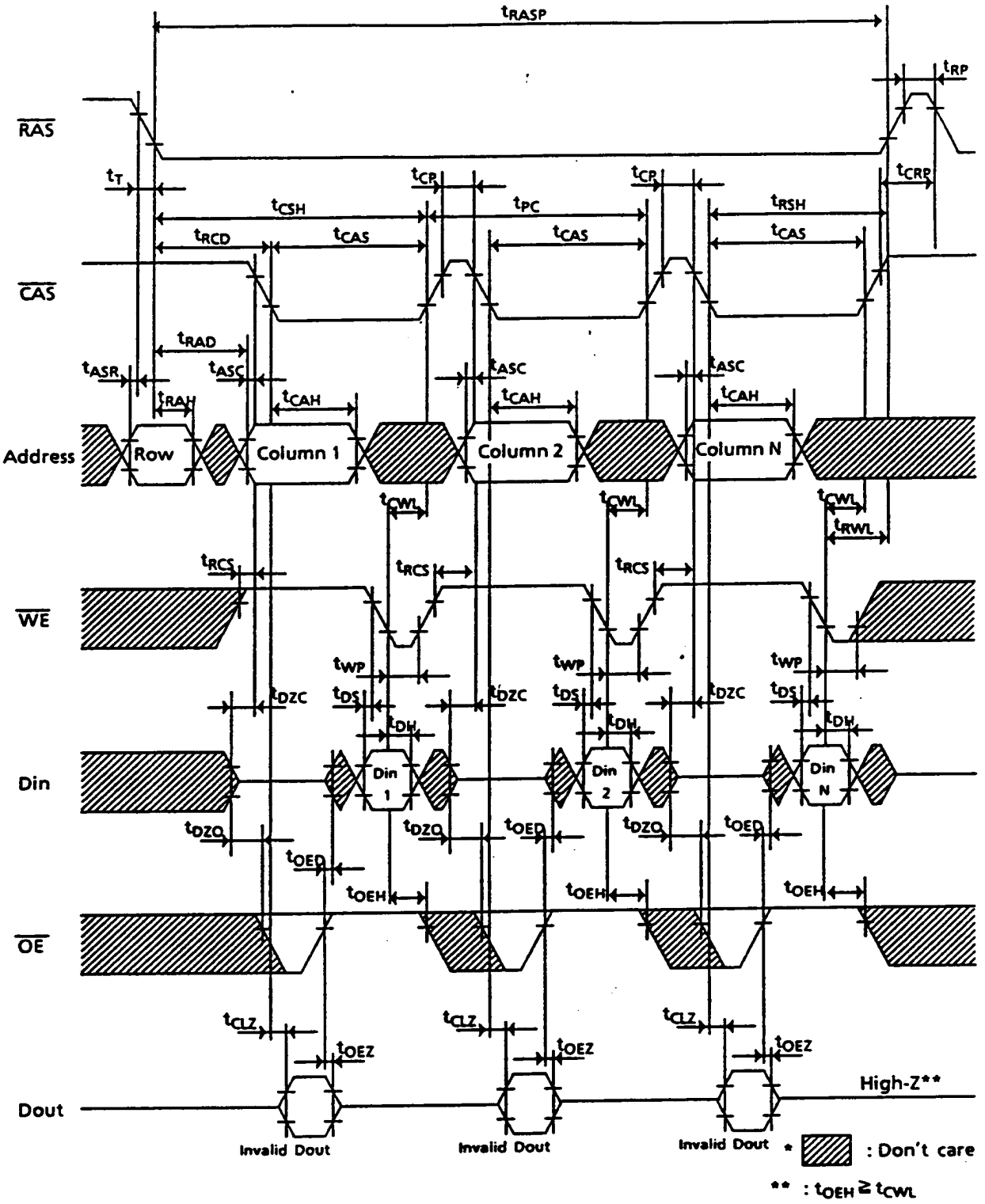


* $\overline{OE}$: Don't care

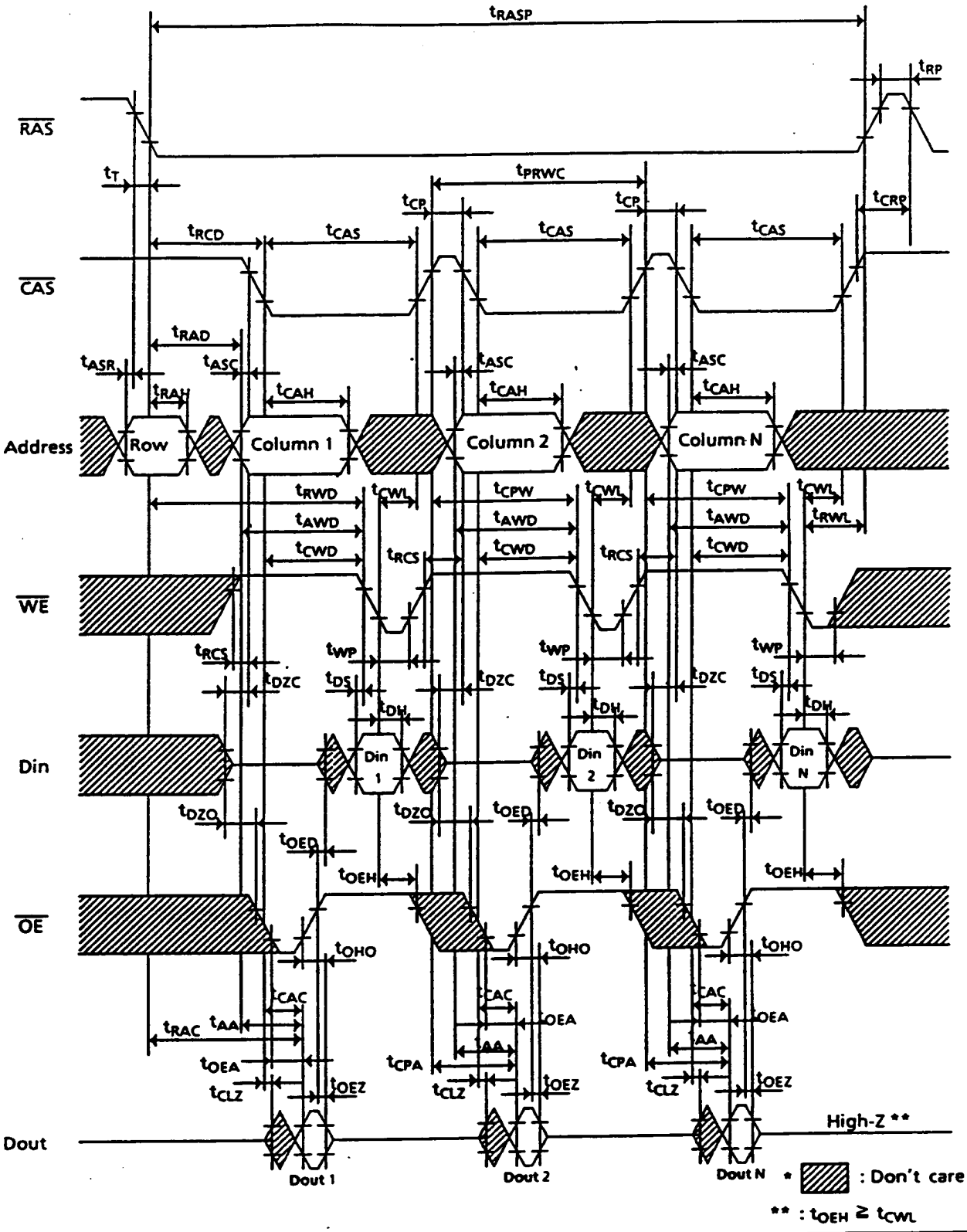
** ▨ : Don't care

*** $t_{WCS} \geq t_{WCS}$ (min)

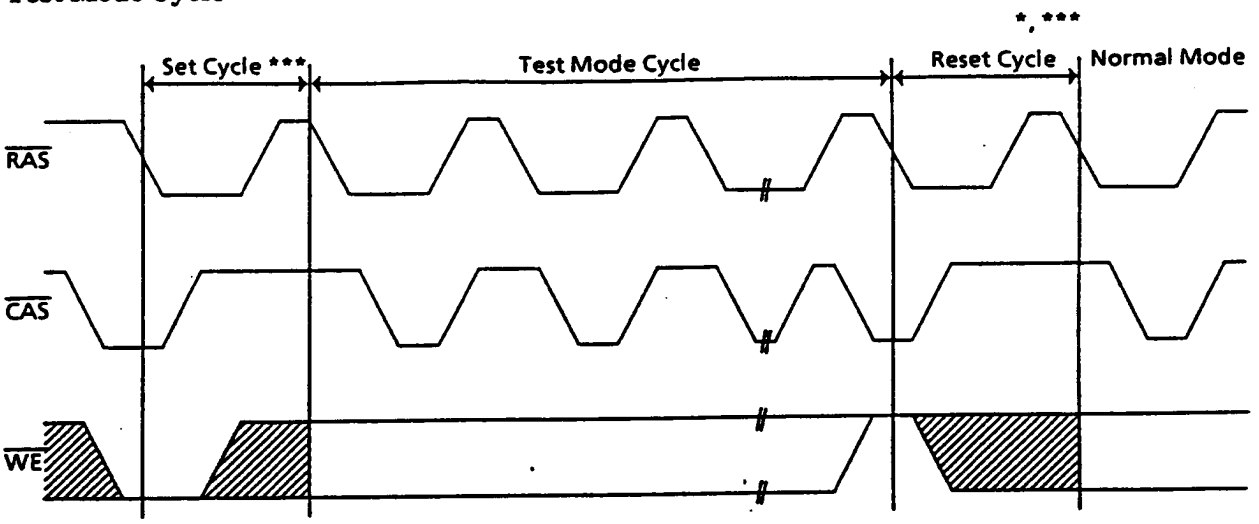
Fast Page Mode Delayed Write Cycle *19



Fast Page Mode Read-Modify-Write Cycle *19

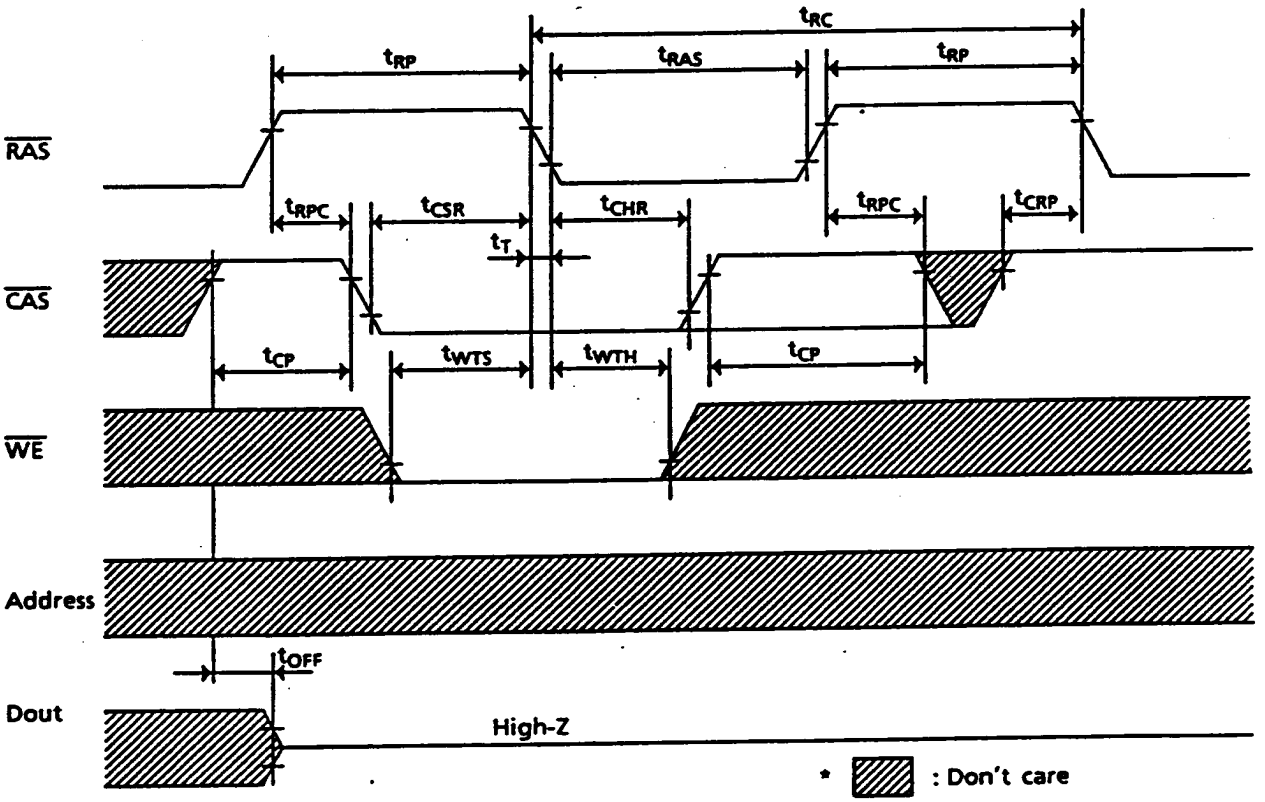


Test Mode Cycle *20



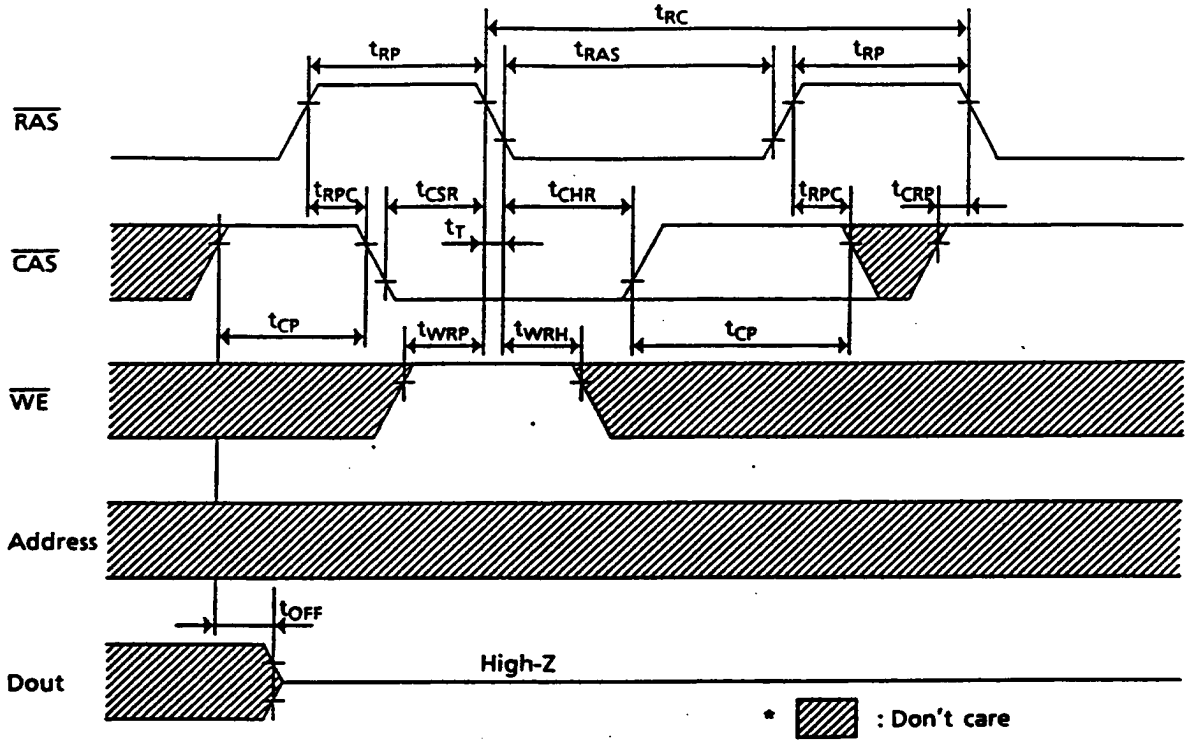
* CBR or $\overline{RAS}$ only refresh
** ▨ : Don't care
*** Address, Din, $\overline{OE}$: Don't care

Test Mode Set Cycle

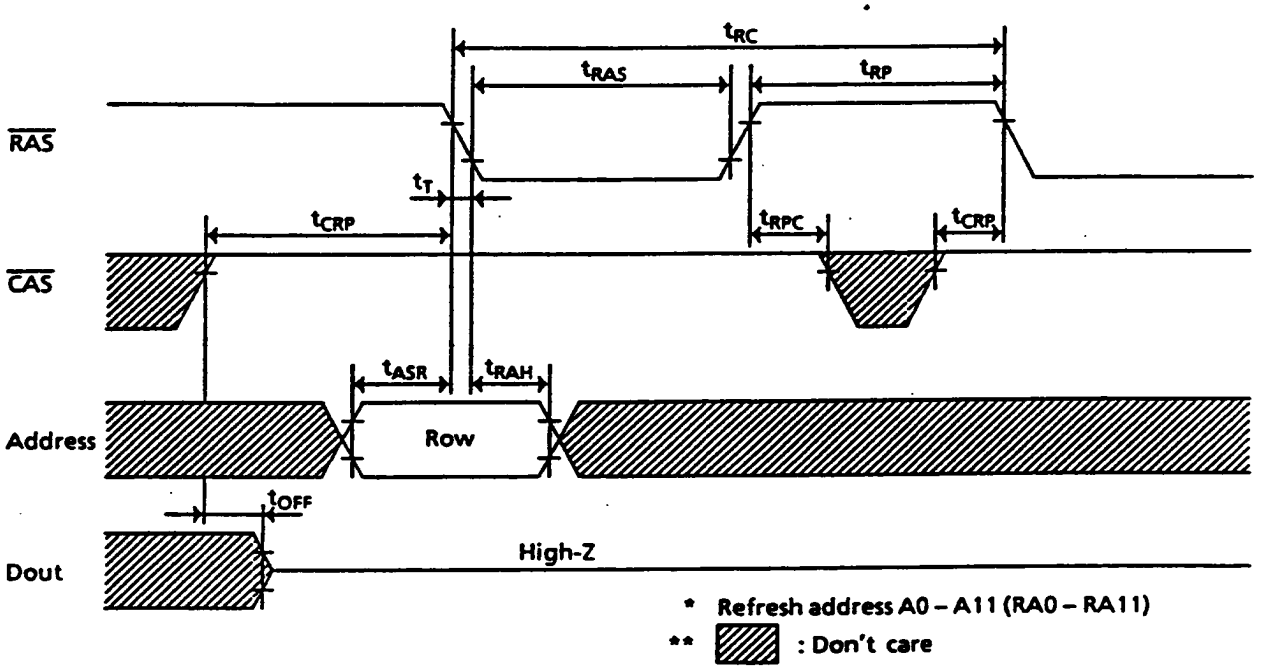


Test Mode Reset Cycle

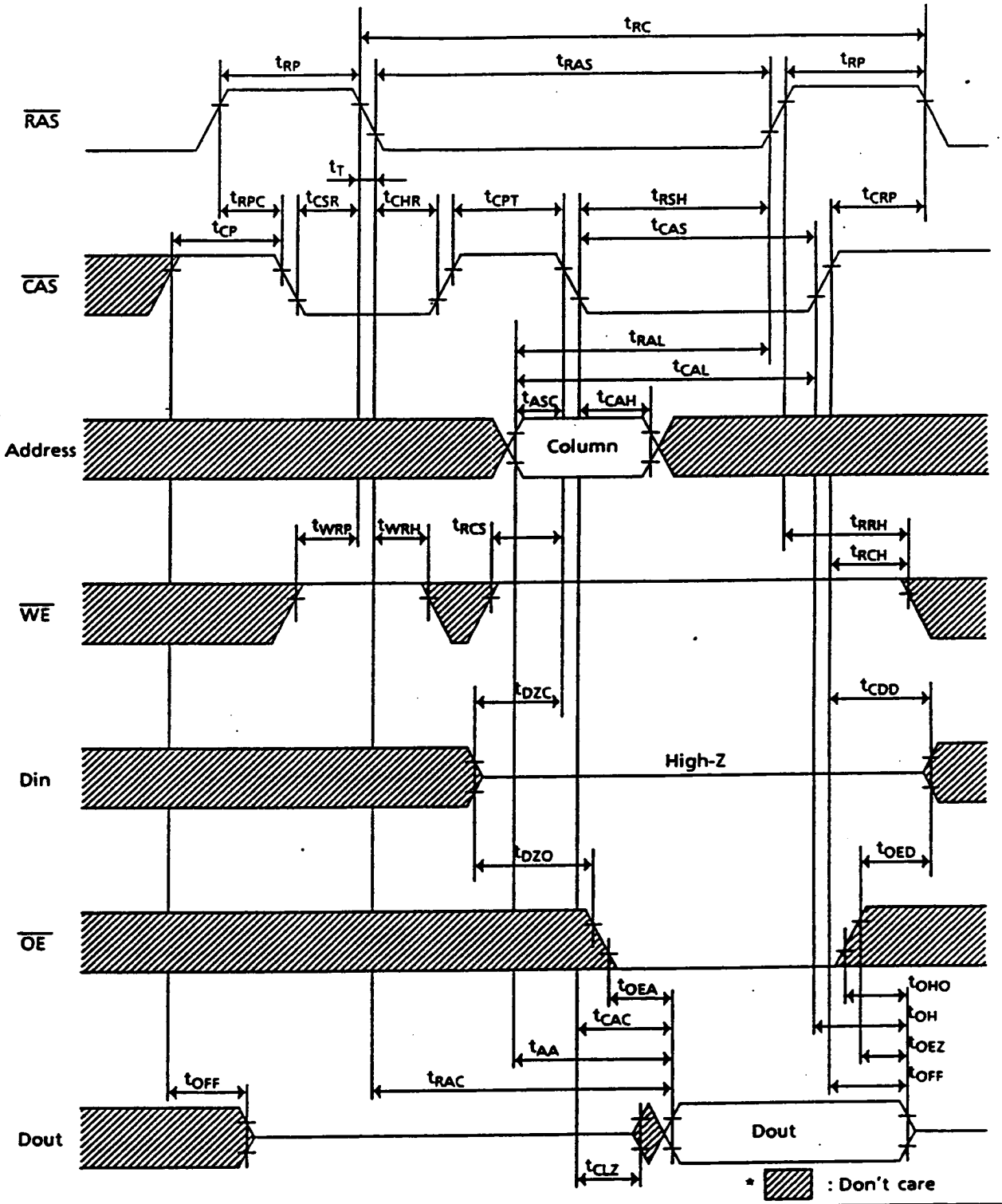
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



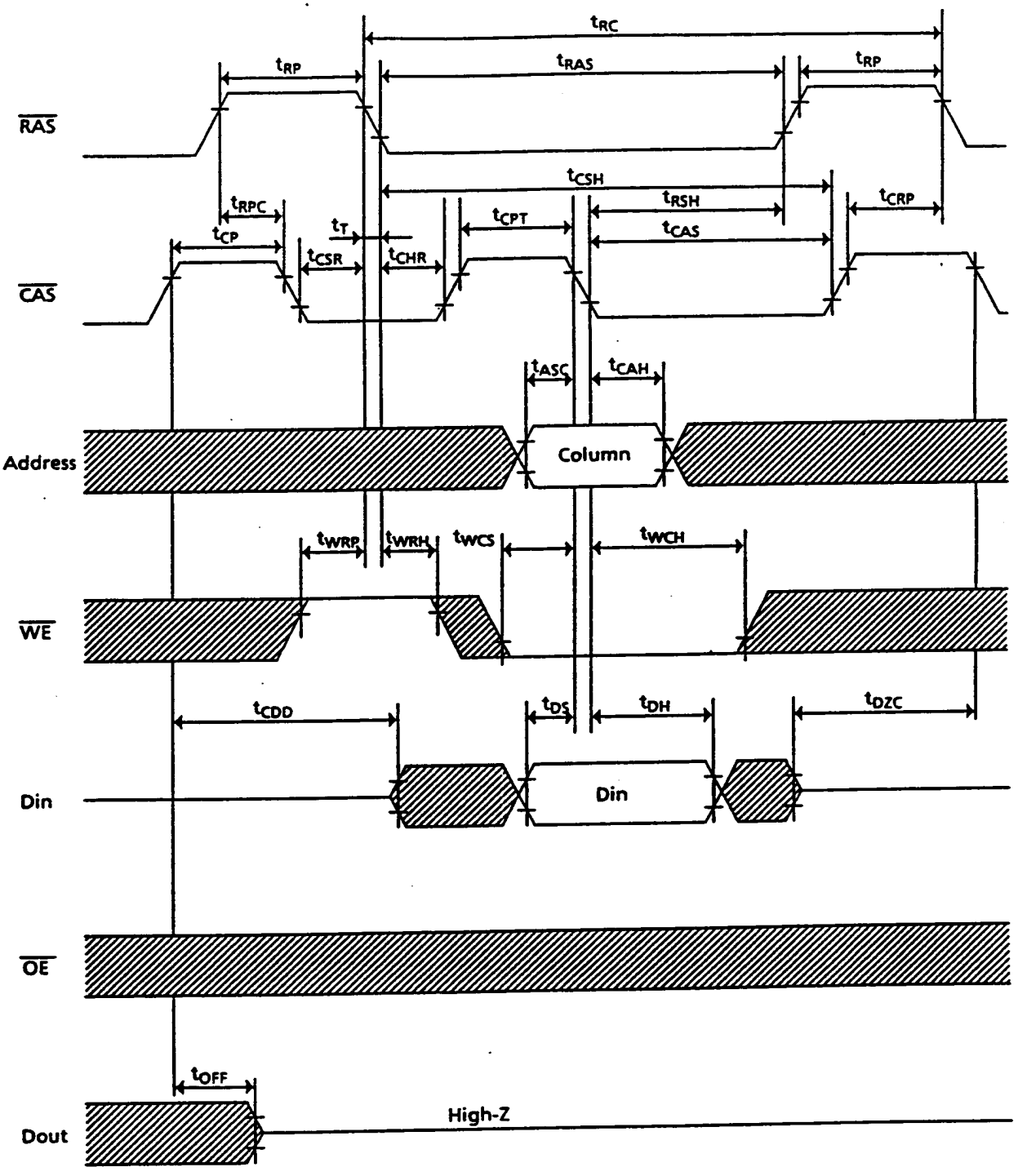
$\overline{RAS}$-Only Refresh Cycle



$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Counter Check Cycle (Read)



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Write)



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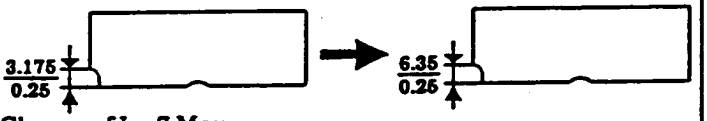
■ Revision Record

Rev.	Data	Content of Modification	Drawn by	Approved by
0	Jun.03,'91	Initial issue	T.Sugano	K.Inoue
1	Nov.08,'91	Add presence detect pin for PD5 and PD6. Change of pin out for A10,A11 and PD2. Change of $I_{CC}7$ Max. 800/700/650/600mA→700/600/500/450mA Change of t_{RWC} Min. 150/176/200/245ns→155/181/205/245ns Change of t_{RWD} Min. 80/93/105/135ns→85/98/110/135ns Change of t_{CWD} Min. 35/41/45/60ns→40/46/50/60ns Change of t_{AWD} Min. 50/58/65/80ns→55/63/70/80ns Change of t_{PRWC} Min. 80/91/100/110ns→85/96/105/120ns Change of t_{CPW} Min. 55/63/70/85ns→60/68/75/85ns Change of Hidden Refresh timing waveform.	T.Sugano	K.Inoue
2	May.22,'92	This specification is based on JEDEC standard for ×40. · Pin out Pin No.2 : DQ0 → DQ0 Pin No.3 : DQ16 → DQ1 Pin No.4 : DQ1 → DQ2 Pin No.5 : DQ17 → DQ3 Pin No.48 : V_{SS}→×40(V_{SS}) PD1−6→PD0−4 · Outline  Change of $I_{CC}7$ Max. 700/600/500/450mA→900/800/750/700mA	T.Sugano	O.Ichai