

Hot Rod Update

The following changes have been made to the Hot Rod data sheet, dated July, 1991:

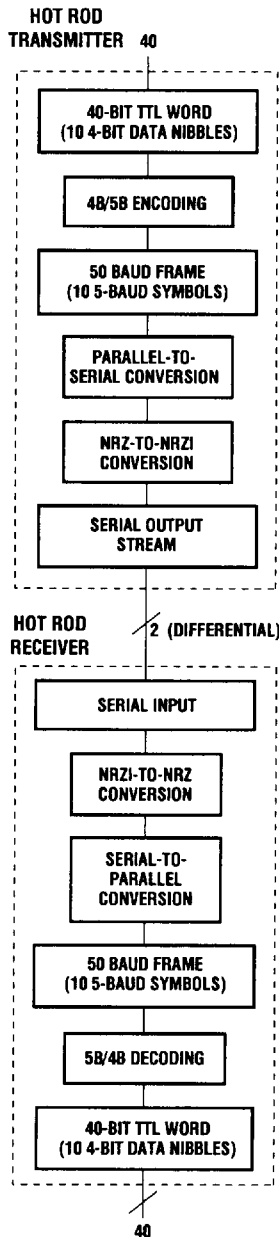
- The maximum transmit strobe interval requirement for guaranteed data integrity has been removed (p. 23).
- Recommended Operating Conditions have been significantly improved (p. 23).
- The PECL specifications have been modified (pp. 24, 25).
- The differentiator for the new version of the transmitter is found in the date code, i.e. 9230 H.

Nomenclature

In the Hot Rod protocol, each group of four data bits are encoded into five bauds for transmission. To avoid confusion, the following definitions are used throughout the data sheet.

Bit	- one unit of user data
Baud	- one unit of information on the serial link
Nibble	- 4 data bits
Symbol	- 5 bauds
Word	- 40 data bits, or 10 nibbles
Frame	- 50 bauds, or 10 symbols
Bit Rate	- Rate at which user data bits are transferred
Word Rate	- Rate at which user data words are transferred
Baud Rate	- Rate of baud transmission over the serial media
Sync Frame	- Predefined frame used for synchronization

Figure 1. Chip Set Data Flow



Communications Protocol Unidirectional Link

Each Hot Rod chip set consists of one Hot Rod transmitter and one Hot Rod receiver and provides a unidirectional 800 Mbit/sec point-to-point communications capability. The chip set appears to the system as a 40-bit parallel register. The transmitter accepts a 40-bit word of TTL-level data; some time later the receiver outputs the same 40-bit parallel word on its TTL-level bus. All internal operations, as well as the serial interface, are transparent to the system.

Data Flow

As shown in Figure 1, the 40-bit data word input to the transmitter undergoes many transformations before it is output on the receiver's parallel bus. The sequence is as follows:

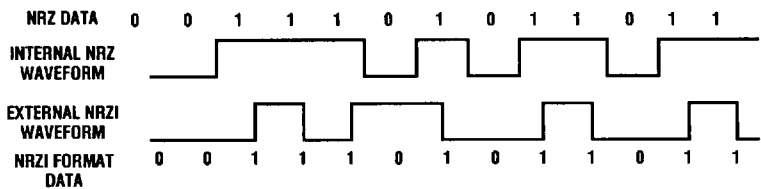
Transmitter Sequence:

1. 40-bit parallel input
2. 4b/5b encoding
3. 50-baud parallel-frame-to-serial conversion
4. NRZ-to-NRZI conversion
5. Serial output

Receiver Sequence:

1. Clock and data recovery from serial input
2. NRZI-to-NRZ conversion
3. Serial-to-parallel (50-baud) conversion
4. 5b/4b decoding
5. 40-bit parallel output

Figure 2. NRZ to NRZI Conversion



Transmitter Sequence Details:

1. A 40-bit TTL-level parallel word is input to the transmitter.
2. The 40-bit input word is encoded into a 50-baud frame using FDDI standard 4b/5b encoding. In this encoding, 4-bit data nibbles are translated into a 5-baud code symbol according to Table 1. The 4b/5b encoding produces ten 5-baud symbols from ten 4-bit data nibbles.
3. The 50-baud parallel frame representation is converted to a serial string 50 bauds in length.
4. At this point, the serial bauds are in standard NRZ (Non-Return-to-Zero) format: a low voltage level represents a logic LOW and a high voltage level represents a logic HIGH. This NRZ serial stream is converted to an NRZI (Non-Return-to-Zero, Invert-on-ones) format. Instead of representing 1s and 0s by voltage levels, NRZI coding represents them by transitions or lack thereof. In NRZI, a HIGH-LOW or LOW-HIGH transition represents a logic one, while a LOW-LOW or HIGH-HIGH transition represents a logic zero (Figure 2).

The combination of 4b/5b encoding and NRZI data formatting provide two benefits to system operation. First, it guarantees frequent transitions on the

transmitter's serial output. No more than three consecutive non-transitions (0s) can occur sequentially. These frequent transitions on the incoming differential input stream aid the receiver's PLL (Phase-Locked Loop) circuitry in maintaining synchronization with the transmitter. Secondly, this format guarantees a worst case 60%/40% duty cycle. This is important for fiber-optic media in that it limits the DC offset voltage of the transmitter's serial outputs.

5. The NRZI format serial stream is transmitted to the receiver on a differential positive-referenced ECL (PECL) signal pair.

PECL interfaces use ECL logic levels referenced to +5 V. This eliminates the need for additional power supplies.

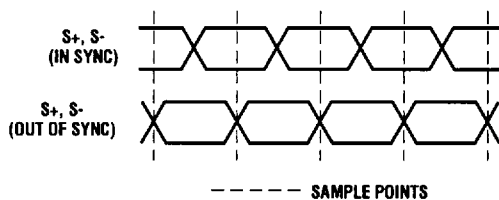
Receiver Sequence Details:

1. The receiver recovers the clock and data information from the incoming serial stream. The serial data is in NRZI format.
2. The NRZI data is converted back to NRZ format. The sequence of logic transitions representing 1s and 0s is converted to voltage levels representing 1s and 0s.
3. The resulting baud stream is assembled in 50-baud frames and passed to the 5b/4b decode circuitry.

4. The 50-baud frames are broken down into ten 5-baud symbols. Each symbol is decoded to a 4-bit data nibble according to Table 1. The ten 4-bit nibbles are assembled to recreate the original 40-bit data word.
5. The resulting 40-bit parallel word is output on a TTL-level bus.

Table 1. 4b/5b Translation

	4-Bit Binary Input Data	Hex Data	5-Baud Symbol Output
Data:	0000	0	11110
	0001	1	01001
	0010	2	10100
	0011	3	10101
	0100	4	01010
	0101	5	01011
	0110	6	01110
	0111	7	01111
	1000	8	10010
	1001	9	10011
	1010	A	10110
	1011	B	10111
	1100	C	11010
	1101	D	11011
	1110	E	11100
	1111	F	11101
Sync	Idle	n/a	11111
Symbols:	Sync J	n/a	11000
	Sync K	n/a	10001

Figure 3. Baud Sampling**Invalid Symbols**

Noise and jitter on the serial link can cause one or more bauds to be corrupted. This can alter the 5b symbol being transmitted. Table 1 lists all of the valid 5-baud symbols. The thirteen unlisted 5b symbols are all considered invalid. The receiver monitors incoming 5b symbols for validity. If an invalid symbol is detected, the receiver will recognize the symbol(s) in error and assert the ERROR signal HIGH. The invalid symbols are arbitrarily decoded into data nibble "1111". (See also the Strobe and Status Generate portion of the Receiver Functional Description).

Synchronous and Asynchronous Protocols

Hot Rod uses a synchronous transmission protocol. A synchronous transmission system continuously transmits information over the serial link, allowing the receiver to

maintain synchronization to the transmitter at all times. In an asynchronous protocol (such as RS-232), data is not continuously transmitted; accordingly the receiver must re-establish synchronization at the start of each data word. Because synchronous protocols eliminate the delay associated with re-acquiring sync on each word, they can yield a higher effective data rate across a given serial media.

Synchronization

As part of its synchronous protocol, the Hot Rod transmitter will continuously send data whenever data is available. If parallel words are not input to the transmitter, sync frames are sent across the serial link. A sync frame is not data; rather it is a predetermined 50-baud string sent to maintain sync. Sync frames are continuously sent until new data is loaded into the transmitter. This ensures a

continuous signal to the receiver. The receiver discards sync frames as they are received; only data frames are kept and passed through to the output bus.

The receiver must be synchronized to the incoming data at both the baud and frame levels. Baud level synchronization is required so the receiver may sample the incoming signal at the midpoint of the baud, and not at the transition between bauds (Figure 3). Frame level synchronization ensures the receiver is frame aligned with the transmitter. If the receiver's frame is misaligned with the transmitter's frame, the incoming signal will be misinterpreted (Figure 4).

Acquiring and Maintaining Sync

If the receiver loses sync due to media noise or other causes, or is out of sync due to a system power-up or reset, the receiver must first acquire baud synchronization and then frame synchronization. Baud sync can be obtained while receiving any sequence of data and/or sync frames, and occurs in the length of time specified by parameter T_{79} specified in the AC Specification section of this datasheet.

For the receiver to acquire or re-acquire frame synchronization, one sync frame must be received after baud synchronization is obtained. Frame synchronization cannot be acquired from a data frame; data frames contain no information indicating the beginning or end of a frame. A sync frame consists of eight Idle symbols, followed by a Sync J and a Sync K (Figure 5). Because a sync frame is fully predefined, it can be used by

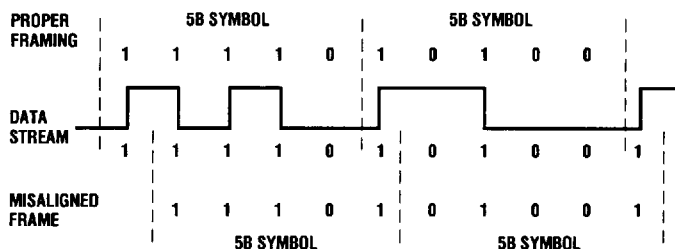
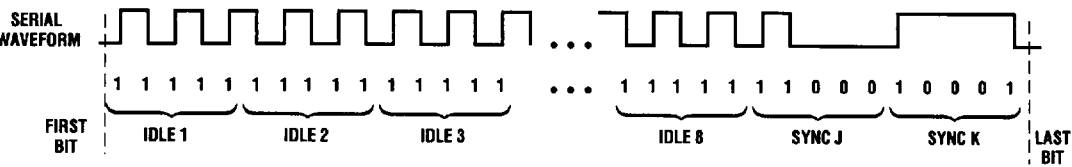
Figure 4. Misalignment

Figure 5. Sync Frame



the receiver to establish the proper frame boundaries.

To ensure a sync frame is received after baud synchronization is obtained, system designs must have the capability of forcing sync frames to be transmitted either a) on an ongoing periodic basis, or b) when the receiver has lost frame synchronization.

Since the Hot Rod transmitter will automatically transmit sync frames when no data is available, approach a) can be achieved by feeding data to the transmitter at a slightly lower rate than the maximum word rate. For example, if the word rate is 20 MHz, and data words are loaded into the transmitter at 18 MHz, one sync frame will be sent for every nine data frames.

Alternatively, when bidirectional links are used, a handshaking protocol can be used to guarantee sync frame transmission whenever either receiver loses synchronization (alternative b above). Care must be taken to ensure that the handshaking protocol allows for proper sequencing after a reset, or in the event both directions of the link lose frame synchronization.

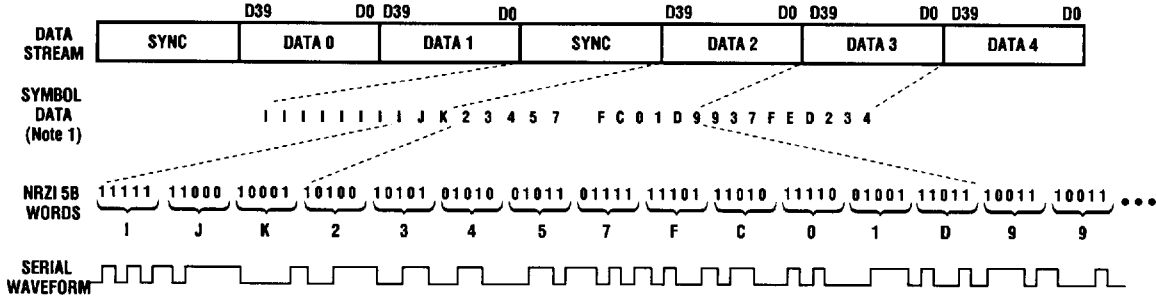
Data and Sync Frames

Serial transmissions are sent in 50-baud frames; they are either 50-baud data frames or 50-baud sync frames. A sync frame is defined as shown in Figure 5. If any of the sync symbols appear outside of this sync frame format, the ERROR signal will be asserted. Once the transmitter has started sending a sync frame, the entire

50-baud frame will be transmitted regardless of the availability of new data in the transmitter. A data frame consists of ten 5-baud symbols, each one corresponding to a 4-bit data nibble of the parallel word. The Most Significant Symbol (MSS), corresponding to data nibble D39..D36, is transmitted first. The symbol corresponding to D35..D32 is sent next. This procedure continues until the Least Significant Symbol (corresponding to D3..D0) is sent.

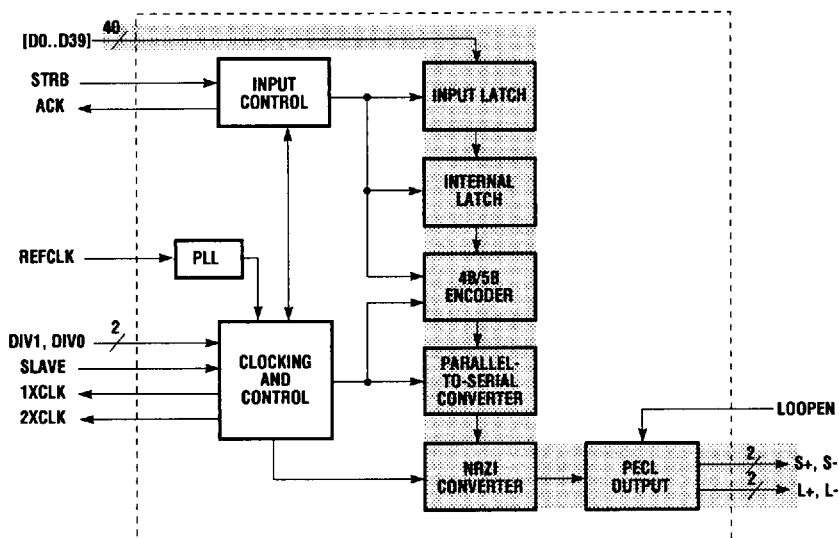
A sample transmission sequence is shown in Figure 6. Parallel word Data2 [D39..D0] = 23457FC01D (Hex). The most significant data nibble is 0010. The 4b/5b symbol is 10100. This is the MSS and is transmitted first. Within the symbol, the bauds are transmitted from most significant baud to least significant baud, so the transmitted bauds will be 1, then 0, then 1, then 0 and 0.

Figure 6. Sample Transmission



NOTE 1: 1 = IDLE
J = SYNC J
K = SYNC K
0..F = HEX DATA } REFER TO TABLE 3 (4B/5B ENCODING)

Figure 7. Hot Rod Transmitter Functional Block Diagram



Transmitter Functional Description

As outlined in the Communications Protocol section, the transmitter accepts a 40-bit word, encodes it into a 50-baud symbol (using 4b/5b coding), converts it to a serial stream, performs an NRZ-to-NRZI conversion, and outputs the data across a serial PECL (positive-referenced ECL) interface. This process occurs in the data path highlighted in blue in Figure 7. The control circuits employed to oversee this function are described below.

Phase-Locked Loop (PLL)

The PLL multiplies the REFCLK input signal by a factor of fifty. The output of the PLL provides the timing reference for all internal clocking and control operations. Figure 8 shows a block diagram of the PLL Circuit.

Clocking and Control

The clocking and control circuitry sets the frequency of operation and controls sync frame insertion.

The Hot Rod transmitter has four selectable speed ranges; these are determined from the frequency of REFCLK and the value of

the DIV1 and DIV0 pins. A proper frequency REFCLK signal should be used with the appropriate values of the DIV pins for the desired data rates and speed grades of the devices as specified in Table 2. The DIV pins provide a divide function for selecting data rates. The Baud Rate is 25% greater than the maximum Bit Data Rate due to the 4b/5b encoding used.

Figure 8. PLL Circuit

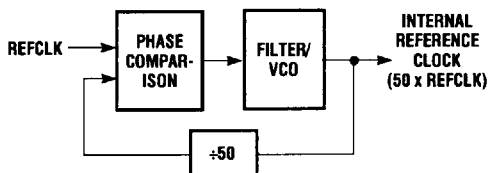


Table 2. Data Rates

GA9011/GA9012-2, 200 Mbit/sec

Max. Speed	DIV 1	DIV 0	Data Rate (Megawords/sec) (Megabits/sec)		Baud Rate (Megabaud/sec)	REFCLK (MHz)
200 Mb/s	1	1		*		
	1	0		*		
	0	1	5.0	200	250	20
	0	0		*		

*Not allowed

GA9011/GA9012-4, 400 Mbit/sec

Max. Speed	DIV 1	DIV 0	Data Rate (Megawords/sec) (Megabits/sec)		Baud Rate (Megabaud/sec)	REFCLK (MHz)
400 Mb/s	1	1		*		
	1	0	10.0	400	500	20
	0	1	5.0	200	250	20
	0	0		*		

*Not allowed

GA9011/GA9012-5, 500 Mbit/sec

Max. Speed	DIV 1	DIV 0	Data Rate (Megawords/sec) (Megabits/sec)		Baud Rate (Megabaud/sec)	REFCLK (MHz)
500 Mb/s	1	1		*		
	1	0	10.0 - 12.5	400 - 500	500 - 625	20 - 25
	0	1	5.0 - 6.25	200 - 250	250 - 312.5	20 - 25
	0	0		*		

*Not allowed

GA9011/GA9012-8, 800 Mbit/sec

Max. Speed	DIV 1	DIV 0	Data Rate (Megawords/sec) (Megabits/sec)		Baud Rate (Megabaud/sec)	REFCLK (MHz)
800 Mb/s	1	1	20.0	800	1000	20
	1	0	10.0	400	500	20
	0	1	5.0	200	250	20
	0	0		*		

*Not allowed

NOTE: Line rate in Megabaud/s = 1.25 * Data Rate in Megabits/s.

The control circuitry inserts a sync frame into the data path whenever there are no data words to send. It continues to do so until new data is strobed in and passed to the serial output.

Input Control

The Input Control handles the input and clocking of the data through the front end of the transmitter. Input data (D0..D39) are latched into the transmitter on the rising edge of the STRB signal.

For most system designers, a key objective is to achieve maximum Hot Rod data throughput without overrunning the transmitter's speed.

The transmitter device is designed to allow broad system design flexibility by providing five distinct ways of clocking data into the transmitter:

1. Asynchronous STRB/ACK handshake (edge-driven)
2. Asynchronous STRB/ACK handshake (level-driven)
3. Synchronous to 1XCLK
4. Synchronous to 2XCLK
5. Free-running STRB

The handshake format should be selected to fit the host system.

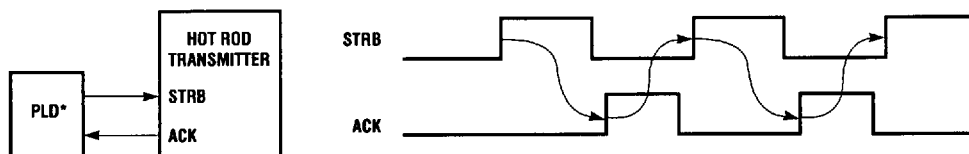
1. Asynchronous Edge-Driven STRB/ACK handshake (Figure 9)

Data may be asynchronously loaded using solely the STRB/ACK protocol. A rising edge on STRB latches the data into the transmitter. STRB can be brought LOW after the minimum pulse width has been

satisfied. When the transmitter becomes available for the next data word, it indicates this by a rising edge on ACK. ACK will fall subsequent to STRB falling. Once the rising edge of the ACK pulse is detected, a new STRB rising edge can be applied.

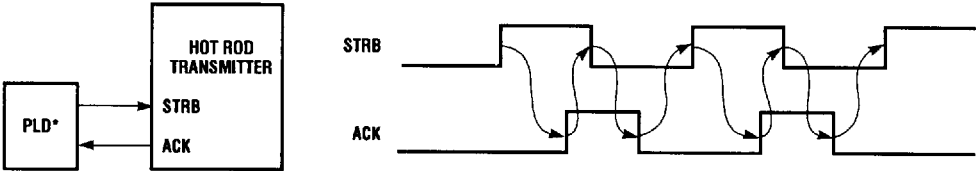
If the user wants to insert occasional sync frames, this feature could be incorporated in the logic generating STRB simply by providing STRBs at a rate lower than the transmitter word rate.

Figure 9. Edge-Driven Handshake



**TriQuint GA22V10 recommended*

Figure 10. Level-Driven Handshake



2. Asynchronous Level-Driven STRB/ACK handshake (Figure 10)

Alternatively, the handshake may be level-driven. STRB is brought HIGH to clock in data. Subsequently, ACK rises, indicating the transmitter is ready for another data word. STRB is then driven LOW; ACK will then fall. STRB is then driven HIGH, and the new data is input. In response, ACK rises and the procedure continues.

3. Synchronous to 1XCLK (Figure 11)

The Hot Rod chipset may be operated synchronously to data word transmission. The transmitter provides a synchronous 1XCLK (frequency = 1 X word rate) and 2XCLK (frequency = 2 X word rate) to drive host system logic. Figure 11 shows a synchronous implementation using the 1XCLK to strobe the transmitter. Since the 1XCLK is synchronous to word transmission, this configuration allows the maximum possible data rate to be achieved whenever STRB rises within T_{10}

of 1XCLK falling. The falling edge (1XCLK) is inverted to drive the STRB signal.

By gating 1XCLK to STRB, sync frames may be inserted in the transmission stream by occasionally disabling STRB through the SYNC-INSERT signal.

4. Synchronous to 2XCLK (Figure 12)

The block diagram and waveforms for synchronous operation using both the 1XCLK and 2XCLK are shown in Figure 12. This implementation widens the window available in Figure 11 for maximum data rate transmission (from T_{10} above to $T_{16} + T_{10}$).

Figure 11. Synchronous to 1XCLK

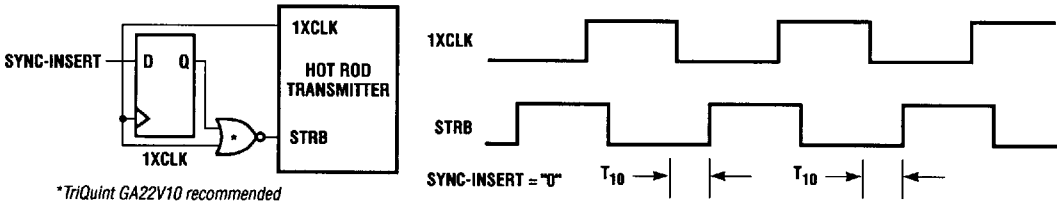


Figure 12. Synchronous to 2XCLK

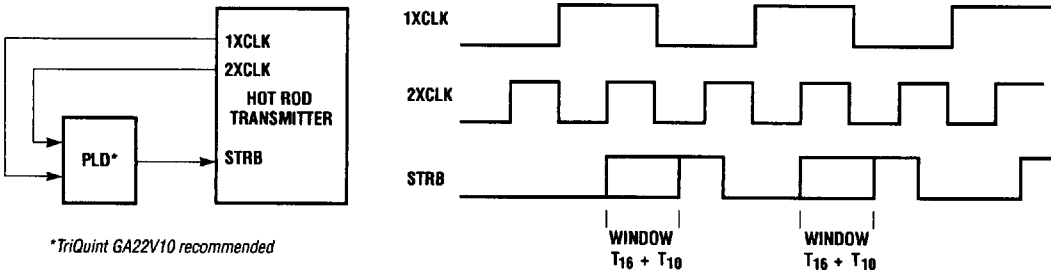
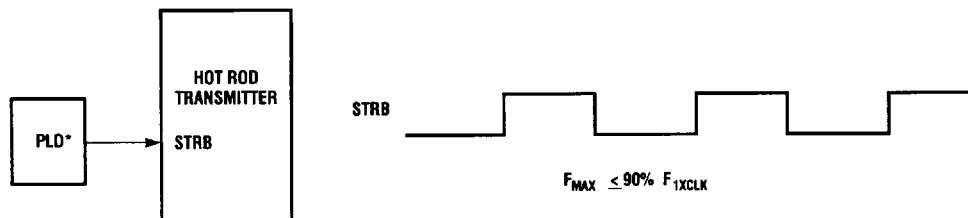


Figure 13. Free-running STRB

*TriQuint GA22V10 recommended

The rising edge of the 2XCLK samples the 1XCLK. If it is high, the STRB signal should be brought high. STRB can rise at any time between 2XCLK rising and T_{10} after 2XCLK falls. This will ensure continuous data transmission can be obtained at the maximum data rate. The capability to suspend data strobing should be added if sync frames are desired.

5. Free-running STRB (Figure 13)

This option offers a trade-off of reduced throughput for ease of interface design. Data may be clocked into the transmitter using a free-running clock on the STRB input. The ACK signal is completely ignored. New data is latched into the transmitter on each STRB rising edge. The free-running STRB is limited to a frequency 90% or less of that of the 1XCLK. The 1XCLK frequency is the maximum word rate frequency using handshaking. The 90% limit arises only when ACK is ignored. This ensures that a data word will never be missed (i.e. the transmitter input latch will be able to accept data on each STRB rising edge).

Since data words are being loaded at 9/10 (or less) the rate at which they are being

serially transmitted, sync frames will be inserted, on the average, every ten frames.

While this input design requires very low overhead, it limits the system to 90% of the maximum possible data rate.

PECL Output

The PECL Output has two serial output interfaces. The S+/S- (Serial) interface is used for serial transmission to a target Hot Rod receiver. The L+/L- (Loopback) interface is intended for system diagnostics. The interface over which transmission occurs is selected by the LOOPEN pin. With LOOPEN LOW, standard transmission over the serial (S+, S-) pins occurs. When LOOPEN is asserted HIGH, output is routed over the

loopback outputs (L+, L-). The de-selected outputs are driven to a fixed state, with S- (or L-) pulled HIGH, and S+ (or L+) pulled LOW through the termination resistors.

The PECL (positive-referenced ECL) interface provides ECL levels referenced to +5 V. It requires +5 V and GND power supplies only. A nominal logic HIGH is 4.2 V and nominal low is 3.2 V. The output stage consists only of an active pullup. As shown in Figures 14 and 15, a passive pulldown resistor (50 Ohms tied to $V_{CC} - 2\text{ V}$, or a Thevenin equivalent circuit to +5 V and GND) must be used.

The loopback feature is described in detail in Operational Configurations — Loopback Mode.

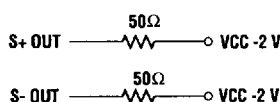
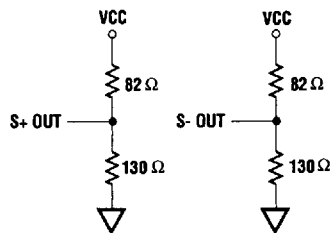
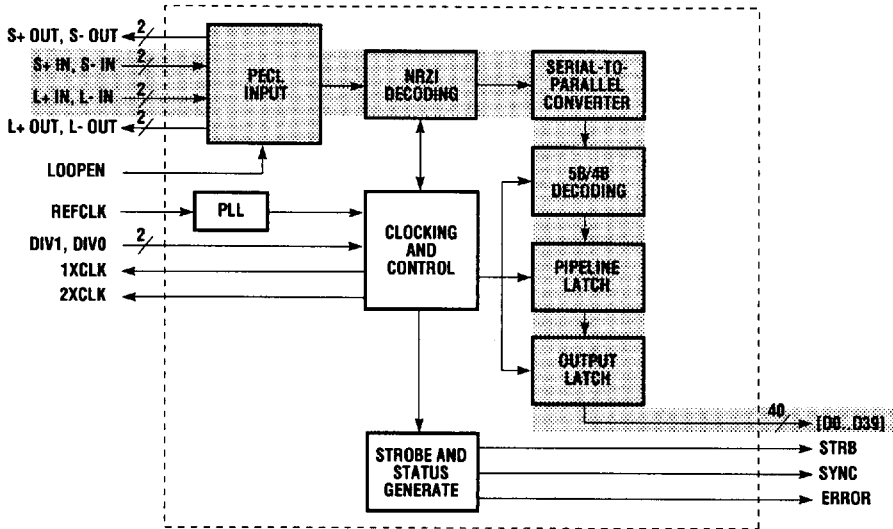
Figure 14. Suggested Serial Termination**Figure 15. Suggested Parallel Termination**

Figure 16. Hot Rod Receiver Functional Block Diagram



Receiver Functional Description

The receiver performs the inverse function of the transmitter (see Figure 16). It accepts a serial, differential, PECL-level signal, recovers clock and data, performs an NRZI-to-NRZ conversion, translates the resulting 5b symbols to 4b data, assembles the 40-bit parallel word and outputs it to the host system. The execution of this progression is described below.

PECL Input

The PECL (positive-referenced ECL) Input accepts data from one of two input lines and offers continuations of those signals to ease termination requirements.

The PECL Input is a multiplexer which accepts serial, differential data on either the

S+ In, S- In (Serial) input lines or the L+ In, L- In (Loopback) lines. The serial lines are selected by LOOPEN being LOW; the loopback lines are selected by LOOPEN being HIGH.

The Hot Rod serial link uses high-speed differential signals which require careful

termination. Typically, these signals would need to be terminated beside the package. This causes a great deal of restriction in circuit board layout. Continuation outputs of the serial inputs allow for Fly-By™ termination (Figure 17). This allows the device to sample the incoming signal before it is routed to termination. The

Figure 17. Fly-by™ Terminations

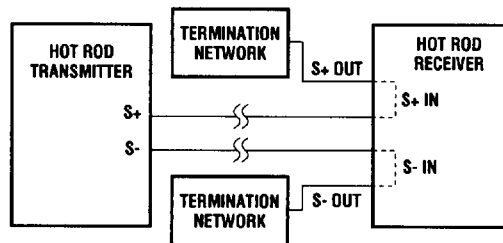
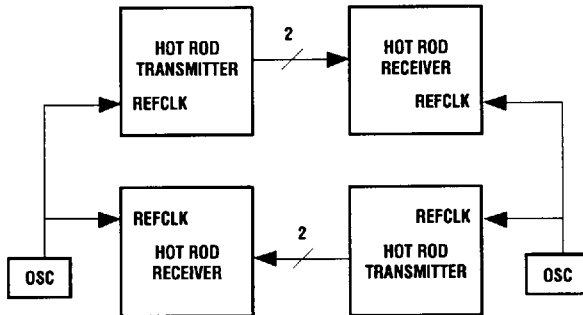


Figure 18. Using the External Clock in Bidirectional Mode

continuations, rather than the input signals, may then be routed to a convenient location on the board for termination. The Hot Rod receiver is designed for 50-Ohm traces, and suggested termination schemes for the PECL differential signals (both serial and loopback) are shown in Figures 14 and 15.

Phase-Locked Loop (PLL)

This is a duplicate of the PLL circuit on the transmitter; it multiplies the input REFCLK by a factor of 50 to generate the timing reference signal for Hot Rod receiver operation. This multiplied signal provides

the reference for extracting clock and data information from the incoming signal.

The REFCLK signal must be driven from a host system. In a bidirectional application, the REFCLK on the transmitter and the receiver can be driven by the same external signal (Figure 18).

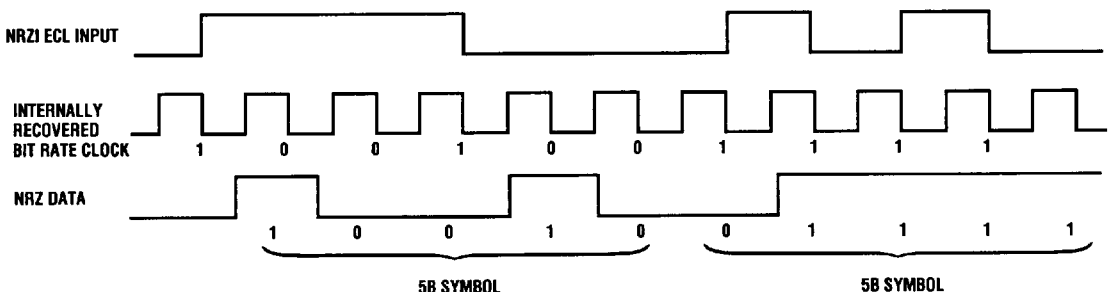
Clocking and Control

The clocking and control section coordinates the construction of the 40-bit parallel data word from the 50-baud serial code word.

Before any data can be read, synchronization must be acquired. (Refer to Communications Protocol.) The receiver must be configured so the reception rate will match the transmission rate of the corresponding transmitter. This is done by providing a REFCLK with the same nominal frequency as the transmitter and setting the DIV pins on the receiver to the same configuration as the transmitter. Table 2 lists the various speeds and configurations for both transmitter and receiver.

Once baud and frame level synchronization are achieved, data information can be recovered from the serial input stream. As data are recovered, they are serially converted back to NRZ format (Figure 19) and grouped in 50-baud frames (ten 5b symbols).

A 50-baud frame can be a sync frame or a data frame. If a sync frame (see Figure 7) is detected, it is discarded and the SYNC signal asserted. SYNC may be sampled synchronously on the rising edge of the 1XCLK. The last data word received (previous to one or more SYNC frames) remains on the output bus D0..D39.

Figure 19. NRZI-to-NRZ Conversion

If a data frame is received, the 5b/4b decoding yields a 40-bit data word which is output on D0..D39. The appearance of new data on D0..D39 is signified by a STRB rising edge.

Within a 50-baud frame, one or more of the ten 5b symbols could be invalid due to a disruption on the media. If so, the invalid 5b symbol(s) decode(s) to an all-HIGH (i.e. "1111") 4-bit data nibble. If one or more invalid 5b symbols are decoded, the ERROR signal is asserted HIGH. For example, if only the first 5b symbol in a frame was invalid, the four Most Significant Bits of the output bus would be "1111," and all other bits in the output data word would carry valid data. The ERROR flag would be HIGH, indicating the presence of one or more erroneous 4-bit data nibbles. Any of the three SYNC symbols, if received in a data frame, are decoded as invalid symbols.

Table 3. Output/Receiver Status

STRB	Error	Sync	Condition
↑	Low	Low	Good data received. Highly probable receiver is in sync.
↑	High	Low	Received bad nibbles. Possible receiver is out of sync.
No Edge	Low or High	High	Sync frame received. Receiver is in sync.

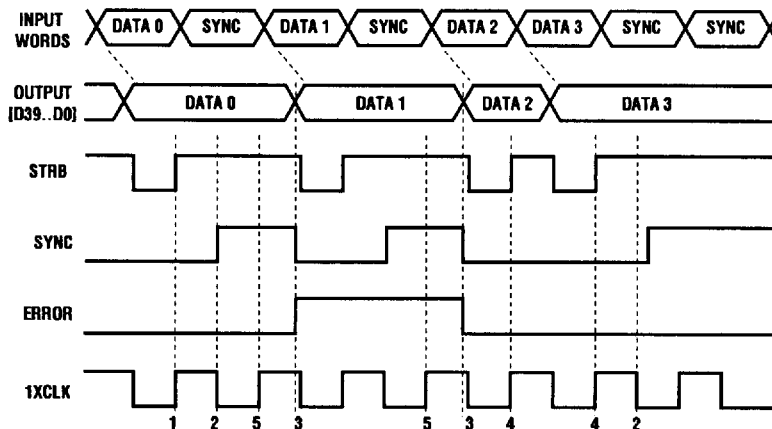
Strobe and Status Generate

This circuitry generates the user interface status signals STRB, SYNC, and ERROR. STRB pulses LOW and the rising edge indicates when a new data word is output on D0..D39. SYNC goes HIGH to indicate the receipt of a sync frame. ERROR is asserted HIGH when the current output word was decoded from one or more invalid 5b symbols. It remains HIGH until a new data word (decoded from ten valid 5b

symbols) is written to the output bus. Table 3 lists the possible signal combinations and their interpretation.

Figure 20 shows sample output waveforms. STRB rising (marker 1) indicates new data (Data 0, in this case) is available on the output bus. When a sync frame is received (marker 2), SYNC is asserted HIGH and will remain HIGH until a data frame is received (marker 3). It is sampled with the 1XCLK at marker 5.

Figure 20. Sample Output Waveforms



Marker number 3 also delineates the ERROR active-HIGH pulse. This implies Data 1 has at least one nibble (set to "1111") in error. ERROR rises and falls coincident with the output data word to which it corresponds. Marker 4 indicates the operation of STRB during continuous data frame transmission; in this case, STRB will be a 50% duty-cycle signal. Each rising edge indicates new data has been written to the output bus D0..D39.

As the Hot Rod receiver receives new data on the serial link, it writes parallel words to the output bus. The host system must capture this information before a new data word is written. Since a rising edge on STRB indicates new data on the output bus, it could be used to clock the output data into a latch, register, or other device. One possible implementation is to clock data into a FIFO. The STRB signal could provide the clocking signal for D0..D39 (Figure 21). The ERROR bit should also be clocked in and later examined to determine the validity of the output data word. No additional external circuitry is required.

Figure 22 offers a similar solution that can operate with slower FIFOs and faster word rates. This design allows the STRB signal to be shaped to better interface with high-performance FIFO devices. The 2XCLK, which is synchronous to STRB, shapes the STRB waveform (typically 50/50 duty cycle) to provide a longer LOW pulse. This better matches industry-standard FIFO T_{WPW} (Write Pulse Width) and T_{WR} (Write Recovery) specifications.

Figure 21. Interfacing the Hot Rod Receiver

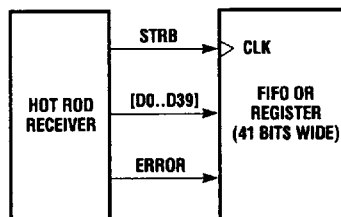
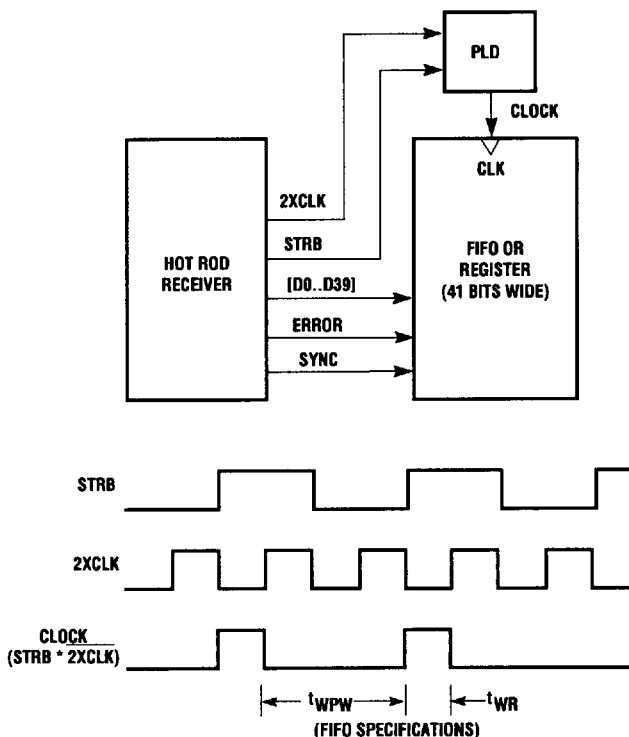


Figure 22. Writing to a FIFO from the Hot Rod Receiver



Operational Configurations

This section presents the basic configurations for using the Hot Rod chipset. They consist of:

1. Bidirectional Mode
2. Unidirectional Mode
3. Parallel Mode
4. Loopback Mode

Bidirectional communications employs two Hot Rod chip sets, each communicating in opposite directions across separate serial links. The

unidirectional mode uses one chipset in one direction only. Parallel operation is achieved through multiple chipsets operating over parallel links communicating in the same direction. Loopback mode is a system diagnostic feature that can be employed in bidirectional applications. By combining the configuration information in this section with the interfacing recommendations made earlier, an entire Hot Rod sub-system can be designed.

Bidirectional Mode

Figure 23 presents the basic layout of a bidirectional Hot Rod communications system.

The nominal frequency of the REFCLK signals for both System A and System B must match, as must the value on the DIV pins (not shown).

The system loopback line controls the loopback mode function, described below in Loopback Mode (4).

Figure 23. Bidirectional Configuration

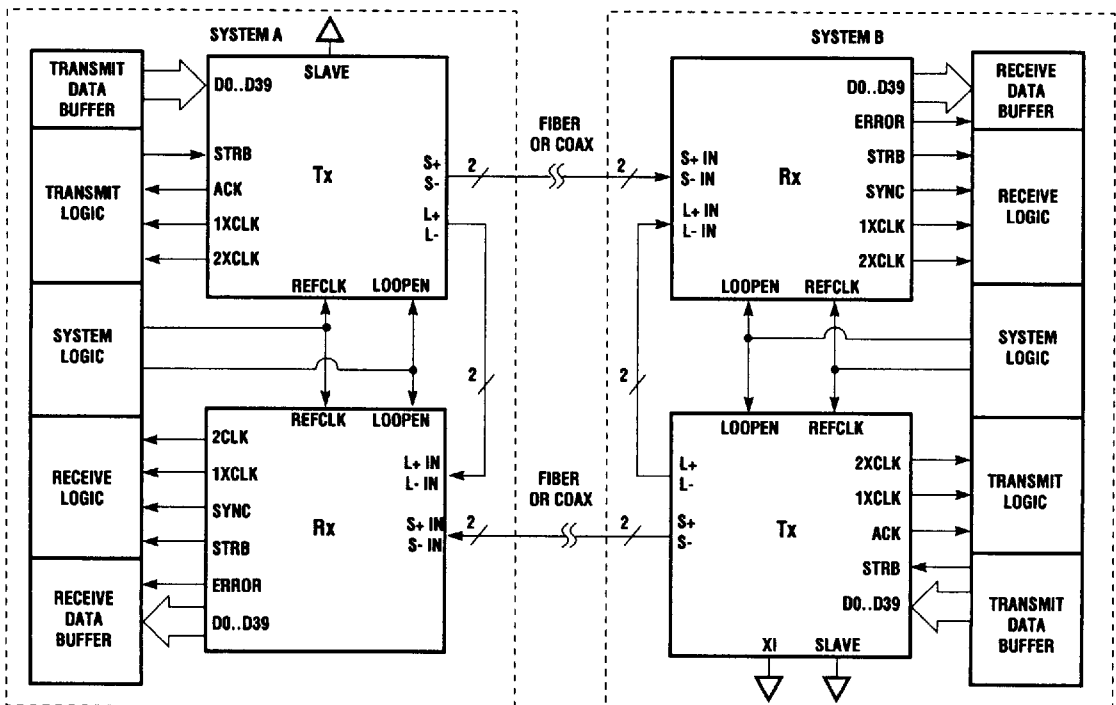
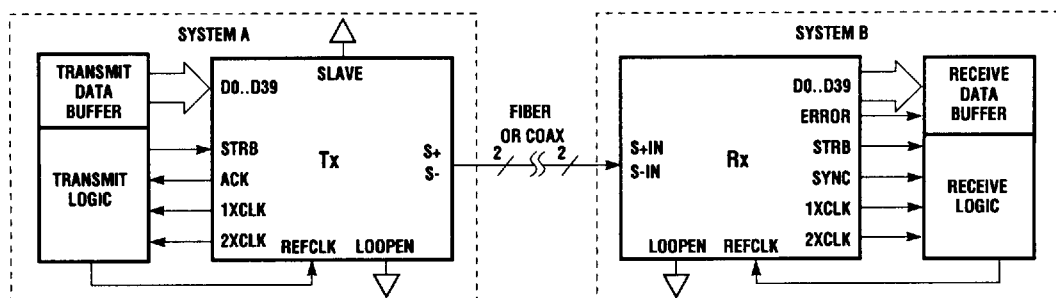


Figure 24. Unidirectional Configuration



Unidirectional Mode

Figure 24 shows a typical unidirectional configuration.

The transmitter and the receiver must receive REFCLK from a host system signal. The frequency of REFCLK and the value of the DIV pins (not shown) must match in order for the transmission rate to equal the reception rate.

The LOOPEN pin is tied to GND; this selects the serial (S+, S-) outputs on the transmitter and the serial (S+, S-) inputs on the receiver. All other system interfacing requirements mirror those of the bidirectional configuration.

Parallel Mode

Parallel mode, in which multiple Gbit/sec throughput can be achieved, is illustrated in Figure 25. The transmitter devices are not cascaded; rather they are run synchronously in parallel. Each Hot Rod chip set requires its own serial link and is individually capable of 1 Gbit/sec data throughput.

For all transmitters to send data synchronously, one transmitter is selected

as the master device and the rest as slave devices. The SLAVE pin on the master is tied to GND. The master's 1XCLK signal drives the SLAVE pins on the slave devices. Because 1XCLK is aligned to frame transmission, it will allow each slave transmitter to align its frame boundaries to those of the master transmitter. All chips should receive the same REFCLK signal, and the DIV pins on all devices must also be configured similarly.

If DIV1 = DIV0 = HIGH, the function of the SLAVE pin is not required because the REFCLK frequency is the actual word rate. When the word rate is divided (using the DIV pins), the SLAVE pin ensures phase alignment across parallel transmitters. If, for example, DIV1 is LOW and DIV0 is HIGH, the word rate is one-fourth the REFCLK frequency, implying four possible frame boundary locations. The SLAVE pin guarantees all transmitters will use the same one (of four).

Figure 25. Parallel "Pseudo-Cascade" Mode

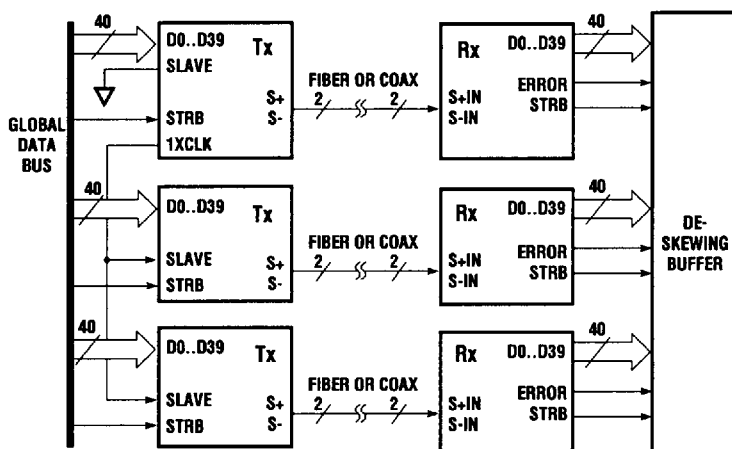
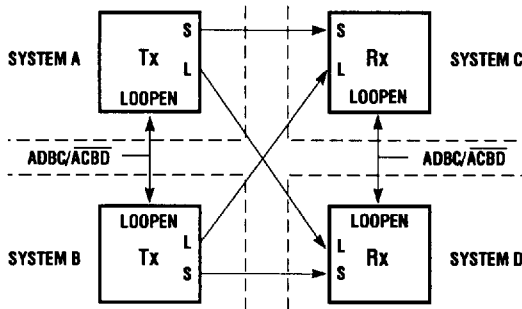


Figure 26. Loopback Mode Used as Switch Capability

There is no master/slave feature in the receiver; the data words are read as they arrive. To recreate the 80- or 120-bit (or greater) word, a deskewing buffer may be used. This will eliminate any minor skew introduced through variations in devices, layout, or serial media.

Loopback Mode

The Loopback Mode is intended to provide a system test capability at speed. Figure 23 (see page 17) shows a bidirectional system with a loopback capability in place. During normal transmission, LOOPEN is disabled LOW and data is transmitted over the serial (S+, S-) lines. By asserting LOOPEN HIGH on the transmitter, the S+, S- outputs are disabled, and the serial data is transmitted over L+, L- to a local Hot Rod receiver. LOOPEN HIGH on the receiver causes it to read from the loopback (L+ In, L- In) signals instead of from the S+ In, S- In signals. This allows local board testing independent of a fiber-optic or coaxial link.

Loopback Used for Switching

Since the serial and loopback signals are functionally identical on both the transmitter and receiver, it is possible to use the loopback capability as a switch or

multiplexer. A basic system using this feature is shown in Figure 26. The switching is controlled by ADBC/(ACBD)'. When LOW, transmission and reception occurs from system A to system C and system B to system D. When HIGH, system A transmits to system D while system B transmits to system C.

Whenever the LOOPEN signal is switched, a new transmitter/receiver link has been established. Initially, this chip set pair will not be in sync. A delay time (T_{79}) must be allowed for baud and frame level synchronization to be acquired on the new link. This synchronization acquisition time should be considered in system designs using the loopback feature.

System Considerations

This section covers some of the system-level issues facing the designer of a Hot Rod system including:

1. Calculation of effective data rate
2. Latency from input to output
3. Error coverage and recommendations
4. Behavior at power-up
5. Receiver synchronization
6. Typical configuration for guaranteed data integrity

Calculation of Effective Data Rate

The effective user data rate of a Hot Rod chip set pair is easily calculated from the frequency of REFCLK, the value of the DIV pins, and the ratio of data frames to sync frames.

REFCLK provides the reference frequency for frame transmissions. The DIV pins can be set to divide the frame transmission by 1, 2, or 4, according to Table 4. The result is the actual frame rate.

Table 4. Effect of DIV Pins on Data Rate

DIV1	DIV0	Divisor
0	1	4
1	0	2
1	1	1 (Maximum rate)

Frames can be data frames or sync frames. Each data frame carries 50 bauds, which is an encoded version of 40 data bits. If data frames are continually transmitted (without sync frames), the effective data rate will be the frame rate times 40 bits. Whenever a percentage of the transmitted frames are sync frames, the effective data rate is lowered by that percentage.

Example 1:

REFCLK = 25 MHz, DIV1 = 1, DIV0 = 0

$25 \text{ MHz} \times 40 \text{ data bits/word} =$
 $1 \text{ Gbit/sec}/2 = 500 \text{ Mbit/sec}$

500 Mbit/sec is the user data rate.

If one sync frame is inserted every 10 frames, the data rate is reduced by 10% to 450 Mbit/sec.

Example 2:

REFCLK = 20 MHz, DIV1 = DIV0 = 1

$20 \text{ MHz} \times 40 \text{ data bits/word} =$
 800 Mbit/sec

800 Mbit/sec is the effective data rate.

If one sync frame is inserted every 8,000 frames, the user data rate is 799.98 Mbit/sec.

Latency from Input to Output

The latency from the transmitter input to the receiver output is the sum of the input-to-output latency in the transmitter (T_{31}), the delay across the serial media, and the input-to-output latency of the receiver (T_{78}).

The on-chip latency is a result of the pipelined structure of the data path. The synchronous nature of the transmitter causes a wide spread between the minimum and maximum values of its internal latency (T_{31}). If the input words are loaded synchronously, latency through the transmitter can be minimized.

On the receiver, data input is synchronized on-chip. The latency through the receiver is solely a function of the clocking of data through the pipelined data path.

Error Detection

The 4b/5b coding is chosen for its frequent transitions and tightly bound duty cycle, not to provide an error-checking capability. While the Hot Rod receiver will detect invalid 5b symbols in the input stream, this does not provide exhaustive error coverage. It is possible for errors on the media to translate one valid 5b symbol

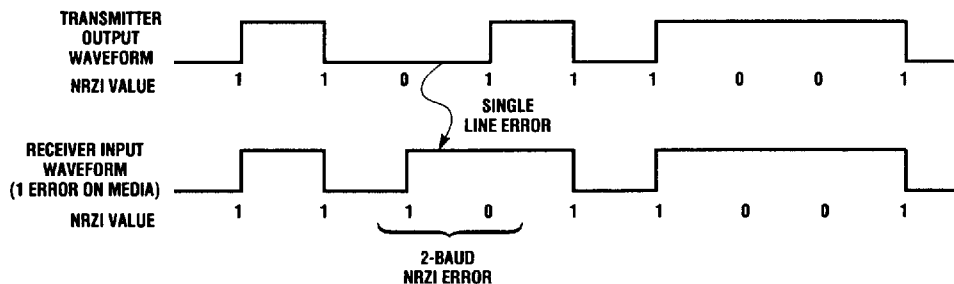
into another valid 5b symbol. In this case, the error will go undetected.

Noise on the serial media will likely be the primary cause for errors during transmission. Because the data are NRZI-formatted, a single error on the line (i.e. the line level being HIGH when it should be LOW, or vice-versa) creates a corresponding double-baud error in the NRZI data (Figure 27). The double-baud error can occur within a 5-baud symbol, or it could affect the last baud of one symbol and the first baud of the following symbol. Any error-checking scheme employed by the user should consider a predominant fault mechanism to be sequential, double-bit errors.

Behavior at Power-Up

Upon power-up of the Hot Rod transmitter and receiver devices, baud and frame synchronization must be established. Once baud sync is acquired, the receiver needs one sync frame to acquire frame sync. To avoid unnecessary switching during sync acquisition, the receiver is designed to "lock" the power-up values of D0..D39, ERROR, and STRB. When SYNC goes HIGH, at least one sync frame has been received, and the synchronous link has

Figure 27. Single Baud Error on Media Creates Sequential Double-Baud NRZI Error



been established. Once sync is established, DO..D39, ERROR and STRB will be "unlocked" and they will switch according to the serial input being received.

The receiver depends on at least one sync frame for sync acquisition. The power-up control of the transmitter must ensure at least one sync frame is transmitted after the receiver acquires baud synchronization. The receiver is specified to acquire baud sync after receiving sync or data frames for time T_{79} .

Receiver Synchronization

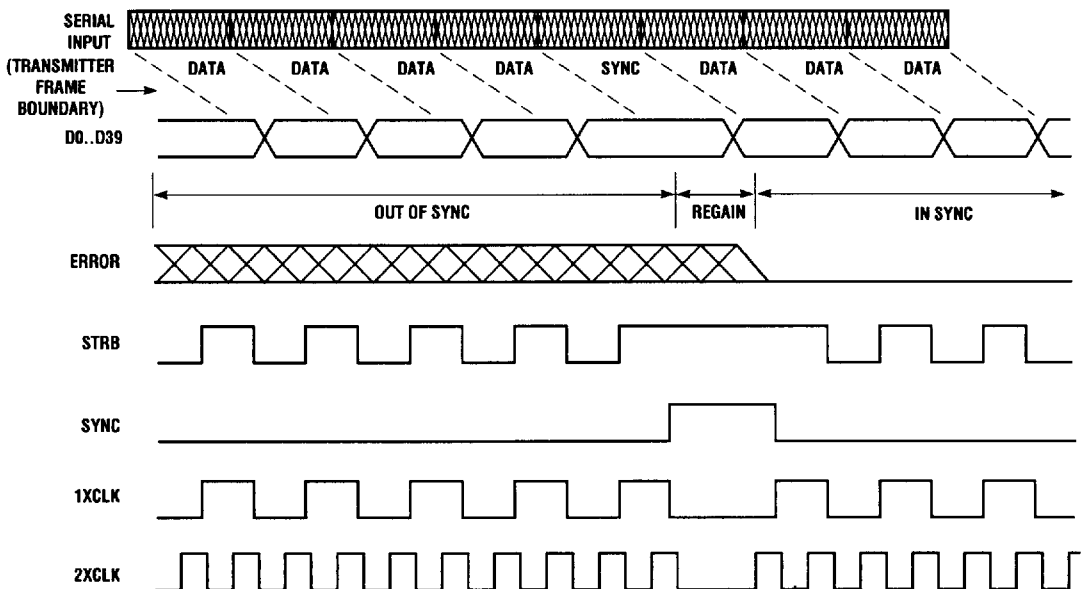
It is possible for the receiver to lose synchronization to the serial signal. This

occurs at: 1) power-up, 2) when the line is too noisy, 3) when the line is broken, 4) if the transmitter is no longer transmitting on that line (transmitter LOOPEN was switched), or 5) if the receiver has just selected the other serial inputs (receiver LOOPEN was switched).

A loss of sync is typically indicated by an abundance of erroneous nibbles. If several sequential data words output by the receiver contain a substantial number of erroneous nibbles, the receiver is likely to be out of synchronization with the transmitter's signal. If the problem is intermittent or temporary, baud level synchronization will be re-acquired from the transmitter's continuous signal.

Even after baud synchronization is achieved, errors on the output data are likely to occur. This is due to frame misalignment. (See Figure 4.) Once a sync frame is received, (indicated to the system by a logic HIGH on the receiver's SYNC signal), the receiver will realign its frame boundaries to match those of the incoming signal. At this time, the synchronous clocks (1XCLK and 2XCLK) will be *stretched* (never truncated) so they align with the new, proper frame boundary. Figure 28 shows typical switching waveforms when sync is re-acquired by the receiver. If the transmitter is sending continuous data frames without a sync frame, the receiver will remain misaligned.

Figure 28. Re-acquiring Sync



Typical Configuration for Guaranteed Data Integrity

A loss of synchronization will occur when the serial data stream is interrupted and then reapplied. It is conceivable that the receiver might not reacquire lock, since it is already locked onto the reference clock input. It is, therefore, recommended that the system be capable of interrupting the reference clock in the event that a signal is not present on the serial data inputs.

A simple logic gate inserted between the reference clock signal and the reference clock input can be used to gate the clock when serial input signals are applied, as shown in Figure 29. This will ensure that

the REFCLK is applied at the same time as the serial input and allow the receiver to reliably recover the receiver clock and the data. The timing for this operation is shown in Figure 30.

Figure 29. Gating the Clock

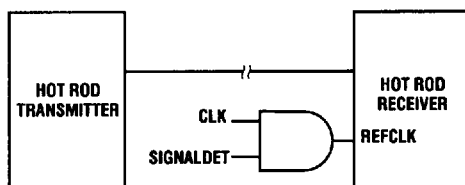
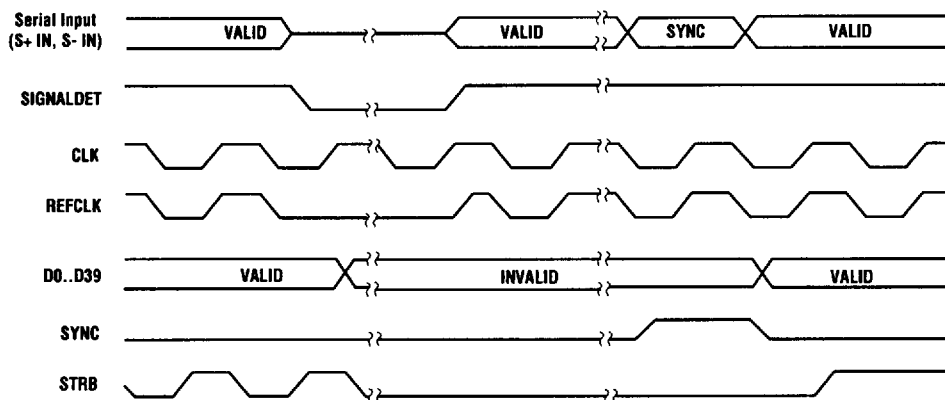
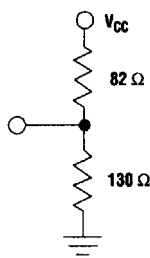


Figure 30. Clock and Data Recovery

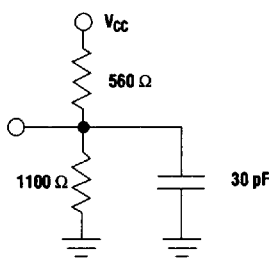


ECL Test Load



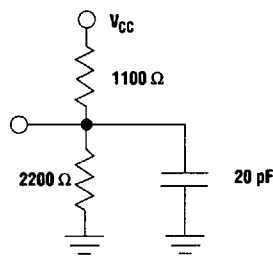
TTL Test Load

(All Tx, Rx 1XCLK, 2XCLK, STRB)



TTL Test Load

(Rx: D0..D39, SYNC, ERROR)



Guide to Specifications

There are a substantial number of specifications defining operation of the Hot Rod chip set. They have been segmented for quick reference:

Conditions

- Absolute maximum ratings
- Operating conditions
- Test conditions

DC Specifications (Transmitter)

- TTL-level pins
- PECL-level pins

DC Specifications (Receiver)

- TTL-level pins
- PECL-level pins

AC Specifications (Transmitter)

- Host system interface timing
- Control timing
- Serial interface timing
- Serial loopback timing

AC Specifications (Receiver)

- Data interface timing
- Data/sync timing
- Serial interface timing
- Serial loopback timing

Many of the switching specifications listed are a function of the user-selectable data rate. In these cases, variables have been used to define equations for calculating these specifications. These are fully described in the Notes following each section of the specifications.

Recommended Operating Conditions

Supply Voltage

- $+5\text{ V} \pm 5\%$ (4.75 V to 5.25 V)

Temperature

- Ambient temperature 0-70°C with at least 100 LFM (linear feet/min.) of moving air

Junction Temperature

- $\theta_{JC} < 5^\circ\text{C/Watt}$
- $\theta_{CA} < 20^\circ\text{C/Watt}$

Absolute Maximum Ratings

(Exceeding these ratings may damage the device)

Storage temperature	-65°C to +150°C
Ambient temperature	-55°C to +125°C
Supply voltage to ground	-0.5 V to +7.0 V
DC input voltage	-0.5 V to (VCC +0.5 V)
DC input current	-30 mA to +5 mA

Capacitance*

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 2.0\text{ V at } f = 1\text{ MHz}$		6		pF
C_{OUT}	Output capacitance	$V_{OUT} = 2.0\text{ V at } f = 1\text{ MHz}$		9		pF

* These parameters are not 100% tested, but are periodically sampled.

DC Characteristics (Over operating range unless otherwise specified)**GA9011 Hot Rod Transmitter TTL Signals** (D0..D39, STRB, ACK, REFCLK, 1XCLK, 2XCLK, DIV1, DIV0, LOOPEN, SLAVE)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH voltage	$V_{CC} = \text{Min}$ $I_{OH} = -1.6 \text{ mA}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	2.4	3.2		V
V_{OL}	Output LOW voltage	$V_{CC} = \text{Min}$ $I_{OL} = 8 \text{ mA}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$		0.3	0.5	V
V_{IH}^1	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs	2.0			V
V_{IL}^1	Input LOW level	Guaranteed input logical LOW voltage for all inputs			0.8	V
I_{IL}	Input LOW current	$V_{CC} = \text{Max}$ $V_{IN} = 0.40 \text{ V}$		-150	-400	μA
I_{IH}	Input HIGH current	$V_{CC} = \text{Max}$ $V_{IN} = 2.7 \text{ V}$			25	μA
I_I	Input HIGH current	$V_{CC} = \text{Max}$ $V_{IN} = 5.5 \text{ V}$			1	mA
I_{SC}^2	Output short-circuit current	$V_{CC} = \text{Max}$ $V_{OUT} = 0.5 \text{ V}$	-30	-60	-120	mA
I_{CC}	Power supply current	$V_{CC} = \text{Max}$		310	400	mA
V_I	Input clamp voltage	$V_{CC} = \text{Min}$ $I_{IN} = -18 \text{ mA}$			-1.2	V

GA9011 Hot Rod Transmitter PECL Signals (S+, S-, L+, L-)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH voltage	$V_{CC} = \text{Min}$, ECL load	$V_{CC} - 1.2$		$V_{CC} - 0.5$	V
V_{OL}	Output LOW voltage	$V_{CC} = \text{Min}$, ECL load	$V_{CC} - 2.0$		$V_{CC} - 1.62$	V
ΔV_{OUT}	Output differential voltage	ECL load	0.7		1.2	V

Notes: Typical limits are: $V_{CC} = +5.0 \text{ V}$ and $T_A = 25^\circ \text{ C}$.

1. These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.

2. No more than one output should be tested at a time. Duration of the short circuit should not exceed one second.

V_{OUT} has been chosen to avoid test problems caused by tester ground degradation.

DC Characteristics (Over operating range unless otherwise specified)

GA9012 Hot Rod Receiver TTL Signals (D0..D39, STRB, SYNC, ERROR, REFCLK, 1XCLK, 2XCLK, DIV1, DIV0, LOOPEN)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH voltage	$V_{CC} = \text{Min}$ $I_{OH} = -1.6 \text{ mA}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	2.4	3.2		V
V_{OL}	Output LOW voltage	$V_{CC} = \text{Min}$ $I_{OL} = 4 \text{ mA}$ $V_{IN} = V_{IH} \text{ or } V_{IL} = 8 \text{ mA}^2$		0.3	0.5	V
V_{IH}^3	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs	2.0			V
V_{IL}^3	Input LOW level	Guaranteed input logical LOW voltage for all inputs			0.8	V
I_{IL}	Input LOW current	$V_{CC} = \text{Max}$ $V_{IN} = 0.40 \text{ V}$		-150	-400	μA
I_{IH}	Input HIGH current	$V_{CC} = \text{Max}$ $V_{IN} = 2.7 \text{ V}$			25	μA
I_I	Input HIGH current	$V_{CC} = \text{Max}$ $V_{IN} = 5.5 \text{ V}$			1	mA
I_{SC}^1	Output short-circuit current	$V_{CC} = \text{Max}$ $V_{OUT} = 0.5 \text{ V}$	-30	-60	-120	mA
I_{CC}	Power supply current	$V_{CC} = \text{Max}$		360	450	mA
V_I	Input clamp voltage	$V_{CC} = \text{Min}$ $I_{IN} = -18 \text{ mA}$			-1.2	V
I_{OZH}^4	Output leakage current HIGH	$V_{CC} = \text{Max}$ $V_{IL} = 0.8 \text{ V}$ $V_{IH} = 2.0 \text{ V}$ $V_{OUT} = 2.7 \text{ V}$			100	μA
I_{OZL}^4	Output leakage current LOW	$V_{CC} = \text{Max}$ $V_{IL} = 0.8 \text{ V}$ $V_{IH} = 2.0 \text{ V}$ $V_{OUT} = 0.4 \text{ V}$			-100	μA

GA9012 Hot Rod Receiver PECL Signals (S+ In, S- In, S+ Out, S- Out, L+ In, L- In, L+ Out, L- Out)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{IHS}	Input HIGH voltage	$V_{CC} = \text{Min}$	$V_{CC} - 1.3$		$V_{CC} - 0.5$	V
V_{ILS}	Input LOW voltage	$V_{CC} = \text{Max}$	$V_{CC} - 2.0$		$V_{CC} - 1.4$	V
V_{DIF}	Differential input voltage	$V_{CC} = \text{Max}$	0.4		1.2	V
V_{ICM}	Input common-mode voltage		2.5		$V_{CC} - 1.1$	V
I_{IL}	Input LOW current	$V_{CC} = \text{Max}$ $V_{IN} = V_{CC} - 2.0 \text{ V}$	0.5			μA
I_{IH}	Input HIGH current	$V_{CC} = \text{Max}$ $V_{IN} = V_{CC} - 0.5 \text{ V}$			250	μA

Notes: Typical limits are: $V_{CC} = +5.0 \text{ V}$ and $T_A = 25^\circ \text{ C}$.

1. No more than one output should be tested at a time. Duration of the short circuit should not exceed one second.

V_{OUT} has been chosen to avoid test problems caused by tester ground degradation.

2. The 1XCLK, 2XCLK, and STRB signals have 8 mA output drivers. All other outputs have a 4 mA I_{OL} .

3. These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.

4. I/O pin leakage is the worst case of I_{OZX} or I_X (where $X = H$ or L).

AC Specifications – GA9011 Hot Rod Transmitter

Parameter	Notes	Description	Min	Max	Unit
1		DATA Setup Time	3	—	ns
2		DATA Hold Time	7	—	ns
3	1	STRB Rise to ACK Rise	10t + 0	62t + 10	ns
	1,2	STRB Rise to ACK Rise (DIV pins HIGH)	12t + 0	66t + 10	ns
4	1,3	STRB Fall to ACK Fall	6t + 0	8t + 10	ns
	1,2	STRB Fall to ACK Fall (DIV pins HIGH)	8t + 0	12t + 10	ns
5		ACK Rise to STRB Rise	0	—	ns
6	1	STRB Pulse Width LOW	3t + 0	—	ns
	1,2	STRB Pulse Width LOW (DIV pins HIGH)	6t + 0	—	ns
7		STRB Pulse Width HIGH	4	—	ns
8	1,4	ACK Pulse Width LOW	6t + 0	—	ns
9	1,4	ACK Pulse Width HIGH	8t - 1	—	ns
10	1,5	1XCLK Fall to STRB Rise	—	8t + 5	ns
11	1	1XCLK Pulse Width LOW	25t - 3.5	25t + 3.5	ns
12	1	1XCLK Pulse Width HIGH	25t - 3.5	25t + 3.5	ns
13	1,6	1XCLK Period	50t - 1	50t + 1	ns
14	1,6	2XCLK Period	25t - 1	25t + 1	ns
15	1	2XCLK Pulse Width LOW	12t - 3.5	12t + 3.5	ns
16	1	2XCLK Pulse Width HIGH	13t - 3.5	13t + 3.5	ns
17		2XCLK Fall to 1XCLK Fall	-2.5	2.5	ns
18		2XCLK Fall to 1XCLK Rise	-3.5	3.5	ns
19		REFCLK Pulse Width LOW	15	—	ns
20		REFCLK Pulse Width HIGH	15	—	ns
21	7	REFCLK Period	40	50	ns
22		REFCLK to 1XCLK	0	10	ns
23	8	SLAVE Setup Time to REFCLK Rise	6	—	ns
24-26		No longer applicable.			
27	9	Input Rise Time	—	6	ns
28	9	Input Fall Time	—	6	ns
29	10	Output Rise Time	2	6	ns
30	10	Output Fall Time	2	6	ns
31	1	Transmitter Latency	63t + 0	113t + 10	ns
32	1,11	Frame Boundary to 1XCLK Fall	6t - 3	6t + 10	ns
33	1,11	Frame Boundary to 2XCLK Fall	6t - 3	6t + 10	ns
34		Serial Output Rise Time	150	320	ps
35		Serial Output Fall Time	150	320	ps
36		Serial Output Skew	-100	+100	ps
37		Serial Disable Time	—	20	ns
38		Serial Enable Time	0	—	ns
39	1	1XCLK Setup Time to 2XCLK Rise	12t - 3.5	—	ns
40	1	1XCLK Hold Time from 2XCLK Rise	13t - 3.5	—	ns
41	8	SLAVE Hold Time from REFCLK Rise	6	—	ns

AC Specifications – GA9012 Hot Rod Receiver

Parameter	Notes	Description	Min	Max	Unit
51	1	D[0..31] Setup Time (to 1XCLK, STRB)	35t - 8.5	—	ns
	1,13	D[32..39] Setup Time (to 1XCLK, STRB)	35t - 3.5	—	ns
52	1	D[0..39] Hold Time (from 1XCLK, STRB)	14t - 2.5	—	ns
53	1,13	ERROR Setup Time (to STRB, 1XCLK)	35t - 3.5	—	ns
54	1	ERROR Hold Time (from STRB, 1XCLK)	14t - 2.5	—	ns
55	1,3	1XCLK Pulse Width HIGH	25t - 3.5	25t + 3.5	ns
56	1,3	1XCLK Pulse Width LOW	25t - 3.5	25t + 3.5	ns
57	2	1XCLK Period	50t - 1	50t + 1	ns
58	1	2XCLK Pulse Width HIGH	13t - 3.5	13t + 3.5	ns
59	1	2XCLK Pulse Width LOW	12t - 3.5	12t + 3.5	ns
60	2	2XCLK Period	25t - 1	25t + 1	ns
61		2XCLK Fall to 1XCLK Fall	-2.5	2.5	ns
62		2XCLK Fall to 1XCLK Rise	-3	5	ns
63		1XCLK Rise to STRB Rise	-2.5	2.5	ns
64	1,4	STRB Pulse Width HIGH	25t - 3.5	—	ns
65	1	STRB Pulse Width LOW	25t - 3.5	—	ns
66	1	SYNC Setup Time (to 1XCLK)	35t - 3.5	—	ns
67	1	SYNC Hold Time (from 1XCLK)	14t - 2.5	—	ns
68	5	REFCLK Period	40	50	ns
69	6	REFCLK to 1XCLK	—	—	ns
70	1	Frame Boundary to 1XCLK Rise	48t	48t + 5	ns
71-73		No longer specified.			
74	7	Input Rise Time	—	6	ns
75	7	Input Fall Time	—	6	ns
76	8	Output Rise Time	2	6	ns
77	8	Output Fall Time	2	6	ns
78	1	Receiver Latency	48t	48t + 6	ns
79	9	Baud Synchronization Time	—	50	µs
80	1	Serial Input Rise Time		MIN (0.4t, 1)	ns
81	1	Serial Input Fall Time		MIN (0.4t, 1)	ns
82	1	Serial Input Jitter		±0.25t	ns
	1,11	Serial Input Jitter (DIV pins HIGH)		±0.125t	ns
83	1	Serial Input Skew		±0.125t	ps
84	10	Serial In/Out Delay		125	ps
85	1	1XCLK, STRB Setup Time to 2XCLK Rise	12t - 3.5	—	ns
86	1	1XCLK, STRB Hold Time from 2XCLK Rise	13t - 3.5	—	ns
87	1,12,13	D[0..31] Setup Time to 2XCLK Rise	22t - 9.5	—	ns
	1,12,13	D[32..39] ERROR, SYNC Setup to 2XCLK Rise	22t - 4.5	—	ns
88	1,12	D[0..39] ERROR, SYNC Hold from 2XCLK Rise	27t - 2.5	—	ns

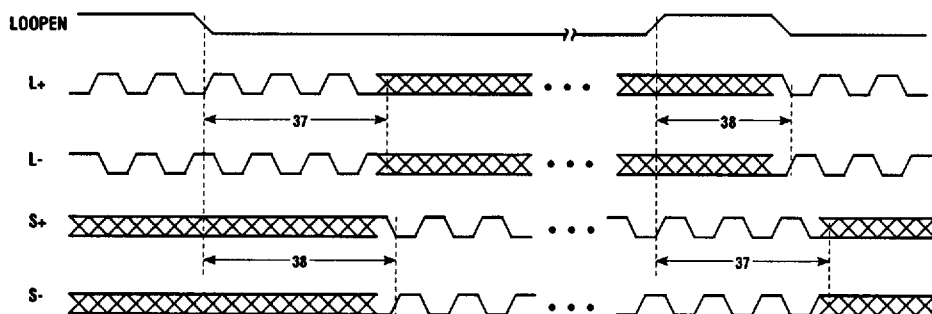
NOTES to Transmitter AC Specs

1. "t" designates 1 baud time, which is calculated as $(T_{2V}/50) \times m$, where m is the value of the DIV pins (e.g., 1, 2, 4). At full speed, the serial link is operating at 1.0 Gbaud, and t = 1 ns. All of these parameters can be calculated from the serial baud rate.
2. Several specifications are different at the maximum data rate. These specifications apply only to the case when DIV1 = DIV0 = "HIGH."
3. This specification applies only to the level-driven interface described in the Transmitter Functional Description—Input Control.
4. The maximum ACK pulse width is controlled by the width of the STRB pulse from the host system.
5. This specification is offered only as a guide to minimizing latency, and is described in the Transmitter Functional Description—Input Control.
6. During normal operation, these track the PLL, and there is essentially no variation.
7. MIN is based on a 25 MHz input and MAX is based on a 20 MHz input.
8. If the 1XCLK from a master device is delayed 7-30 ns, then connected to the SLAVE pin of the other devices, synchronous parallel operation is achieved.
9. Applies to TTL inputs D0..D39, STRB, REFCLK, SLAVE, and LOOPEN.
10. Applies to TTL outputs ACK, 1XCLK, and 2XCLK.
11. This information is provided for debugging purposes.
12. Frequency tolerance on REFCLK is ± 100 parts per million (ppm).

NOTES to Receiver AC Specs

1. "t" designates 1 baud time, which depends on the speed of the part. This "t" must match that of the corresponding Hot Rod transmitter. (See Note 1 of Transmitter AC specs.)
2. These match the frequency of incoming bauds. This assumes the incoming baud rate is within 0.2% of that defined by REFCLK and the DIV pins.
3. The maximum values listed correspond to normal operation of the part. If frame synchronization is re-acquired, these clocks may stretch (one cycle) during acquisition.
4. The STRB pulse width HIGH is unlimited; if sync frames are received, STRB will remain HIGH.
5. The REFCLK period must match that of the corresponding Hot Rod transmitter.
6. REFCLK and 1XCLK have no defined phase relationship. In addition, the 1XCLK is generated from the incoming baud stream, and its frequency could deviate slightly from that of REFCLK.
7. Applies to TTL signals REFCLK and LOOPEN.
8. Applies to TTL signals 1XCLK, 2XCLK, SYNC, ERROR, STRB, and D0..D39.
9. In addition to the time required for baud synchronization, the appearance of a HIGH on SYNC depends on the corresponding Hot Rod transmitter sending a sync frame.
10. The serial input and output lines are wire connections; there is no gate delay. However, due to potential impedance mismatching, daisy-chaining of Hot Rod receivers to one transmitter serial signal is discouraged.
11. Several specifications are different at the maximum data rate. These specifications apply to the case when DIV1 = DIV0 = "HIGH."
12. These parameters are with respect to 2XCLK rise when 1XCLK is "LOW".
13. The outputs and switching are staggered; some designs may benefit from extra setup time available on the highest order [D39..D32] data byte, ERROR, and SYNC signals.
14. Frequency tolerance on REFCLK is ± 100 ppm.

Figure 34.



Receiver Waveforms

Figure 35.

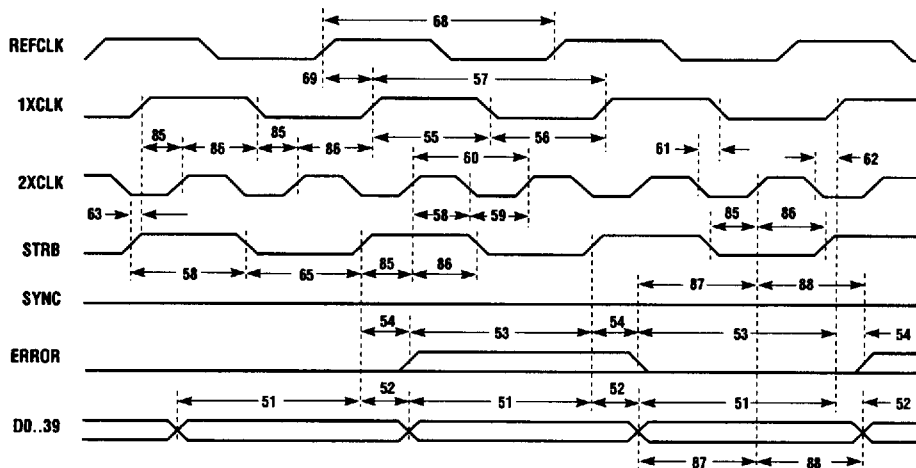


Figure 36.

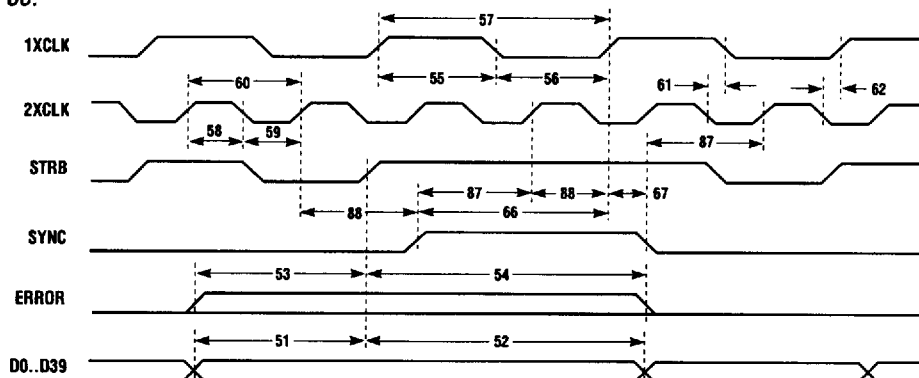


Figure 37.

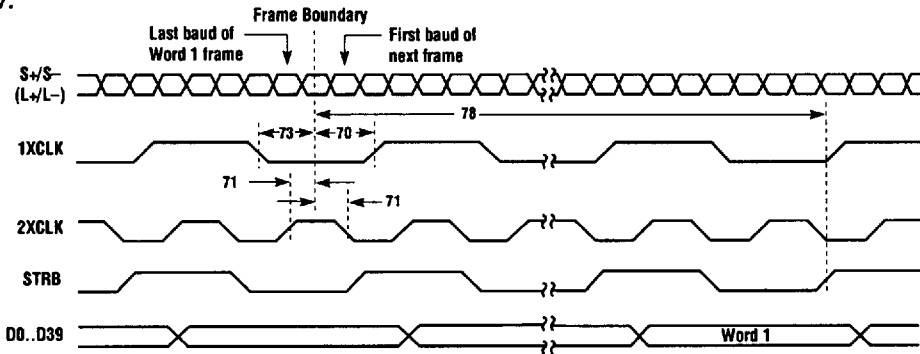


Figure 38.

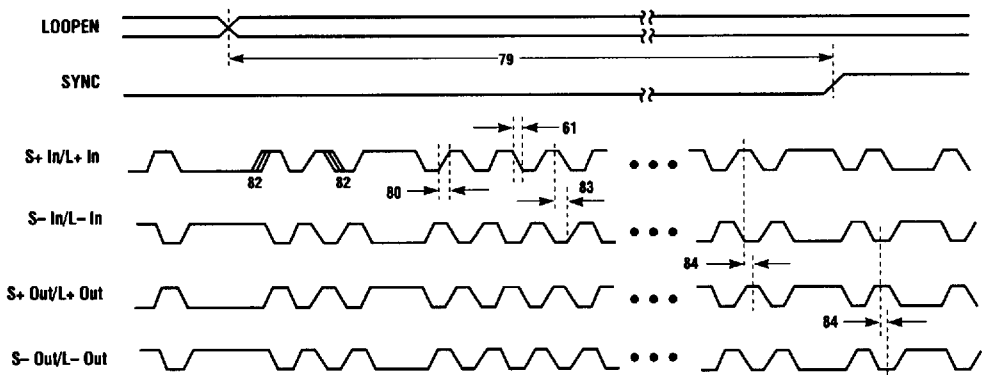


Table 5. Transmitter Pin Descriptions

Name	Qty	I/O	Logic Level	Description
DO..D39	40	In	TTL	40-bit parallel data word to be transmitted
STRB	1	In	TTL	Rising edge latches in new 40-bit data word
ACK	1	Out	TTL	Acknowledges transmitter ready for new data word
REFCLK	1	In	TTL	Reference clock input
SLAVE	1	In	TTL	Maintains word sync in multiple Hot Rod systems
1XCLK	1	Out	TTL	Synchronous word rate clock for host system use
2XCLK	1	Out	TTL	Synchronous 2X word rate clock for host system use
DIV1, DIV0	2	In	TTL	Data rate divider pins
TEST	1	In	TTL	Factory test pin; must always be tied to GND
S+, S-	2	Out	PECL	Differential serial data outputs
LOOPEN	1	In	TTL	Disables S+, S-; enable loopback mode and L+, L-
L+, L-	2	Out	PECL	Differential loopback data outputs
GND	5	In	N/A	All pins must be tied to GND
VCC	4	In	N/A	All pins must be tied to +5 V

Table 6. Receiver Pin Descriptions

Name	Qty	I/O	Logic Level	Description
S+ In, S- In	2	In	PECL	Differential serial data inputs
S+ Out, S- Out	2	Out	PECL	Continuation of S+ In, S- In for easy termination
LOOPEN	1	In	TTL	Enables loopback mode
L+ In, L- In	2	In	PECL	Differential loopback data inputs for loopback mode
L+ Out, L- Out	2	Out	PECL	Continuation of L+ In, L- In for easy termination
REFCLK	1	In	TTL	Reference clock input
1XCLK	1	Out	TTL	Synchronous word rate clock for host system use
2XCLK	1	Out	TTL	Synchronous 2X word rate clock for host system use
DIV1, DIV0	2	In	TTL	Data rate divider; must match transmitter DIV pins
SYNC	1	Out	TTL	Indicates last frame received was a sync frame
ERROR	1	Out	TTL	Indicates one or more invalid 5b code words
TEST	1	In	TTL	Factory test pin; must always be tied to GND
DO..D39	40	Out	TTL	40-bit parallel word TTL-level output bus
STRB	1	Out	TTL	Rising edge indicates new data on output bus
GND	4	In	N/A	All pins must be tied to GND
VCC	4	In	N/A	All pins must be tied to +5 V

Figure 39. Pinout for GA9011 Hot Rod Transmitter

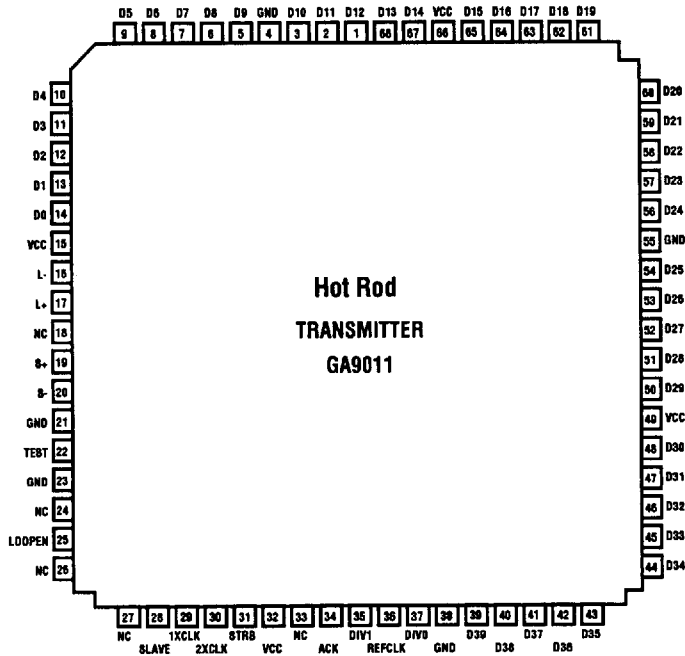
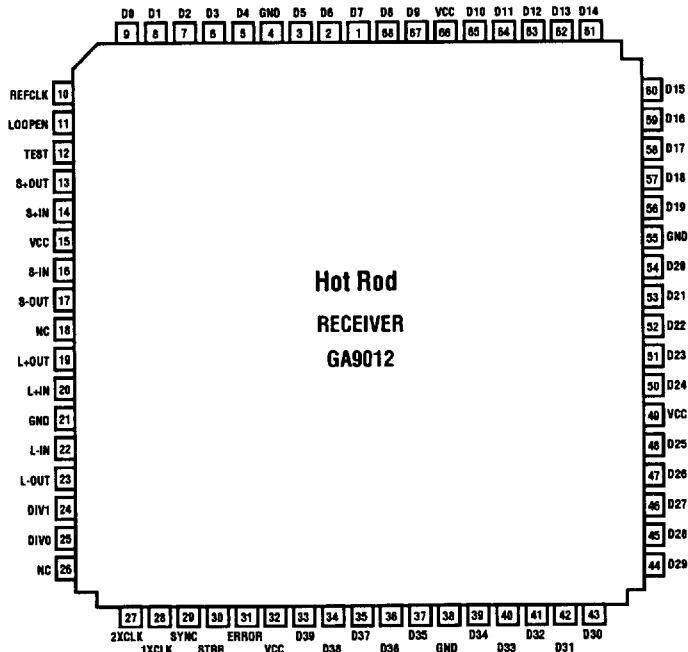
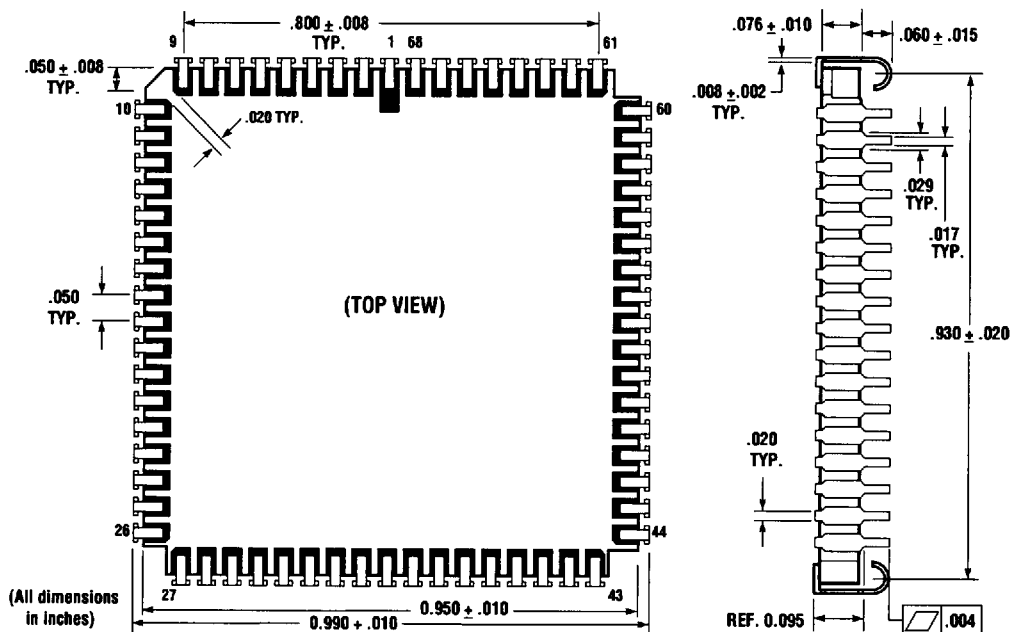


Figure 40. Pinout for GA9012 Hot Rod Receiver



68-Pin J-Lead (CLCC) Package



Ordering Information

GA —

Device Number/Description

- 9011 — Hot Rod Transmitter
- 9012 — Hot Rod Receiver

Temperature Range

- C — Commercial

Speed

- 8 — 800 Mbit/sec maximum data rate
- 5 — 500 Mbit/sec maximum data rate
- 4 — 400 Mbit/sec maximum data rate
- 2 — 200 Mbit/sec maximum data rate

Package Type

- C — 68-Pin Ceramic J-Lead CLCC



DATA COMMUNICATIONS

S E M I C O N D U C T O R , I N C .

Section 6 - Packaging

Thermal Resistance Information	6-3
Device Markings	6-3
Package Outlines	6-4

Packaging

Thermal Resistance Information

Power Dissipation Calculations

The maximum power dissipation that an IC can tolerate is determined by the thermal impedance characteristics of the package. The equation to find the allowable power dissipation at a given ambient operating temperature is:

$$P_D = (T_J - T_A) / \theta_{JA}, \text{ where:}$$

P_D = power dissipation at ambient operating temperature

T_J = maximum junction operating temperature (150°C is typically used)

T_A = maximum ambient operating temperature (free air)

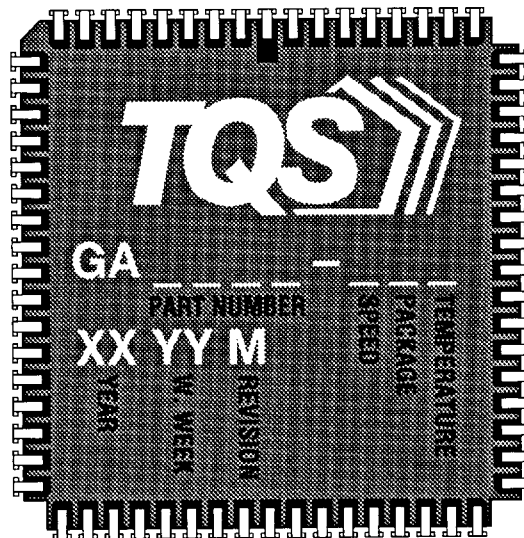
θ_{JA} = typical thermal resistance of junction to ambient (°C/W)

Packaging Notes

Unless otherwise indicated, all thermal impedances listed are typical range values or values in still air for the package only. These impedances will vary when additional heat sinking capability is provided through PCB solder attachment or air flow.

Device Markings

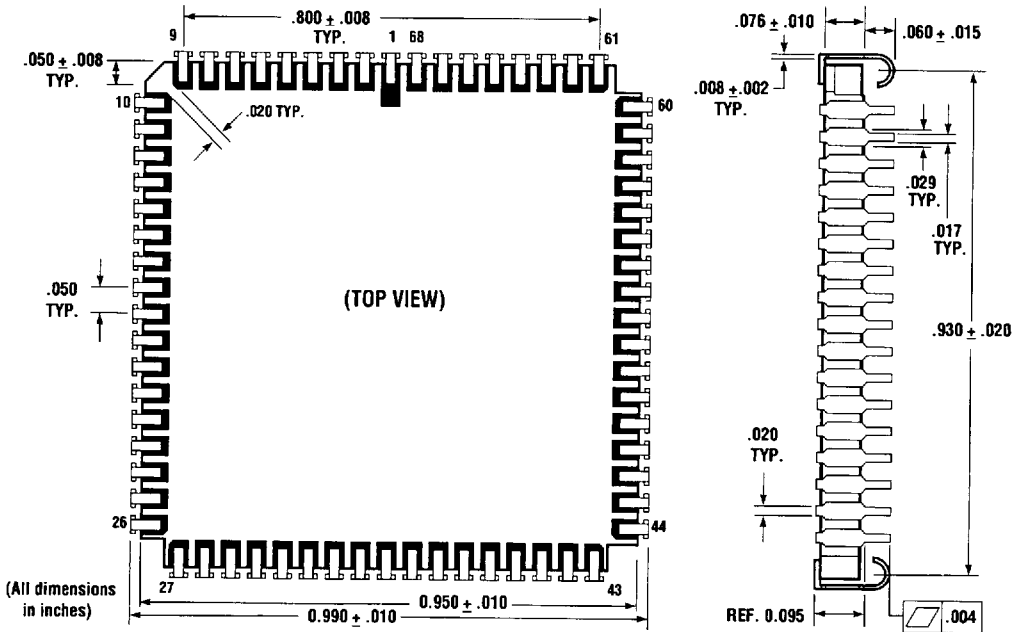
TriQuint's Standard Device Markings



Package Outlines

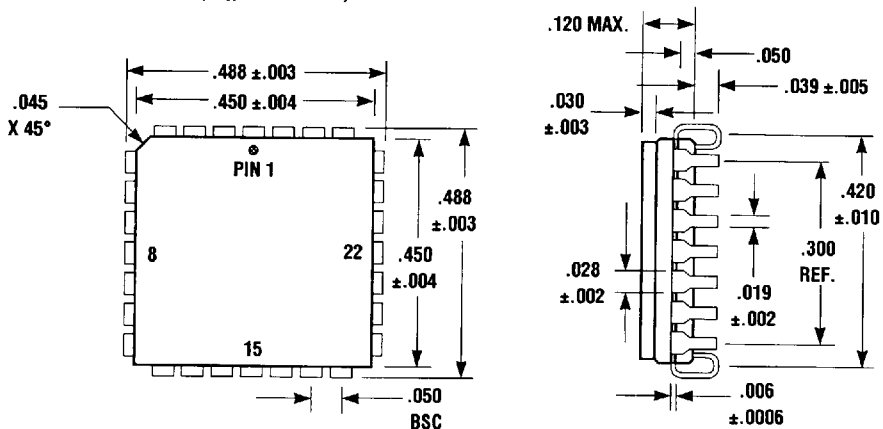
68-Pin J-Lead (CLCC) Package

Packaging for: GA9011, GA9012 ($\theta_{JA} = 25^{\circ}\text{C/Watt}$)



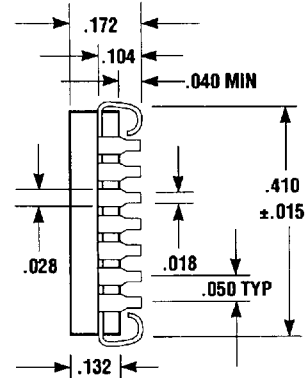
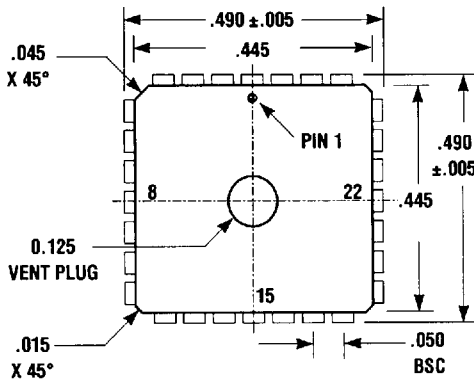
28-Pin J-Lead CerQuad Package

Packaging for: GA9101, GA9102 ($\theta_{JA} = 60^{\circ}\text{C/Watt}$)



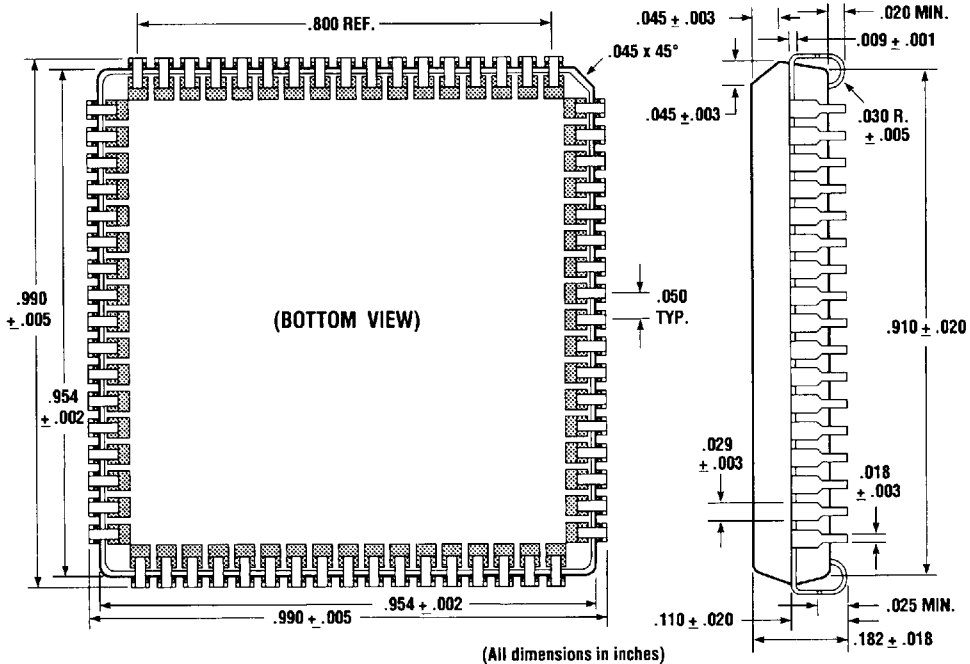
28-Pin J-Lead MQuad Package

Packaging for: GA9101, GA9102 ($\theta_{JA} = 42^{\circ}\text{C/Watt}$)



68-Pin PLCC Package

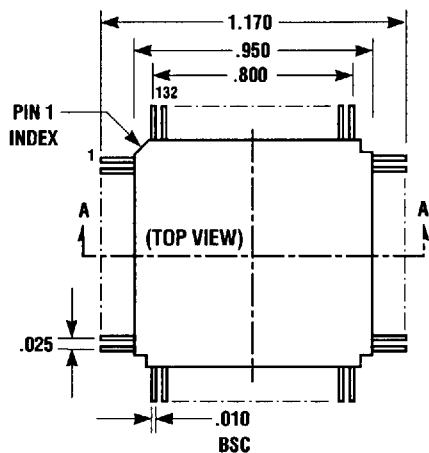
Packaging for: GA9103, GA9104 ($\theta_{JA} = 47^{\circ}\text{C/Watt}$)



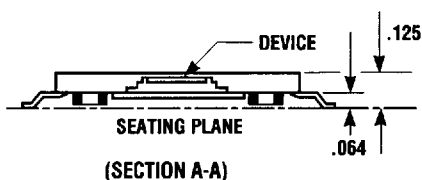
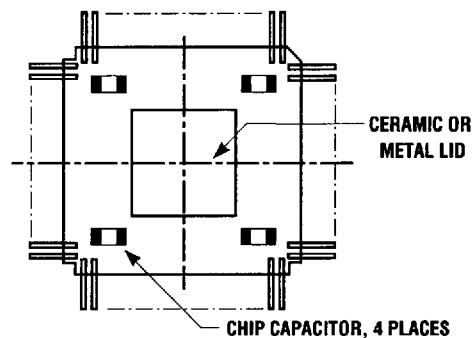
PACKAGING

132-Pin Leaded Ceramic Chip Carrier

Packaging for: TQ8016 (Heat sink required, $\theta_{JC} = 8^{\circ}\text{C/Watt}$)

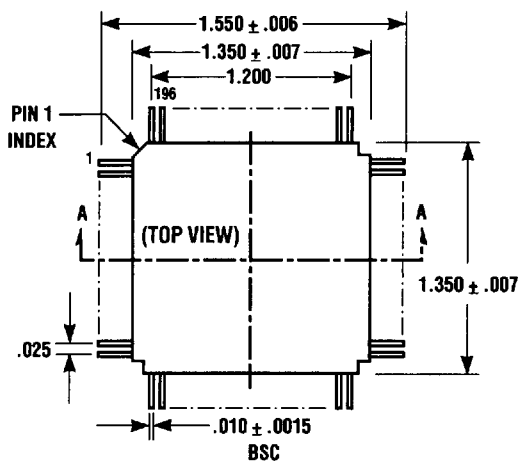


(BOTTOM VIEW)

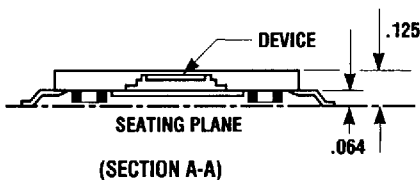
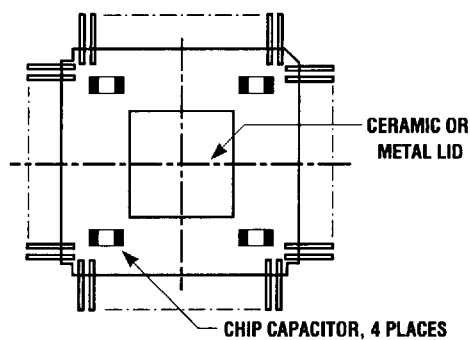


196-Pin Leaded Ceramic Chip Carrier

Packaging for: TQ8032 (Heat sink required, $\theta_{JC} = 8^{\circ}\text{C/Watt}$)



(BOTTOM VIEW)



TriQuint 
SEMICONDUCTOR