

SONY**CXK581120J****- 12/15/20****131,072-WORD X 8-BIT HIGH SPEED CMOS STATIC RAM****PRELIMINARY****DESCRIPTION SONY CORP/COMPONENT PRODS**

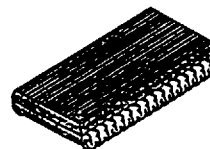
The CXK581120J is a high speed 1M-bit CMOS static RAM organized as a 131,072-word by 8-bit array. It operates at 12/15/20ns access time from a single 5V power supply, utilizing center-ground/power pin architecture.

FEATURES

- High speed, low power consumption:

	Access time (Max.)	Power consumption (Typ., Cycle = Min.)
CXK581120J- 12	12ns	690mW
CXK581120J- 15	15ns	550mW
CXK581120J-20	20ns	500mW
- Single +5V power supply
- Fully static memory. No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible: All inputs and outputs.
- Common data input and output: three state output.
- Available in a 32 pin 400mil SOJ package.

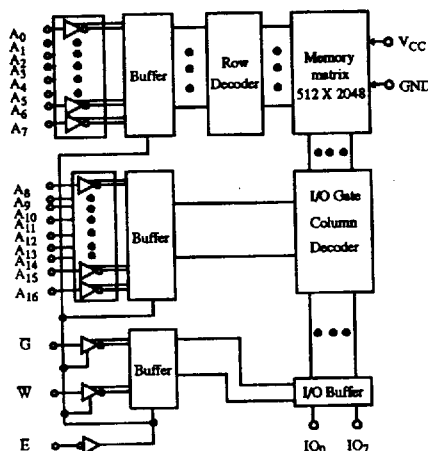
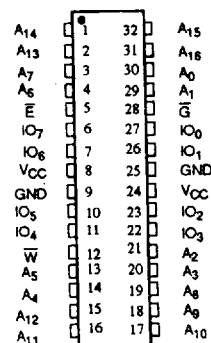
CXK581120J
32 PIN SOJ
(PLASTIC)

**FUNCTION**

131,072-word x 8-bit Static RAM

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A ₀ to A ₁₆	Address input
IO ₀ to IO ₇	Data input/output
E	Chip enable input
W	Write enable input
G	Output enable input
V _{CC}	+5V power supply
GND	Ground

BLOCK DIAGRAM**PIN CONFIGURATION (TOP VIEW)**

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ABSOLUTE MAXIMUM RATINGS

 $(T_A = 25^{\circ}\text{C}, \text{GND} = 0\text{V})$

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ITEM	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to $V_{CC}+0.5$	V
Input and output voltage	V_{IO}	-0.5 to $V_{CC}+0.5$	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	T_{OPR}	0 to +70	$^{\circ}\text{C}$
Storage temperature	T_{STG}	-55 to +150	$^{\circ}\text{C}$
Soldering temperature • time	T_{SOLDER}	260 • 10	$^{\circ}\text{C} \bullet \text{sec}$

TRUTH TABLE

MODE	$\bar{E}$	$\bar{G}$	$\bar{W}$	IO_{0-7}	POWER
Not selected	H	X	X	Hi-Z	I_{SB1}, I_{SB2}
Output disable	L	H	H	Hi-Z	I_{CC}
Read	L	L	H	Data out	I_{CC}
Write	L	X	L	Data in	I_{CC}

Note: X = H OR L

DC RECOMMENDED OPERATING CONDITIONS

 $(T_A = 0 \text{ to } +70^{\circ}\text{C}, \text{GND} = 0\text{V})$

ITEM		SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	-12/15	V_{CC}	4.75	5.0	5.25	V
	20		4.5	5.0	5.5	V
Input high voltage		V_{IH}	2.2	—	$V_{CC}+0.3$	V
Input low voltage		V_{IL}	-0.3	—	0.8	V

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ELECTRICAL CHARACTERISTICS

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• DC AND OPERATING CHARACTERISTICS

ITEM	SYMBOL	TEST CONDITIONS		MIN.	TYP*	MAX.	UNIT
Input leakage current	I_{LI}	$V_{IN} = GND \text{ to } V_{CC}$		-1	—	1	μA
Output leakage current	I_{LO}	$V_{IO} = GND \text{ to } V_{CC}$, $\bar{E} = V_{IH} \text{ or } \bar{G} = V_{IH} \text{ or } \bar{W} = V_{IL}$		-1	—	1	μA
Average operating current	I_{CC}	CYCLE = t_{MIN} DUTY = 100% IOUT = 0mA $\bar{E} = V_{IL}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	-12	Write	—	250	mA
				Read	—	180	
			-15	Write	—	220	
				Read	—	150	
			-20	Write	—	200	
				Read	—	140	
Standby current	I_{SB1}	$\bar{E} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V \text{ or } V_{IN} \leq 0.2V$		—	—	10	mA
	I_{SB2}	CYCLE = t_{MIN} , DUTY CYCLE = 100%, $\bar{E} = V_{IH}$, $V_{IN} = V_{IL} \text{ or } V_{IH}$		—	25	40	mA
Output high voltage	V_{OH}	$I_{OH} = -4.0mA$		2.4	—	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0mA$		—	—	0.4	V

* NOTE: $V_{CC} = 5V$, $T_A = 25^\circ C$

I/O CAPACITANCE *

 $(T_A = 25^\circ C, f = 1MHz)$

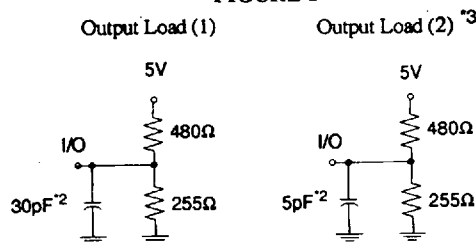
ITEM	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Input capacitance	C_{IN}	$V_{IN} = 0V$	—	5	pF
Output capacitance	C_{IO}	$V_{IO} = 0V$	—	7	pF

* NOTE: This parameter is sampled and is not 100% tested

• AC CHARACTERISTICS AND TEST CONDITIONS ($T_A = 0 \text{ to } +70^\circ C$, $V_{CC} = 5V \pm 5\%$ *1)

ITEM	CONDITIONS
Input pulse high level	$V_{IH} = 3.0V$
Input pulse low level	$V_{IL} = 0V$
Input rise time	$t_R = 3nS$
Input fall time	$t_F = 3nS$
Input and output reference level	1.5V
Output load conditions	Figure 1

FIGURE 1

*1 $V_{CC} = 5V \pm 10\%$ for CXK581120J-17

*2 Including scope and jig capacitance

*3 For t_{LZ} , t_{HZ} , t_{OHZ} , t_{OLZ} , t_{ow} , t_{wHZ}

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READ CYCLE

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ITEM	SYMBOL	- 12		- 15		- 20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read cycle time	t_{RC}	12	—	15	—	20	—	ns
Address access time	t_{AA}	—	12	—	15	—	20	ns
Chip enable access time	t_{CO}	—	12	—	15	—	20	ns
Output enable to output valid ($\bar{G}$)	t_{OE}	—	6	—	7	—	8	ns
Output hold from address change	t_{OH}	2	—	2	—	3	—	ns
Chip enable to output in low Z ($\bar{E}$)	t_{LZ}^*	3	—	3	—	3	—	ns
Output enable to output in low Z ($\bar{G}$)	t_{OLZ}^*	2	—	2	—	2	—	ns
Chip disable to output in high Z ($\bar{E}$)	t_{HZ}^*	—	6	—	7	—	8	ns
Output disable to output in high Z ($\bar{G}$)	t_{OHZ}^*	—	6	—	7	—	8	ns
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	12	—	15	—	20	ns

WRITE CYCLE

ITEM	SYMBOL	- 12		- 15		- 20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write cycle time	t_{WC}	12	—	15	—	20	—	ns
Address valid to end of write	t_{AW}	10	—	12	—	15	—	ns
Chip enable to end of write	t_{CW}	10	—	12	—	15	—	ns
Data to write time overlap	t_{DW}	6	—	8	—	12	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	10	—	12	—	15	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}^*	3	—	3	—	3	—	ns
Write to output in high Z	t_{WHZ}^*	—	6	—	7	—	9	ns

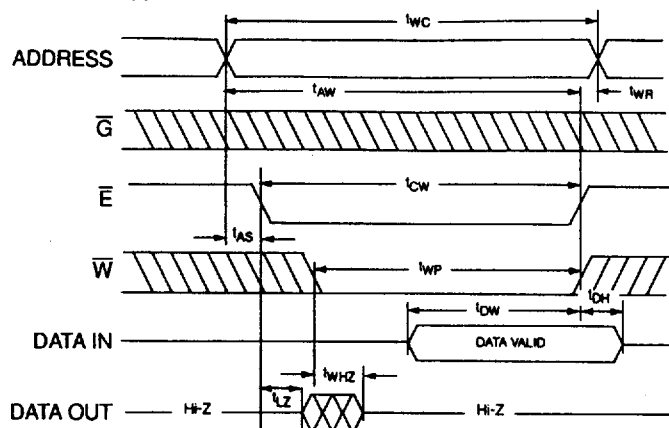
* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and is not 100% tested.

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• WRITE CYCLE (2): $\bar{E}$ CONTROL

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- Note:
- 1) Write occurs during the low overlap of $\bar{E}$ and $\bar{W}$.
 - 2) During $t_{whz}-t_{lz}$, the I/O pins are in the output state during which data input signals of the opposite phase to the output must not be applied.