PCI Clock Generator

Features

- Generates up to 8 preset CPU frequencies, 1 PCI clock, 1 peripheral clock, and buffers the input reference frequency
- Tristate and output enable feature supporting "Green PC" applications
- External loop filter provides exceptionally smooth, glitch-free frequency transitions
- Low, short-term and long-term jitter
- Supports Pentium™ and all x86-based designs
- Supports ISA, VESA, and PCI-based designs
- CMOS technology in 20-pin PDIP and SOIC
- 5V or 3.3V supply

Description

CH9080 is a triple PLL clock generator designed for high performance computer motherboards used in portable computers, notebooks, and handheld PDAs.

CH9080 buffers the 14.318 MHz reference frequency into two outputs, generates three CPU clocks from a preset ROM table, and provides one PCI clock and one peripheral clock. The CPU output frequencies can be selected with the frequency select inputs, FS[2:0].

The CH9080 generates all essential clock signals for personal computer motherboards, eliminating the need for multiple oscillators.

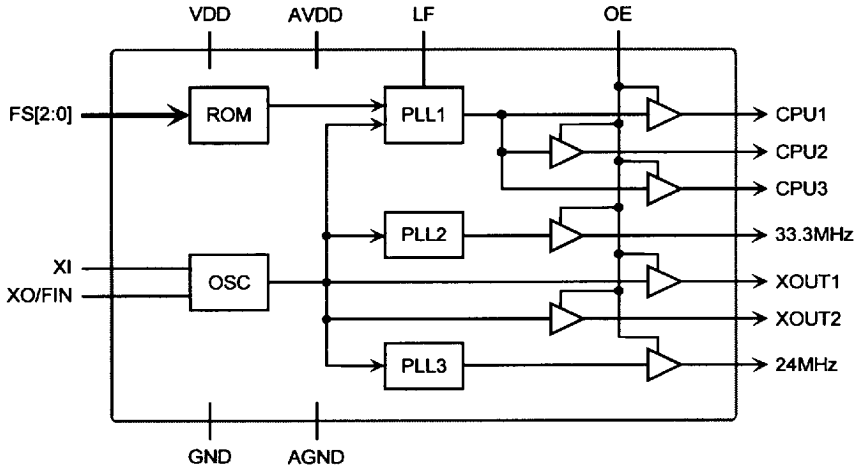

Figure 1: Block Diagram

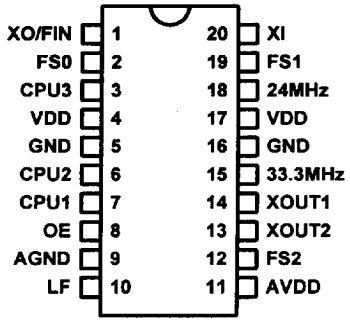

Figure 2: CH9080A

Table 1 • Pin Description CH9080A

Pin	Type	Symbol	Description
1	Out / In	XO / FIN	Crystal output or external FREF input
2, 12, 19	In	FS0, FS2, FS1	Frequency select inputs (internal pull-up)
3, 6, 7	Out	CPU3, CPU2, CPU1	CPU clock outputs
4, 17	Power	VDD	5V or 3.3V supply
5, 16	Power	GND	Ground
8	In	OE	Output enable (active high, internal pull-up). When OE is low, all outputs are tristated.
9	Power	AGND	Analog ground
10	Out	LF	External loop filter
11	Power	AVDD	Analog 5V supply
13, 14	Out	XOUT2, XOUT1	Buffered reference (14.318 MHz) clock output
15	Out	33.3 MHz	33.3 MHz PCI clock output
18	Out	24 MHz	24 MHz clock output
20	In	XI	Crystal input

Table 2 • Frequencies for CH9080A (in MHz)

Frequency Select Inputs			
FS2	FS1	FS0	CPU
0	0	0	8.0
0	0	1	8.0
0	1	0	8.0
0	1	1	16.0
1	0	0	25.0
1	0	1	33.3
1	1	0	40.0
1	1	1	50.0

Table 3 • Absolute Maximum Ratings

Symbol	Description	Value	Unit
V_{DD}	Power supply voltage with respect to GND	–0.5 TO +7.0	V
V_{IN}	Input voltage on any pin with respect to GND	–0.5 TO VDD+0.5	V
TSTOR	Storage temperature	–55 TO +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 4 • DC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
V_{OH}	Output high voltage	V_{DD} = 4.75V, I_{OH} = 12mA	2.4			V
V_{OL}	Output low voltage	V_{DD} = 4.75V, I_{OL} = 12mA			0.4	V
V_{IH}	Input high voltage		2.0			V
V_{IL}	Input low voltage				0.8	V
I_{PU}	Input pull-up current			5	20	µA
I_{LK}	Input leakage current		–10		10	µA
CI	Input capacitance	Except XO / FIN, XI			10	pF
CI	Input capacitance	Pins XO / FIN, XI		20		pF
I_{DD}	Operating current	V_{DD} = 5V CPU = 40 MHz, No load CPU = 80 MHz, No load		25 30		mA

Table 5 • AC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
FXTAL	Crystal frequency			14.318		MHz
FIN	Input frequency		1	14.318	32	MHz
TIR	Input clock rise time				20	ns
TIF	Input clock fall time				20	ns
TR	Output clock rise time	30 pF load, V_{OUT} = 0.8V to 2.0V			2	ns
TF	Output clock fall time	30 pF load, V_{OUT} = 0.8V to 2.0V			2	ns
TDC	Duty cycle		45	48/52	55	%
TJCC	Jitter, cycle to cycle	CPU = 50 MHz		TBD		ps
TFT	Frequency transition time	8 – 80 MHz		10		ms
TPU	Power up time	From OFF to 100 MHz		15		ms

Table 6 • DC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 3.3V ± 0.3V)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
VOH	Output high voltage	VDD = 3.0V, IOH = 1.5mA	VDD – 0.5			V
VOL	Output low voltage	VDD = 3.0V, IOL = 3mA			0.5	V
VIH	Input high voltage		2.0			V
VIL	Input low voltage				0.8	V
IPU	Input pull-up current			3		µA
ILK	Input leakage current		–10		10	µA
CI	Input capacitance	Except XO / FIN, XI			10	pF
CI	Input capacitance	Pins XO / FIN, XI		20		pF
IDD	Operating current	VDD = 3.3V CPU = 40 MHz, No load CPU = 80 MHz, No load		20 25		mA

Table 7 • AC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 3.3V ± 0.3V)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
FXTAL	Crystal frequency			14.318		MHz
FIN	Input frequency		1	14.318	20	MHz
TIR	Input clock rise time				20	ns
TIF	Input clock fall time				20	ns
TR	Output clock rise time	30 pF load, VOUT = 0.8V to 2.0V			5	ns
TF	Output clock fall time	30 pF load, VOUT = 0.8V to 2.0V			5	ns
TDC	Duty cycle		45	48/52	55	%
TJCC	Jitter, cycle to cycle	CPU = 50 MHz		TBD		ps
TFT	Frequency transition time	8 – 80 MHz		10		ms
TPU	Power up time	From OFF to 100 MHz		15		ms

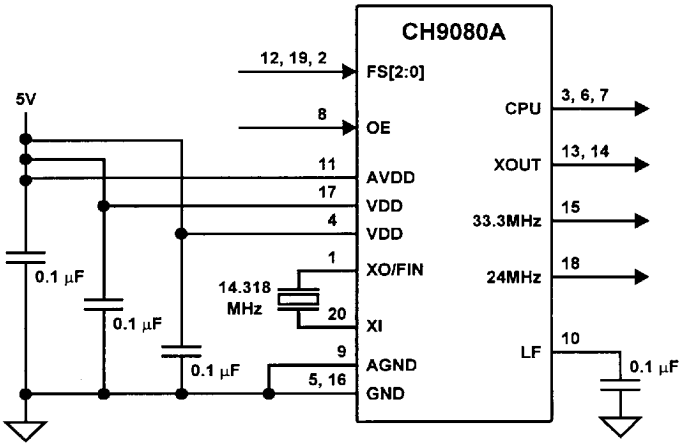

Figure 3: Application Schematic

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ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH9080A-N	300 mil PDIP	20	5V
CH9080A-S	300 mil SOIC	20	5V
CH9080A-N-L	300 mil PDIP	20	3.3V
CH9080A-S-L	300 mil SOIC	20	3.3V