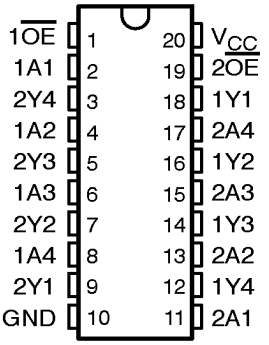
CDC244
OCTAL CLOCK DRIVER WITH 3-STATE OUTPUTS

SCAS501A – APRIL 1995 – REVISED NOVEMBER 1995

- State-of-the-Art *EPIC*-ΠB™ BiCMOS Design Significantly Reduces Power Dissipation
- 750-ps Maximum Output Skew Between All Outputs
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C
- High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})
- Packaged in Shrink Small-Outline Package

DB PACKAGE
(TOP VIEW)



description

This octal clock driver is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The CDC244 provides a low-cost solution in applications requiring skews of less than 500 ps.

The CDC244 is organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

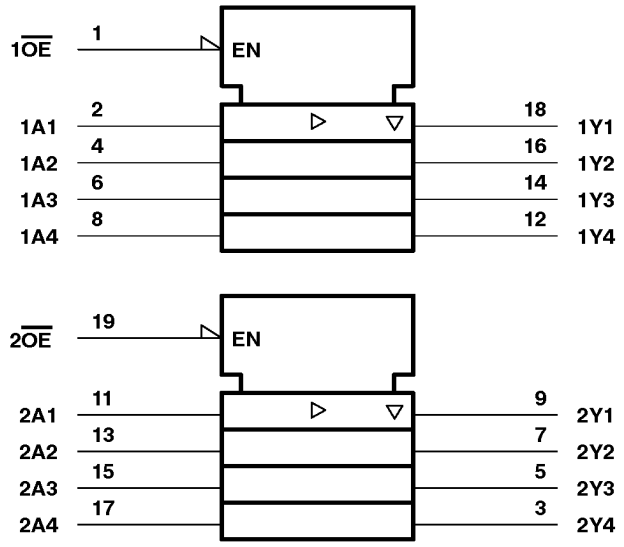
The CDC244 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The CDC244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each driver)

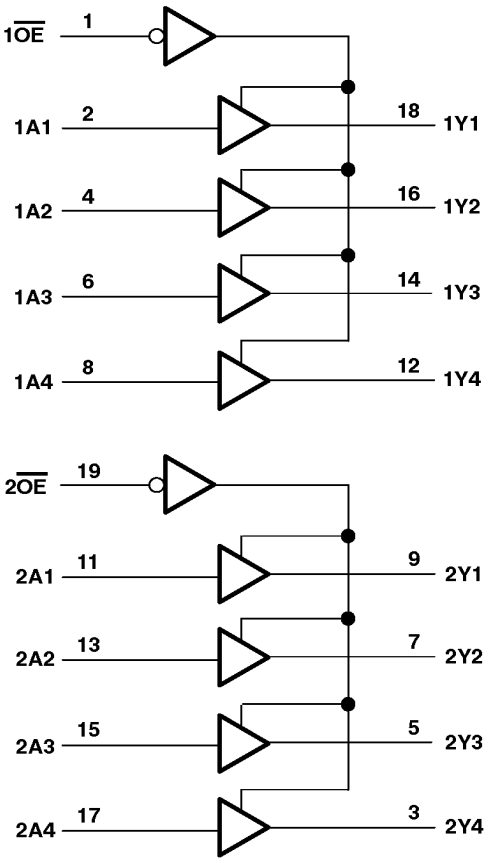
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) . . −0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . −18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) . . . . . 0.6 W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
f_{clock}	Clock frequency			MHz
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP†	MAX			
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –3 mA		2.5			2.5		V
	V_{CC} = 5 V,	I_{OH} = –3 mA		3			3		
	V_{CC} = 4.5 V	I_{OH} = –32 mA		2			2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55		0.55	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				10‡		10‡	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				–10‡		–10‡	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100		±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		1	250		250	µA
			Outputs low		24	30		30	mA
			Outputs disabled		0.5	250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5	mA
			Outputs disabled			0.05		0.05	
		Control inputs				1.5		1.5	
C_i	V_I = 2.5 V or 0.5 V				3				pF
C_o	V_O = 2.5 V or 0.5 V				8				pF

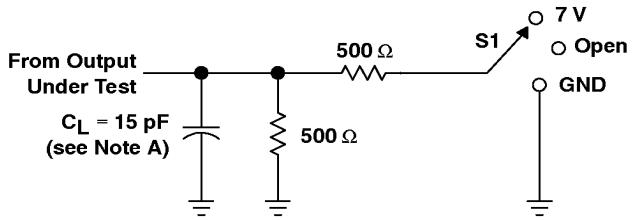
† All typical values are at V_{CC} = 5 V.
‡ This limit may vary among suppliers.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP†	MAX			
t_{PLH}	A	Y	1	2.6	4.1		4.6	ns
t_{PHL}			1	2.9	4.2		4.6	
t_{PZH}	$\overline{OE}$	Y	1.1	3.1	4.6		5.1	ns
t_{PZL}			2.1	4.1	5.6		6.1	
t_{PHZ}	$\overline{OE}$	Y	2.1	4.1	5.6		6.6	ns
t_{PLZ}			1.7	3.7	5.2		5.7	
$t_{sk(o)}$	A	Y			750		750	ps

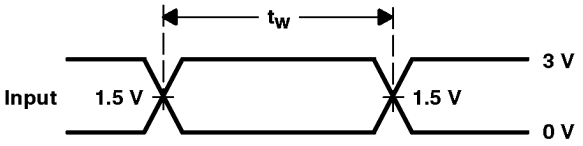
† All typical values are at V_{CC} = 5 V.

PARAMETER MEASUREMENT INFORMATION

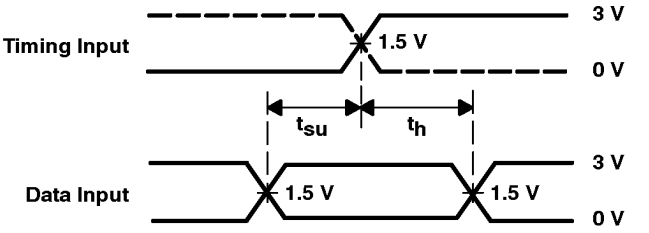


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

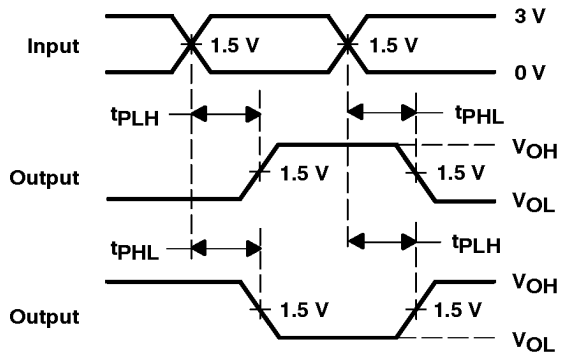
LOAD CIRCUIT FOR OUTPUTS



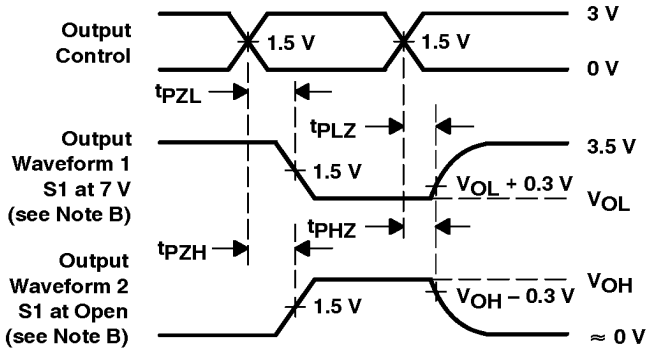
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

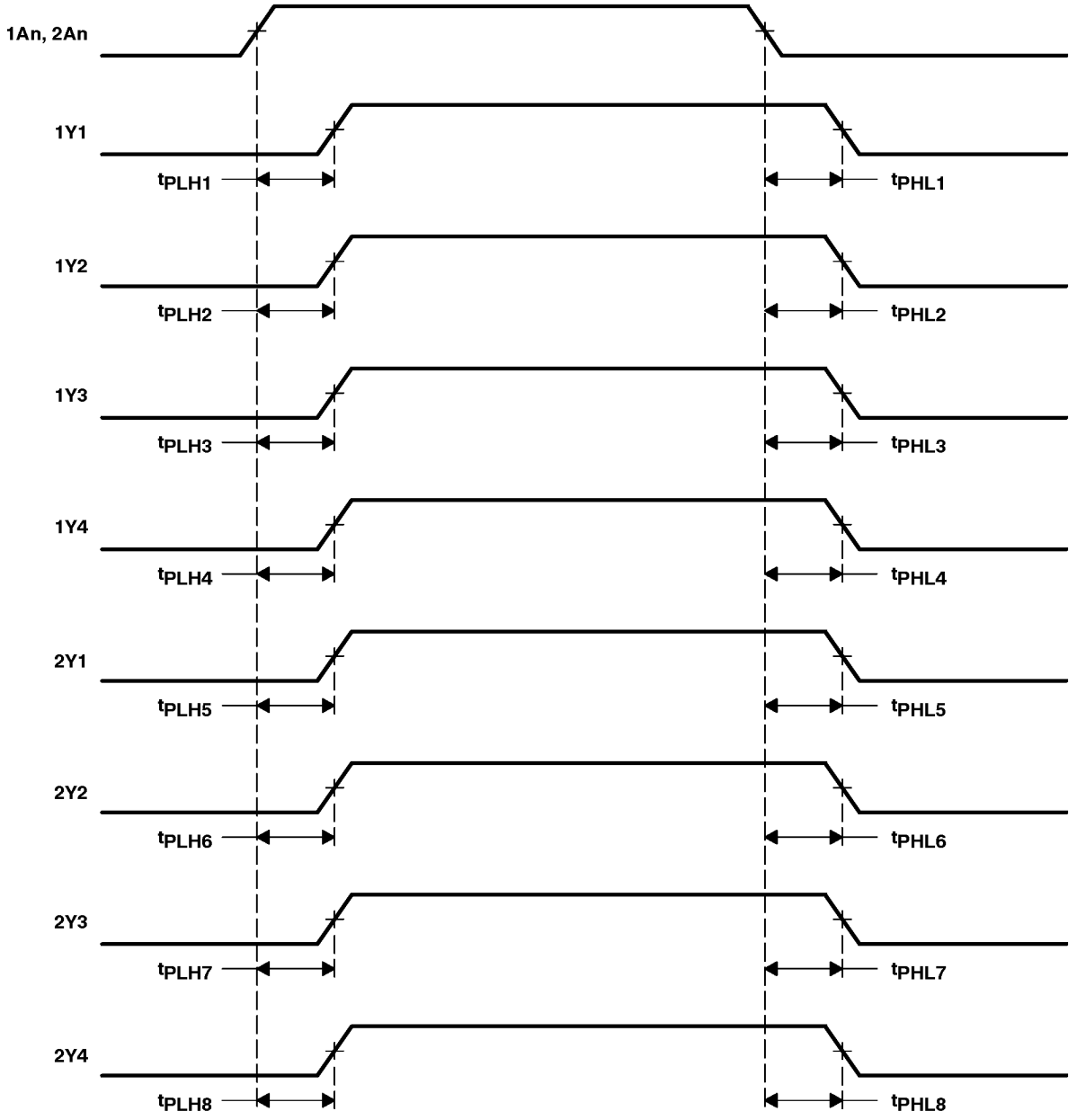


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, . . . , 8)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, . . . , 8)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$