THAT Corporation

IC RMS-Level Detector

THAT 2252

FEATURES

- True RMS Response
- Wide Dynamic Range: >80 dB
- High Crest Factor: 8 (1 dB error)
- Wide Bandwidth: to > 20 kHz
- Logarithmic Output Scaling
- Low Cost: $2.20 in '000s
- Single In-Line Package
- Matches 2180 and 2181 Series VCAs

APPLICATIONS

- Meters
- Spectrum Analyzers
- Compressors
- Expanders
- Oscillators
- Psychoacoustic Modeling
- Noise Measurement

Description

The THAT 2252 integrated-circuit rms-level detector is designed to convert an ac input current into a dc output voltage. The output is proportional to the log of the true rms value of the input signal. The parts are housed in a space-efficient plastic 8-pin single-in-line (SIP) package, and require minimal support circuitry. Based on dbx technology and fabricated in a super low-noise process, the 2252 combines wide dynamic range with frequency response to beyond 20 kHz. The logarithmic output is especially convenient for audio applications requiring decibel-linear scaling. The integration time is adjustable via an external R/C pair. With some external circuitry, response to dc is also possible.

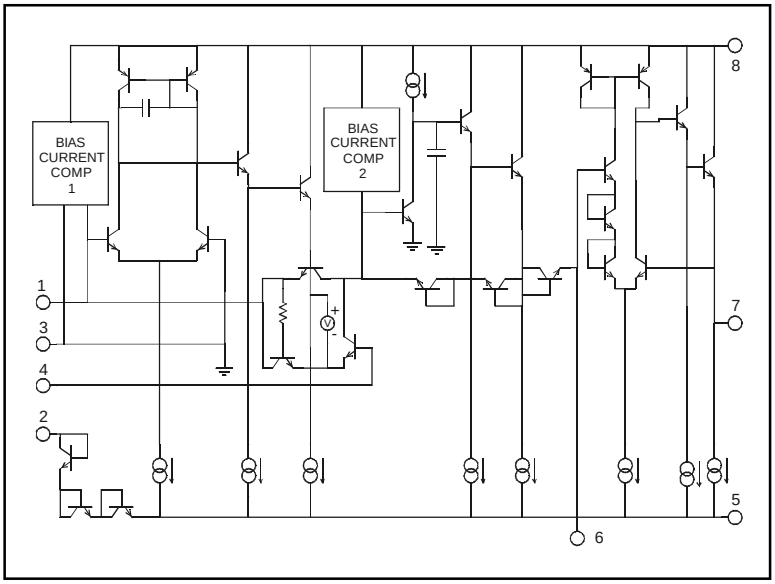


Figure 1. 2252 Equivalent Circuit Diagram

Pin Name	SIP Pin
Input	1
I BIAS	2
Gnd	3
Sym	4
V-	5
Cap	6
Output	7
V+	8

Figure 2. 2252 Pin Assignments

SPECIFICATIONS[1]

Absolute-Maximum Ratings (TA = 25°C)

Positive Supply Voltage (VCC)	+18 V	Power Dissipation (PD)	330 mW
Negative Supply Voltage (VEE)	-18 V	Operating Temperature Range (TOP)	-20 to +75°C
Supply Current (ICC)	10 mA	Storage Temperature Range (TST)	-40 to +125°C

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Positive Supply Voltage	V_{CC}		+4	+12	+15	V
Negative Supply Voltage	V_{EE}		-4	-12	-15	V
Bias Set Current	I_{BIAS}		15	24	50	µA
Signal Current	I_{in}	I_{BIAS} = 24 µA	—	—	1	mA
Timing Current	I_T		1	7.5	50	µA

Electrical Characteristics[2]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current	I_{CC}	No Signal	—	1	3	mA
Equiv. Input Bias Current	I_B	No Signal	—	5	8	nA
Input Offset Voltage	$V_{OFF(IN)}$	No Signal	0	+8	+16	mV
Symmetry Voltage	V_{SYM}		-2	8	+18	mV
Output Scale Factor	$E_O/20\log(I_{in} / I_{in0})$	31.6nA<I_{IN}<1mA				
		T_A=25°C (T_{CHIP} ≈35°C)	6.0	6.1	6.2	mV/dB
Input Current for 0V Output	I_{in0}		$\frac{\sqrt{I_{BIAS} \times I_T}}{3.5}$	$\frac{\sqrt{I_{BIAS} \times I_T}}{2.9}$	$\frac{\sqrt{I_{BIAS} \times I_T}}{2.4}$	
Output Linearity		f_{IN} = 1kHz				
		1µA < I_{in} < 100µA	—	0.1	—	dB
		100nA < I_{in} < 316µA	—	0.5	—	dB
		31.6nA < I_{in} < 1mA	—	1.0	—	dB
Crest Factor		1ms pulse repetition rate				
		0.2 dB error	—	3.5	—	
		0.5 dB error	—	5	—	
		1.0 dB error	—	8	—	
Maximum Frequency for 1 dB additional error		I_{in} ≥ 100µA	—	80	—	kHz
		I_{in} ≥ 10µA		74	—	kHz
		I_{in} ≥ 1µA		30	—	kHz
		I_{in} ≥ 100nA		4	—	kHz
Filtering Time Constant				$(.026)\frac{C_T}{I_T}$		s
Output TempCo	$\Delta E_0 / \Delta T_{CHIP}$	Re: T_{CHIP} = 27°C	—	0.33	—	%/°C

1. All specifications subject to change without notice.
2. Unless otherwise noted, T_A=25°C, V_{CC} = +15V, V_{EE}= -15V. Test circuit is as shown in Figure 4. SYM is adjusted for minimum ripple at V_{out} with V_{in}=1 V_{RMS}, 100 Hz.

Theory of Operation

The THAT 2252 RMS-Level Detector is designed for high performance in audio-frequency applications requiring logarithmic output, rms response, and wide dynamic range. The parts compute rms level by rectifying input current signals, converting the resulting current waveform to a logarithmic voltage, and applying this voltage to a log-domain filter.

Current Rectification

Figure 3 presents a simplified internal circuit diagram of the 2252. The input signal current, I_{in}, flows in pin 1, the input pin. OA1 drives the base of Q3 and the emitter of Q1 (through V1) to maintain pin 1 at virtual ground potential. A negative input current (flowing out of pin 1) will tend to drive the inverting input of OA1 negative, driving OA1's output positive, turning on Q3. V1 is designed to cut off Q1 while Q3 is on. Therefore, negative input currents are forced to flow through the collector-emitter of Q3.

Positive I_{in} will drive OA1's output negative, cutting off Q3 and turning on diode-connected transistor Q1. Positive input current is thereby forced to flow through the collector-emitter of Q1. Pin 4 is normally connected through a 20 Ω resistor to ground (see Figure 4, *Typical Application Circuit*, Page 4, and *Symmetry Adjustment*, Page 6), so the base-emitter potential of Q2 is the same as that of Q1. Therefore, the current in the collector of Q2 (I_{C2}) will mirror that in the collector of Q1 (I_{C1}), which equals the positive input current.

Since the input impedance of OA2 is high, the current in the emitter of Q4 (I_{C4}), is the sum of the currents I_{C2} and I_{C3}. The mirror action of Q1/Q2 reverses the positive input currents so that they add to the negative input currents in Q4. The current in Q4, therefore, is equal to the absolute value of the input current.

Mathematically,

$$I_{C3} = \begin{cases} -I_{in}, I_{in} \le 0 \\ 0, I_{in} > 0 \end{cases}, \text{and } I_{C1} = I_{C2} = \begin{cases} 0, I_{in} \le 0 \\ I_{in}, I_{in} > 0 \end{cases}.$$

But, $I_{C4} = I_{C3} + I_{C2} = I_{C3} + I_{C1}$

$$= \begin{cases} -I_{in}, I_{in} < 0 \\ I_{in}, I_{in} > 0 \end{cases}$$

$$= |I_{in}|.$$

See Figure 3 for definitions of these currents.

Logging Action

OA2, together with Q4 and Q5, forms a log amplifier. By using two diode-connected transistors in the feedback loop of OA2, the 2252 produces a voltage proportional to twice the log of IC4 at the output of OA2. This voltage, V_{log}, is therefore proportional to the log of the square of the input current, plus a bias voltage (V2).

Mathematically,

$$V_{\log} = 2V_T \ln\left(\frac{I_{C4}}{I_S}\right) + V_2$$

$$= 2V_T \ln(I_{C4}) - 2V_T \ln(I_S) + V_2$$

$$= V_T \ln(I_{C4})^2 - 2V_T \ln(I_S) + V_2$$

$$= V_T \ln|I_{in}|^2 - 2V_T \ln(I_S) + V_2,$$

Where V_T is the thermal voltage, $\frac{kT}{q}$, and I_S is the reverse-saturation current of Q4 and Q5 (assumed to be the same in each).

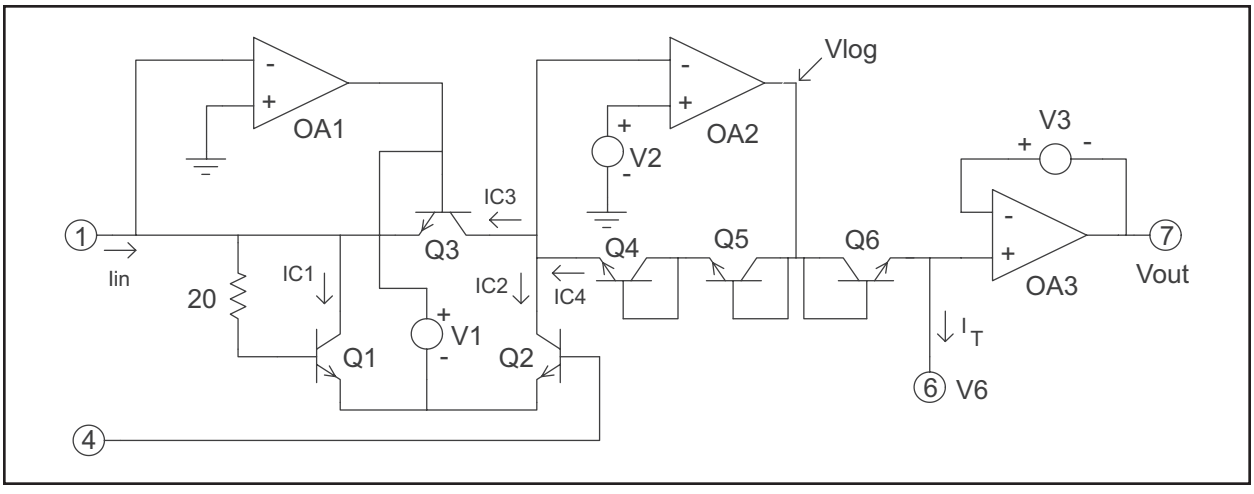


Figure 3. Simplified Internal Schematic

Computing the Mean

In the classic mathematical definition of rms value, the time integral of the square of the signal must be evaluated over infinite time. Obviously, for a practical measurement, only a finite time is available, which leads to the question of how to weight events occuring at various times. Traditionally, the simplest and most meaningful weighting is exponential in time, giving highest weight to the most recent history, and exponentially less weight to increasingly older events. This weighting corresponds to convolution in time with the familiar exponential weighting function, $e^{\frac{-t}{\tau}}$.

To accomplish this weighting, Pin 6 is normally connected to a capacitor and a negative current source. (Refer to the *Typical Application Circuit* in Figure 4. In this circuit, C_T is the capacitor and R_T together with V- form the current source.) This current source establishes a quiescent dc bias current, I_T, through Q6. Over time, the capacitor charges to 1 V_{BE} below V_{log} (the potential at the output of OA2).

The instantaneous emitter current in Q6 is proportional to the antilog of its V_{BE}, which is the difference between Q6's base voltage and the voltage at pin 6. The potential at the base of Q6 represents the log of the *square* of the input current, while the emitter of Q6 is held at ac ground via the capacitor. Since Q6's emitter current is proportional to the antilog of its V_{BE}, the current in Q6 is proportional to the square of the instantaneous input current.

Note that this antilogging only takes place for *dynamic* signals. For a dc input, the output of OA2 represents the square of the input current. After charging, the external timing capacitor voltage again approaches one diode drop below V_{log}. The exact value of the diode drop will be determined by the bias current I_T. However, for sudden increases in the input current I_{in}, the current available to charge the capacitor C_T is proportional to the square of the short-term increase in input current.

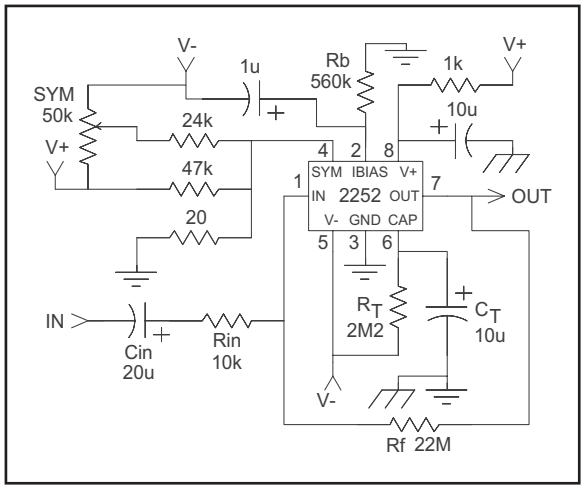


Figure 4. Typical Application Circuit (±15V)

The "dynamic" antilogging causes the capacitor voltage to represent the log of the mean of the square of the input current.

Time Constants

Another way of looking at this situation is to consider the action of Q6 and C_T as a first-order filter in the log domain. Q6 and C_T establish a single pole at a frequency determined by a) the impedance of Q6 at the bias current I_T and b) the value of C_T. The time constant τ is given below.

$$\tau = C_T \frac{V_T}{I_T}$$

$$= C_T \frac{0.0259}{I_T}, \text{ at } 300^\circ \text{ Kelvin.}$$

The result is that the voltage at pin 6 represents the average (or mean) of the square of the input signal, averaged over the time constant τ. The averaging corresponds to convolution with the time weighting of a simple RC circuit. Mathematically, this is as follows:

$V6 \propto \ln\left(\frac{1}{T^2}\int_0^T I_{in}^2 e^{\frac{-t}{\tau}} dt\right)$, where T is the time at which the average level is computed. Note that $\left(e^{\frac{-t}{\tau}}\right)$ represents the exponential time weighting imposed by the log-domain filter.

How fast the 2252 acquires a signal (the "attack"), and how fast it returns to rest following a signal (the "release"), are locked in relationship to each other by the nature of the exponential time-weighting imposed by this log-domain filter. Separate attack and release adjustments are not possible within the constraint of rms response.

The time response for typical values of I_T and C_T (the circuit of Figure 4) is shown in Figure 5, which shows the 2252's response to a 100 ms, 1 kHz tone burst at ~ +10 dBV followed by ~500 ms of 1 kHz at ~ –30 dBV. The top trace is the input tone burst (at 10 V/div), the bottom trace is the output at 50 mV/div. The time scale is 50 ms/div.

The shape of the attack and release waveforms is determined by the interaction of the exponential response of the log-domain filter with the log-representation of the signal. The straight-line decay follows from the fact that the natural release of the exponential time weighting is a decaying exponential in the linear world. This maps to a straight line in the log representation. The attack in the photo appears exponential, but actually follows the $(1-e^{-t})$ shape of the attack curve. The transformation from the linear to the log world steepens the apparent attack shape.

The time constant, τ, also determines the amount of ripple (at frequency $2f_{in}$) in the output for any

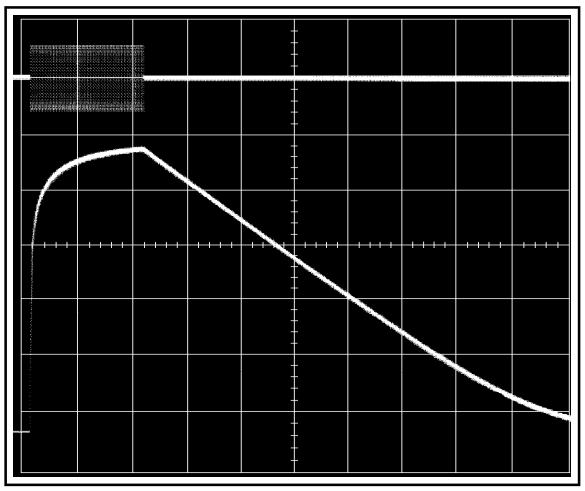


Figure 5. Tone Burst Response

given input frequency, f_{in}. Larger values of τ reduce ripple at the expense of longer attack and release times. For $f_{in} >> \frac{1}{4\pi t}$, the ripple voltage at the output is given by: $V_R \approx \frac{V_T}{4\pi\sqrt{2} f_{in} t}$, where V_R is the rms ripple voltage.

Taking the Square Root

The square root portion of the Root-Mean Square is implied by the constant of proportionality for the output voltage: it is not computed explicitly. This is because, in the log representation, taking the square root is equivalent to division by two. The voltage at pin 6 is proportional to the mean of the square at approximately 3 mV/dB, and proportional to the *square root* of the mean of the square at approximately 6 mV/dB.

Output Buffering and Level Shifting

The voltage at pin 6 is buffered by OA3, and level shifted down by the bias voltage V3. Level shifting is required so that the output voltage will be zero when the rms input current reaches a predetermined value, I_{in0}. This current is often called *level match*, and represents the 0 dB reference of the circuit.

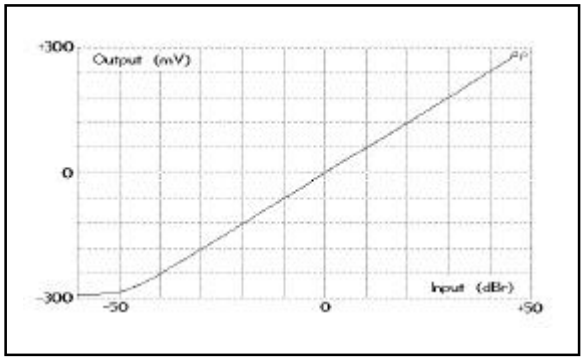


Figure 6. 2252 DC Output Vs. AC Input Level

The various level shifts throughout the 2252 are as follows: V2 represents one diode drop, so the voltage at the emitter of Q4 is $+1V_{BE}$. The output of OA2 is two diode drops higher than this, or $+3V_{BE}$. Q6 will subtract one diode drop from the output of OA2, so the voltage at pin 6 will be $+2V_{BE}$. Finally, V3 represents two diode drops, setting the voltage at pin 7 to 0 V.

Of course, the actual value of all these level shifts is dependent on the currents through the transistors responsible for each V_{BE}. These currents, in turn, are dependent on the bias programming current in pin 2 (I_{BIAS}) and the timing current pulled from pin 6 (I_T). This dependence may be given as follows:

$I_{in0} = \frac{\sqrt{I_{BIAS}\ I_T}}{2.9}$, where I_{in0} is the input current causing 0 V output, I_T is the current in pin 6, and I_{BIAS} is the current in pin 2. The factor 2.9 derives from the geometry of the transistors involved.

Figure 6 plots output voltage versus input level for a 2252 in its recommended circuit configuration (Figure 4). In this plot, 0 dBr ≈ 43 mV. Figure 7 plots output voltage for several different constant-amplitude frequency sweeps for the same circuit. The vertical divisions are 60 mV apart, representing approximately 10 dB increments. Full audio bandwidth is maintained over a 60 dB dynamic range.

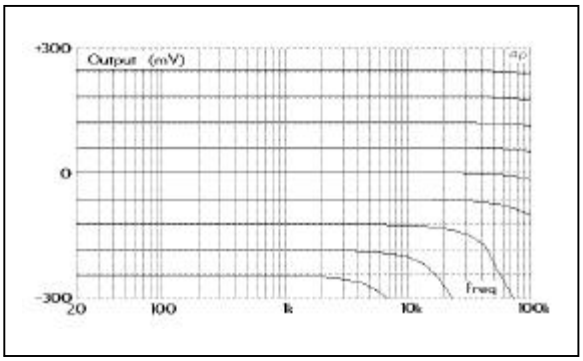


Figure 7. 2252 DC Output Vs. Frequency at Various Levels

Current Programming

All the internal current sources in the 2252 are slaved to the current in pin 2, I_{BIAS}. As mentioned above, the choice of this current affects I_{in0}. I_{BIAS} is normally set by a resistor from pin 2 to ground (V_{CC} would do also). Note that the voltage at pin 2 is normally V_{EE} + 2.1 V, where V_{EE} is the negative supply voltage.

Symmetry Adjustment

The rectifier (Q1 through Q3 and OA1) depends on the matching between Q1 and Q2 for accurate re-

production of positive-half input signals. The base of Q2 is brought out to pin 4 in order to allow adjustment for mismatches between these transistors and for the input offset voltage of OA1. Pin 4 should be connected to a variable low-impedance voltage source capable of supplying a few millivolts (V_{SYM}). The base of Q1 is connected to its collector through a 20Ω resistor to allow matching between the base impedances of Q1 and Q2. A 20Ω source should be used at pin 4 for optimum matching.

Input Bias Currents and Voltages

OA1 will rectify any currents flowing in its feedback network, including the bias current of OA1 itself. Input signals below OA1's bias current will be obscured, with a steady dc output "floor" the result. The input bias compensation for OA1 largely cancels OA1's bias current, improving low-level performance. Even if overcompensated, any uncorrected bias current (positive or negative) in OA1 results in a limit to the low-level resolution of the 2252.

Any dc offset voltage at pin 1 will cause dc input currents to flow if the input is dc coupled. The dc offset at pin 1 is typically 8 mV, so the input should be ac coupled (as shown in Figure 4) for most applications. If low-level performance is not required, dc coupling may be used without further modifications to the application circuits. However, dc coupling *and* good low-level performance are possible with additional external circuitry, as described in the section on *DC Measurements* on Page 9.

Positive equivalent input bias current in OA2 (after correction) will also *add* to the output level reading. This is because the equivalent input bias current is supplied through Q4 and Q5, which adds to the dc level at the output of OA2. OA2, like OA1, has input bias compensation. While generally extending low-level performance, the compensation can cause OA2's net input bias requirement to become *negative,* tending to reverse bias Q4 and Q5. The circuit of Figure 4 uses a 22 MΩ resistor, Rf, to supply increasing dc input current as the 2252 output drops. This forces current to flow in Q2, which overwhelms any negative input bias at OA2 and prevents the current in Q4 and Q5 from reversing.

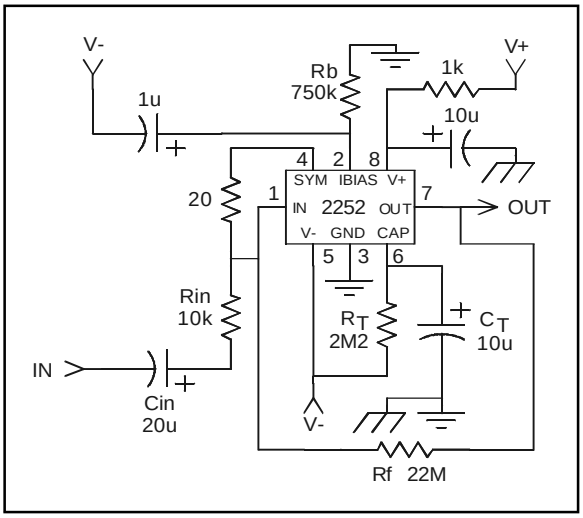


Figure 9. Application Circuit Without Symmetry Control

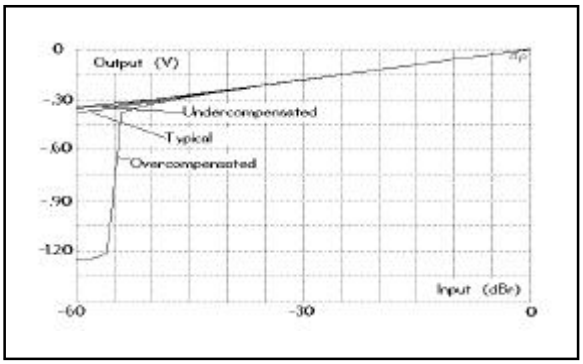


Figure 8. Low Level Output from Several 2252s (no Rf)

Rf is responsible for the flattening of the low-level response shown in Figure 6 (Page 5). The feedback current provided enforces a lower limit to the resolvable input current. Without this feedback, those 2252s where the OA2 input bias is overcorrected will exhibit a sharp downward swing in output level at low input signals (see Figure 8). For many applications, such low-level response is not necessary. In such cases, Rf may be deleted, as shown in Figure 11. See further discussion of this subject in *Output Considerations*, (Page 8).

Applications

The intended purpose of the 2252 is to compute the log of the time-weighted root-mean-square of an input current signal. Several practical considerations apply when attempting to make full use of the 100 dB dynamic range of the device.

Input Considerations

The 2252 input is intended to accept a current: as is clear from Figure 3 (page 3), pin 1 is a summing junction supplied with internal negative feedback. Maximum input current is on the order of 1 mA, limited by internal device characteristics. The minimum practical input current is determined by the effects of internal bias currents (whether from OA1, OA2, or the effect of V1). At currents as low as 31 nA, approximately 1 dB error in reading will result from interal bias currents.

The gain of the input op amp (OA1) is sufficient to provide effective logging for $R_{in} \geq 10$ kΩ. However, with $R_{in} < 10$ kΩ., low level and high frequency performance will suffer due to the finite open-loop gain of OA1. This is because OA1 is required to swing across a "dead zone" between turning on Q1 and Q3. The dead zone is reduced by V1. But, V1 is small (≈0.5 V) to maintain low-level tracking, so OA1 must still swing through several tenths of a volt at each reversal of the input polarity. The smaller the value of R_{in}, the higher the loop gain demanded from OA1 for accurate rectification.

Therefore, for good high-frequency performance, R_{in} should be 10 kΩ or larger. Otherwise, choose R_{in} based on the desired input voltage at level match, E_{in0}, and I_{in0} as follows: $R_{in} = \frac{E_{in0}}{I_{in0}}$

The negative input of OA1 typically rests at +8 mV. If dc coupled, this will cause an input current to flow which will effectively set a low-level "floor" below which readings will be obscured. Therefore, ac coupling is required if low level signals are to be accurately observed. Choose the value of the ac coupling capacitor (C_{in} in Figure 4) based on the value of R_{in} and the desired low-frequency limit. $C_{in} = \frac{1}{2p\, R_{in}\, F_C}$, where F_C is the desired 3 dB-down point. (For dc coupling, see the section on page 9, *DC Measurements*.)

Symmetry Adjustment

As noted earlier, the rectifier relies on the matching of Q1 and Q2 for precise reproduction of positive-half input currents. Q2's base is brought out to pin 4 to allow adjustment of this match. Pin 4 should be connected to a 20 Ω voltage source capable of supplying from –4 mV to +20 mV. The application circuits in Figure 4 (page 4) and Figure 11 (page 6) are typical.

To set the symmetry, apply a low-frequency sine wave to the input. Neither the frequency nor the level are critical: 100 Hz at near level match is usually a good choice. Observe the output waveform with a 'scope while adjusting the symmetry trim. With proper adjustment, the ripple in the output will be almost pure second harmonic of the input frequency. No fundamental frequency should be present in the output. Another method would be to sense ripple in the output via a narrow bandpass filter centered at the fundamental feeding an ac voltmeter: adjust the trim for minimum voltage reading.

The actual voltage required for proper symmetry depends on the input offset voltage of OA1 (typically +8 mV), and the V_{BE} mismatch between Q1 and Q2 (< ±6 mV). For less critical applications where precise rectification is not required, pin 4 may be connected to a voltage matching the input offset voltage of OA1, preferably through a 20 Ω resistor (to match the 20 Ω in Q1's base). The simplest circuit connects pin 4 to pin 1 through a 20 Ω resistor, as shown in Figure 9. This connection ensures that the V_{BE} of Q1 will equal that of Q2, but does not allow for adjustment for any mismatch in the two devices. When using this configuration, one should try to keep the bias programming current below 20 µA, to ensure stable operation.

Time Constants

Both the capacitor (C_T) and current source (I_T) connected to pin 6 control the time constant over which the rms value of the input current is evaluated. Either may be varied, but a few practical considerations influence the choice of values. First, the input bias current of OA3 in Figure 3 will add to the charging current I_T. For small values of I_T, this will affect the accuracy of the resulting time constant. The input bias current for OA3 is typically 100nA, so I_T should be kept above 1 µA.

At the other extreme, I_T flows from OA2 and through Q6 under steady-state conditions. Dynamically, as was mentioned on page 4 in *Computing the Mean*, the current which charges C_T is proportional to the square of the short-term increase in I_{in}. A sudden 30 dB increase in input causes a 60 dB increase in charging current. For example, if I_T is 10 µA, the peak charging current will be 10 mA. However, if I_T were 100 µA, the peak charging current called for would be 100 mA. The devices within the 2252 will not support this high a current demand, so timing will be less accurate under this condition. (The *steady-state* output voltage will be accurate, since over time the error will be "forgotten" due to the time-weighting $e^{\frac{-t}{t}}$. However, the dynamic response will be incorrect.)

The best performance normally results when 5 µA < I_T < 50 µA. C_T is usually chosen to be a convenient value which results in the desired time constant τ, and an I_T within these limits. See *Time Constants* (page 4) for the relationship between τ, I_T and C_T.

Since C_T is commonly 1µf or larger, this capacitor is often a polarized electrolytic or tantalum. V6 is normally positive approximately $2V_{be}$ (≈1.4 V), which determines the polarity of C_T. Leakage in C_T will add to I_T, so low-leakage electrolytics or tantalums are preferred. Tantalum, once preferred for long-term stability and low leakage, has been largely superceded by premium electrolytic types which are available in low-leakage, high-stability versions. When using an electrolytic, however, it is good practice to select a voltage rating higher than absolutely necessary (at least 15 V is recommended).

When a resistor to the negative supply is used as the I_T current source (as in the circuits shown here), determine its value by the equation:

$R_T = \frac{|V_{EE}| + 1.4}{I_T}$, where V_{EE} is the negative supply voltage.

Bias Programming

As shown in Figure 1 (page 1), pin 2 is connected to the negative supply through three diodes in series. Its typical voltage is V_{EE} + 2.1 V. The current in these diodes, I_{BIAS}, controls the current sources throughout the 2252, and therefore affects the bandwidth of the device, as well as I_{in0}. Because it is responsible for programming so many currents, I_{BIAS} should be restricted to a relatively narrow range about the nominal 24 µA.

Normally, I_{BIAS} is chosen to fine-tune I_{in0}, the 0 dB reference point. $I_{BIAS} = 8.4 \frac{I_{in0}^2}{I_T}$. The factor 8.4 derives from the geometry of the devices in the 2252.

As with the value of R_T, R_b is determined by the desired I_{BIAS} and the negative supply voltage, as follows: $R_b = \frac{|V_{EE}| - 2.1}{I_{BIAS}}$.

Power Supply Bypassing

The 2252 is not particularly sensitive to power supply impedances, but the high charging currents which are possible in C_T *must* be kept out of the PC board ground and voltage supply system for good results. The application circuits show a 1 kΩ resistor in series with the positive supply pin (pin 8), and a 10 µf capacitor bypassing this pin to ground. The ground end of this capacitor is intended to be connected directly to the ground end of C_T. One (and *only* one) point on this trace should be connected to the circuit ground system, since high currents flow in this trace during input signal transients.

Figure 8 illustrates the flow of current, I_{CHARGE}, during an input transient. Note that I_{CHARGE} is confined to a local loop, flowing from C_B through OA2 and Q6 (within the 2252) into C_T, and returning directly to C_B. By keeping the return trace short, and connecting it to system ground at only one point, high currents are kept out of the overall ground system, while C_T maintains its reference to ground potential through the *single* connection to ground.

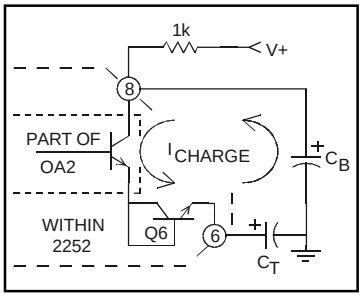


Figure 10.
Decoupling Supply Transients

Another bypass capacitor is required at pin 2 (the I_{BIAS} pin). Typically, with $I_{BIAS} \approx 24$ µA, the impedance at pin 2 is approximately 3 kΩ to V–. If the input signal capacitively couples into pin 2, I_{BIAS} will be modulated at the input signal frequency. This modulation adds signal voltage (as ripple) to the output at pin 7. (Recall that, ideally, the 2252 produces ripple only at the second harmonic of the input signal.) When the 2252 is used to control the gain of a voltage-controlled amplifier (VCA) such as the THAT 2180 or 2181, this fundamental-frequency ripple will cause second harmonic distortion in the VCA. Bypassing pin 2 to the negative supply shunts any signal-related currents around the 2252 bias system, preventing this ripple from occuring.

Output Considerations

The output of the 2252 (pin 7) presents a low source impedance, but it is somewhat limited in available current drive. Referring to Figure 1 (page 1), the negative current source at the output pin is approximately 10 I_{BIAS}. Therefore, for the typical I_{BIAS} of 24 µA, the maximum current sink at pin 7 is 240 µA. (The 2252 will source considerably more than this current if required.) Since the output voltage normally swings between ±300 mV, the 2252 will directly drive loads of greater than 1.5 kΩ without difficulty.

In the section on *Input Bias Currents and Voltages* (page 6), it was noted that the 2252 output is generally proportional to the log of the ac rms input current. But, at low levels (<20 nA input current), the input bias compensation in internal opamp OA2 in Figure 3 (page 3) can cause a sharp increase in the output change with input, as shown in Figure 8, (page 6). Since this effect is dependent on the accuracy of the bias compensation, some 2252s will exhibit this behavior, but most will not.

For most applications, where consistent low-level response is desireable, the 2252 should be configured to supply its own "correction" signal to prevent this discontinuity from occuring, as shown in the circuit of Figure 4, (page 4). In this circuit, a 22 MΩ resistor (Rf) is connected from the output of the 2252 back to the input.

When the output voltage is near 0 V, Rf contributes negligible current to the input of the detector. For positive output voltages, the current in Rf is very small compared to the ac input signal which causes a positive output, so its effect is again negligible. However, as the ac input signal drops in level, the dc output goes negative, supplying more and more input current through Rf, which tends to drive the dc output positive. The point at which the two effects will balance is dependent on I_{BIAS}, I_T, and the size of the feedback resistor. In the circuit of Figure 4, the output will "bottom out" at approximately -300 mV, where Rf supplies ~14 nA of dc current to the input.

Rf establishes a stable "floor" in the 2252's response. However, this self-supplied lower limit will obscure very low-level input signals which could be measured by those 2252s with good input-bias correction at OA2 of Figure 3. If accurate low-level

response is quite important, the 2252s may be selected, and Rf may be omitted, as shown in Figure 11. The 2252s should be selected on the basis of accurate low-level, low-frequency performance (see Figure 8, page 6).

The circuit of Figure 11 may also be used with *unselected* 2252s for applications where accurate low-level performance is unnecessary. However, the relatively low cost of a 5% 22 MΩ resistor usually argues in favor of its use.

DC Measurements

As noted earlier, the 2252 is primarily intended for measuring the rms value of ac signals. This follows from the 2252's relatively high input offset voltage (typically +8 mV). If the input is dc coupled, the input offset voltage will cause a dc current to flow in the input, which will interfere with precise low-level rectification, ultimately producing a "floor" below which input signals will be obscured. For typical values of $R_{in} \approx 10$ kΩ, this dc input current would be 800 nA, upsetting rectification for ac signals below approximately 8 µA, and almost completely obscuring signals below 800 nA peak. C_{in} in Figures 4 and 11 blocks this dc current, extending low-level performance to well below 100 nA.

However, as shown in Figure 12, with a few added parts, it is possible to extend response to dc with little loss in low-level accuracy.

The essential purpose of the added circuitry (OA1, OA2 and associated parts) is to buffer the input offset voltage (at pin 1) and add it to the input signal. The circuit of Figure 12 operates as follows.

As has been noted, pin 1 is a virtual ground. Theoretically, the voltage at pin 1 is only the dc offset of the 2252's internal input amplifier, $V_{OFF(IN)}$. Practically, the voltage at pin 1 will consist of this offset plus a small ac signal determined by the value of R_{in} and the loop gain of the internal amplifier. OA2 is intended to buffer $V_{OFF(IN)}$ without drawing any additional current from the pin 1 node. For the output of OA2 to be an accurate representation of $V_{OFF(IN)}$, OA2 must be a low drift, low input bias current opamp, and should have either low input offset voltage (< 0.1 mV) or be trimmed to have low input offset. Typical choices would include an OP07 or an LM108A with a trim for offset voltage.

The voltage at OA2's output is divided by 2 through the two 10 kΩ resistors R_1 and R_2. The 1 µf capacitor bypasses any ac signal at the output of OA2 so that only dc is present at the noninverting input of OA1. Assuming that the input to the entire circuit is connected to a 0 Ω voltage source, the voltage gain from the noninverting input of OA1 to its output will be 2.0, so the combined gain from the output of OA2 to the output of OA1 is unity.

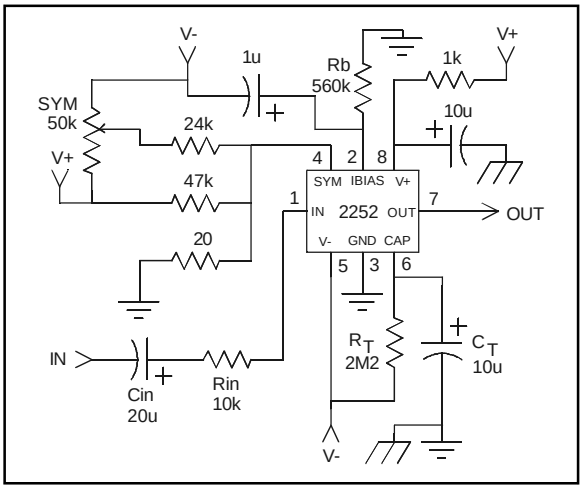


Figure 11. Extended Low-Level Range with Selected 2252s

In this fashion, the dc voltage at the output of OA1 is equal to $V_{OFF(IN)}$ plus the input voltage. Under no-signal conditions, no current flows in R_{in}. With signal, this current is $\frac{V_{in}}{R_{in}}$. Of course, OA1 must also be a low-offset opamp, though its input current is not as critical as that for OA2. Typical choices here would include an OP27 or an LM308A type with offset-voltage trimming.

An additional consideration is that R_1, R_2, R_3 and R_4 should be precision tolerance types, or the voltage applied to R_{in} will not accurately represent $V_{OFF(IN)}$. The source impedance of the voltage to be measured will also affect the gain to $V_{OFF(IN)}$. For well-defined, but non-zero source impedances, reduce the value of R_3 by the value of the source. For uncontrolled, non-zero source impedances, the input signal should be buffered.

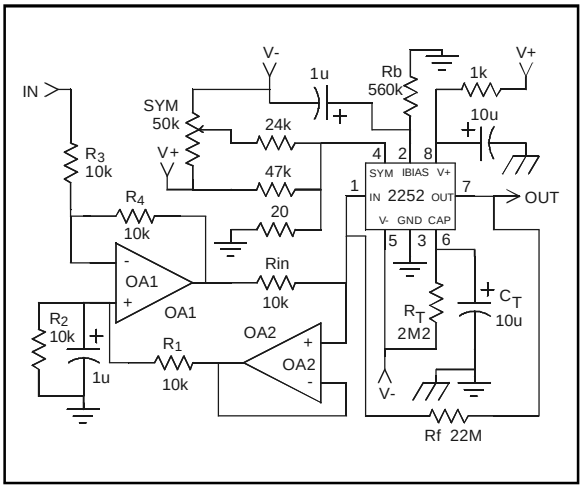


Figure 12. Measuring DC and AC Signals

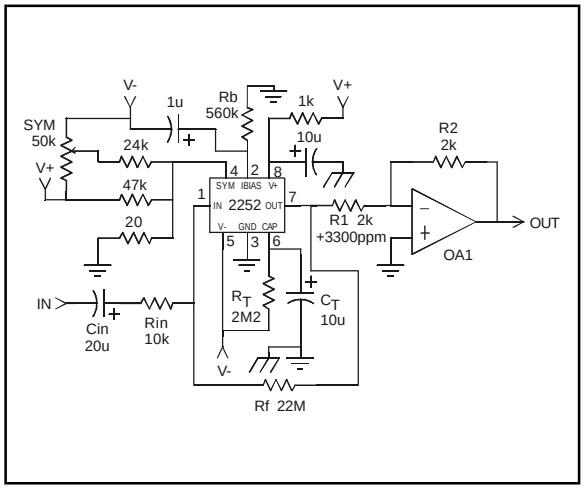


Figure 13. Temperature Compensating the 2252

With this technique, the frequency response is extended to dc, while a slight loss in low-level accuracy results from the additional bias current drawn by OA2.

Temperature-Compensated Measurements

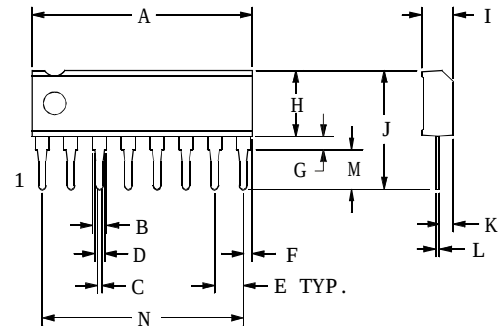
In certain applications, the 2252 may be used for high-precision measurements where the 0.33% / °C variation in output scaling may be unacceptable. For these situations, the output should be temperature compensated through the use of a 3300ppm / °C resistor. Such resistors are available from RCD Components, Inc., 3301 Bedford St., Manchester, NH, USA [(603)-669-0054] and KOA/Speer Electronics, PO Box 547, Bradford, PA, 16701 USA [(814)-362-5536]. Figure 13 shows a typical circuit. For good results, R1 should be located physically close to the 2252 to optimize temperature tracking.

Unusual Applications

Since the 2252 contains a precision rectifier followed by a logging stage, it is possible to think of other ways to apply the part beyond its conventional use as an rms-level detector.

Log Amplifier

In applications where precision logging is required, the rectifier can be entirely bypassed by driving the input with a single-sided dc signal, and the logged output used directly. In such cases, the timing capacitor (C_T) connected to the pin 6 should be reduced to a small value (1~10 nf) to quiet noise in the output while avoiding significant delay in the response.



ITEM	MILLIMETERS	INCHES
A	19.5 +0.2/-0	0.77 +0.008/-0
B	1.25	0.049
C	0.65	0.026
D	0.85	0.033
E	2.54 ±0.2	0.100 ±0.008
F	0.9	0.04
G	1.2	0.05
H	5.8 +0.2/-0	0.23 +0.008/-0
I	2.8 +0.1/-0	0.11 +0.004/-0
J	10.5 ±0.5	0.413 ±0.02
K	1.3	0.05
L	0.3	0.012
M	3.5 ±0.5	0.14 ±0.02
N	17.78 ±0.3	0.700 ±0.012

Figure 14. SIP Package Outline

Log-Responsive Peak Detector

Where peak detection is desired, the 2252 may be configured with very fast time constants (as in the *Log Amplifier* above), and followed by a peak hold amplifier. The advantage of using the 2252 for this application is that the 2252 provides rectification and logging before the peak detector, which allows extremely wide dynamic range in the resulting signal.

Closing Thoughts

THAT Corporation welcomes comments, questions and suggestions regarding this device, its design and application. Our engineering staff has extensive experience in applying this part to commercial circuits. We are pleased to offer assistance in optimizing your circuitry to adapt the 2252 to your particular application. Please feel free to contact us with your thoughts and questions.